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### Product Portfolio

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> (mA)				Standby, I <sub>SB2</sub> (μA)	
		f = 1 MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[1]</sup>	Max		Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max	Typ <sup>[1]</sup>	Max
CY62157ELL	Industrial	4.5	5.0	5.5	45	1.8	3	18	25	2	8
CY62157ELL	Automotive	4.5	5.0	5.5	55	1.8	4	18	35	2	30

### Pin Configurations

Figure 1. 44-pin TSOP II pinout <sup>[2, 3]</sup>

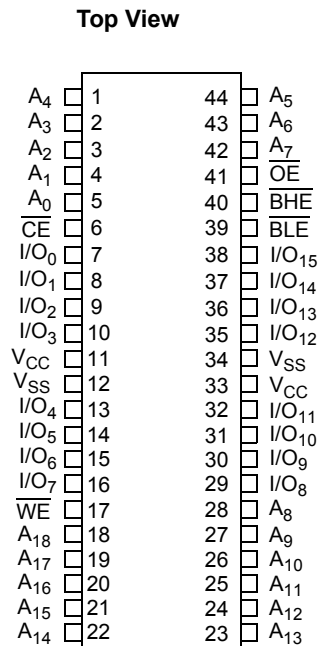
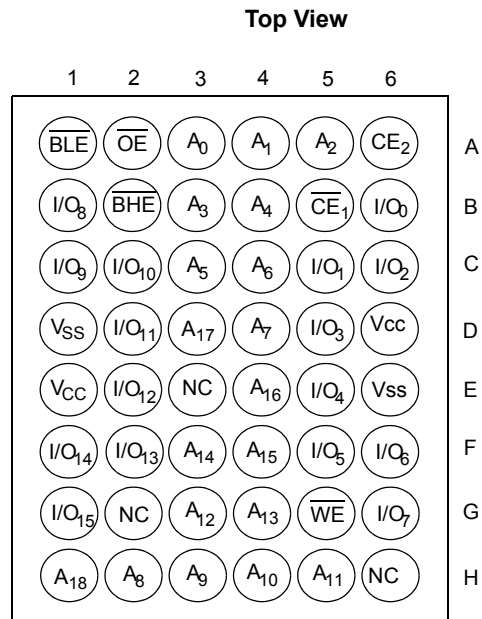


Figure 2. 48-ball VFBGA pinout <sup>[2]</sup>



**Notes**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
2. NC pins are not connected on the die.
3. The 44-pin TSOP II package has only one chip enable ( $\overline{CE}$ ) pin.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .....	-65 °C to + 150 °C
Ambient Temperature with Power Applied .....	-55 °C to + 125 °C
Supply Voltage to Ground Potential .....	-0.5 V to 6.0 V
DC Voltage Applied to Outputs in High Z State <sup>[4, 5]</sup> .....	-0.5 V to 6.0 V
DC Input Voltage <sup>[4, 5]</sup> .....	-0.5 V to 6.0 V

Output Current into Outputs (LOW) .....	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015) .....	> 2001 V
Latch up Current .....	> 200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[6]</sup>
CY62157ELL	Industrial	-40 °C to +85 °C	4.5 V to 5.5 V
	Automotive	-40 °C to +125 °C	

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial)			55 ns (Automotive)			Unit
			Min	Typ <sup>[7]</sup>	Max	Min	Typ <sup>[7]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 4.5 V   I <sub>OH</sub> = -1 mA	2.4	-	-	2.4	-	-	V
		V <sub>CC</sub> = 5.5 V   I <sub>OH</sub> = -0.1 mA	-	-	3.4 <sup>[8]</sup>	-	-	3.4 <sup>[8]</sup>	
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	-	-	0.4	-	-	0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.2	-	V <sub>CC</sub> + 0.5	2.2	-	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-0.5	-	0.8	-0.5	-	0.8	V
I <sub>Ix</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	-	+1	-4	-	+4	μA
I <sub>Oz</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	-	+1	-4	-	+4	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub>   V <sub>CC</sub> = V <sub>CC(max)</sub>   I <sub>OUT</sub> = 0 mA   CMOS levels	-	18	25	-	18	35	mA
		f = 1 MHz	-	1.8	3	-	1.8	4	
I <sub>SB1</sub> <sup>[9]</sup>	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 V$ or $CE_2 \leq 0.2 V$ or (BHE and BLE) $\geq V_{CC} - 0.2 V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2 V$ , V <sub>IN</sub> $\leq 0.2 V$ , f = f <sub>max</sub> (Address and Data Only), f = 0 (OE and WE), V <sub>CC</sub> = V <sub>CC(max)</sub>	-	2	8	-	2	30	μA
I <sub>SB2</sub> <sup>[9]</sup>	Automatic CE Power Down Current – CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 V$ or $CE_2 \leq 0.2 V$ or (BHE and BLE) $\geq V_{CC} - 0.2 V$ , V <sub>IN</sub> $\geq V_{CC} - 0.2 V$ or V <sub>IN</sub> $\leq 0.2 V$ , f = 0, V <sub>CC</sub> = V <sub>CC(max)</sub>	-	2	8	-	2	30	μA

### Notes

- V<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns for I < 30 mA.
- V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.
- Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V<sub>IH</sub> of 3.5V, please refer to Application Note AN6081 for technical details and options you may consider.
- Chip enables (CE<sub>1</sub> and CE<sub>2</sub>) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

### Capacitance

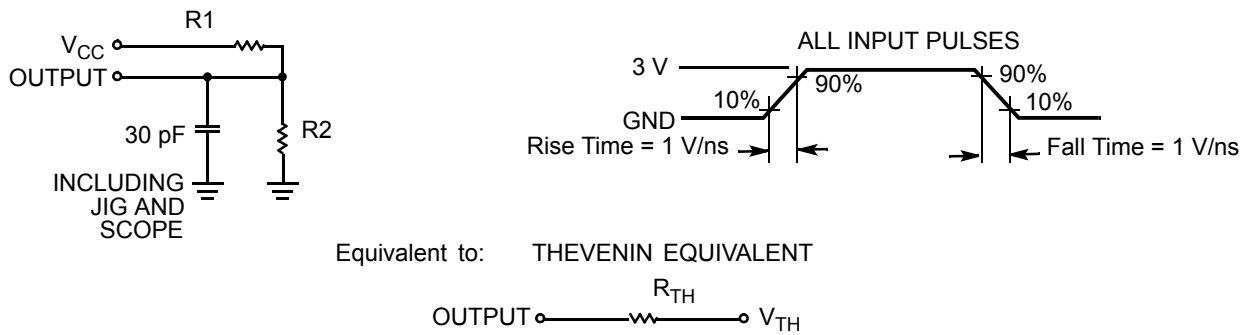
Parameter <sup>[10]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[10]</sup>	Description	Test Conditions	44-pin TSOP II	48-ball VFBGA	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55.84	48.34	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		15.79	8.78	°C/W

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	Values	Unit
R1	1800	Ω
R2	990	Ω
R <sub>TH</sub>	639	Ω
V <sub>TH</sub>	1.77	V

**Note**  
10. Tested initially and after any design or process changes that may affect these parameters.

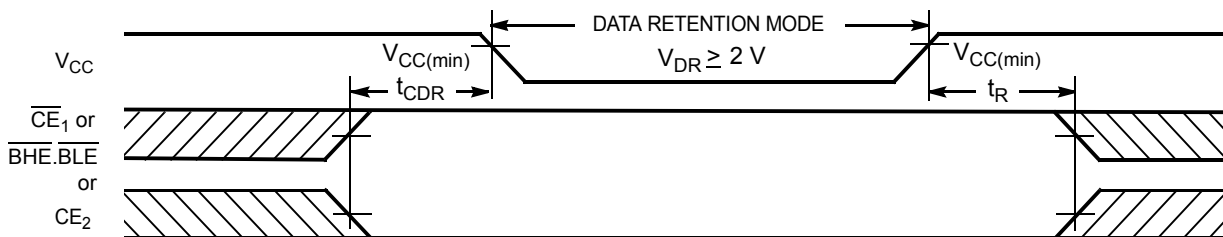
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[11]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2	–	–	V
$I_{CCDR}$ <sup>[12]</sup>	Data Retention Current	$V_{CC} = 2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$				$\mu\text{A}$
		Industrial	–	–	8	
		Automotive	–	–	30	
$t_{CDR}$ <sup>[13]</sup>	Chip Deselect to Data Retention Time		0	–	–	ns
$t_R$ <sup>[14]</sup>	Operation Recovery Time					ns
		CY62157ELL-45	45	–	–	
		CY62157ELL-55	55	–	–	

## Data Retention Waveform

Figure 4. Data Retention Waveform<sup>[15]</sup>



### Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(\text{typ})}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .
12. Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) and byte enables ( $\overline{BHE}$  and  $\overline{BLE}$ ) need to be tied to CMOS levels to meet the  $I_{SB1} / I_{SB2} / I_{CCDR}$  spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ .
15.  $\overline{BHE}.\overline{BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Deselect the chip by either disabling chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

## Switching Characteristics

Over the Operating Range

Parameter <sup>[16, 17]</sup>	Description	45 ns (Industrial)		55 ns (Automotive)		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	45	–	55	–	ns
$t_{AA}$	Address to Data Valid	–	45	–	55	ns
$t_{OHA}$	Data Hold from Address Change	10	–	10	–	ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid	–	45	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid	–	22	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[18]</sup>	5	–	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[18, 19]</sup>	–	18	–	20	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[18]</sup>	10	–	10	–	ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z <sup>[18, 19]</sup>	–	18	–	20	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power Up	0	–	0	–	ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to Power Down	–	45	–	55	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid	–	45	–	55	ns
$t_{LZBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[18]</sup>	10	–	10	–	ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to High Z <sup>[18, 19]</sup>	–	18	–	20	ns
<b>Write Cycle <sup>[20, 21]</sup></b>						
$t_{WC}$	Write Cycle Time	45	–	55	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35	–	40	–	ns
$t_{AW}$	Address Setup to Write End	35	–	40	–	ns
$t_{HA}$	Address Hold from Write End	0	–	0	–	ns
$t_{SA}$	Address Setup to Write Start	0	–	0	–	ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35	–	40	–	ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35	–	40	–	ns
$t_{SD}$	Data Setup to Write End	25	–	25	–	ns
$t_{HD}$	Data Hold from Write End	0	–	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[18, 19]</sup>	–	18	–	20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[18]</sup>	10	–	10	–	ns

### Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [Figure 3 on page 5](#).

17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes [AN13842](#) and [AN66311](#). However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.

18. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device.

19.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.

20. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE_1 = V_{IL}$ ,  $BHE$ ,  $BLE$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

21. The minimum write cycle pulse width for Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .

### Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [22, 23]

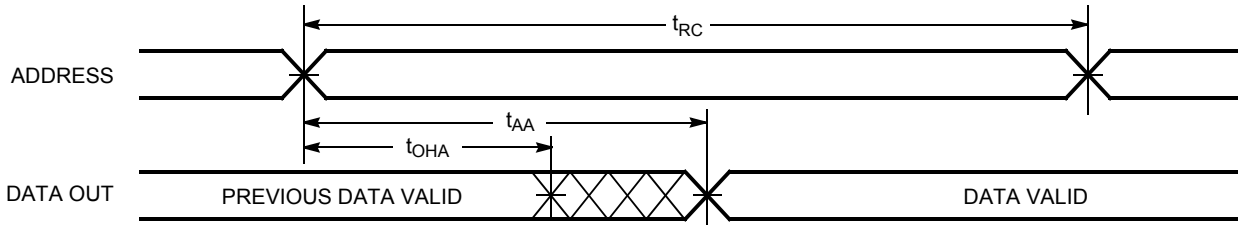
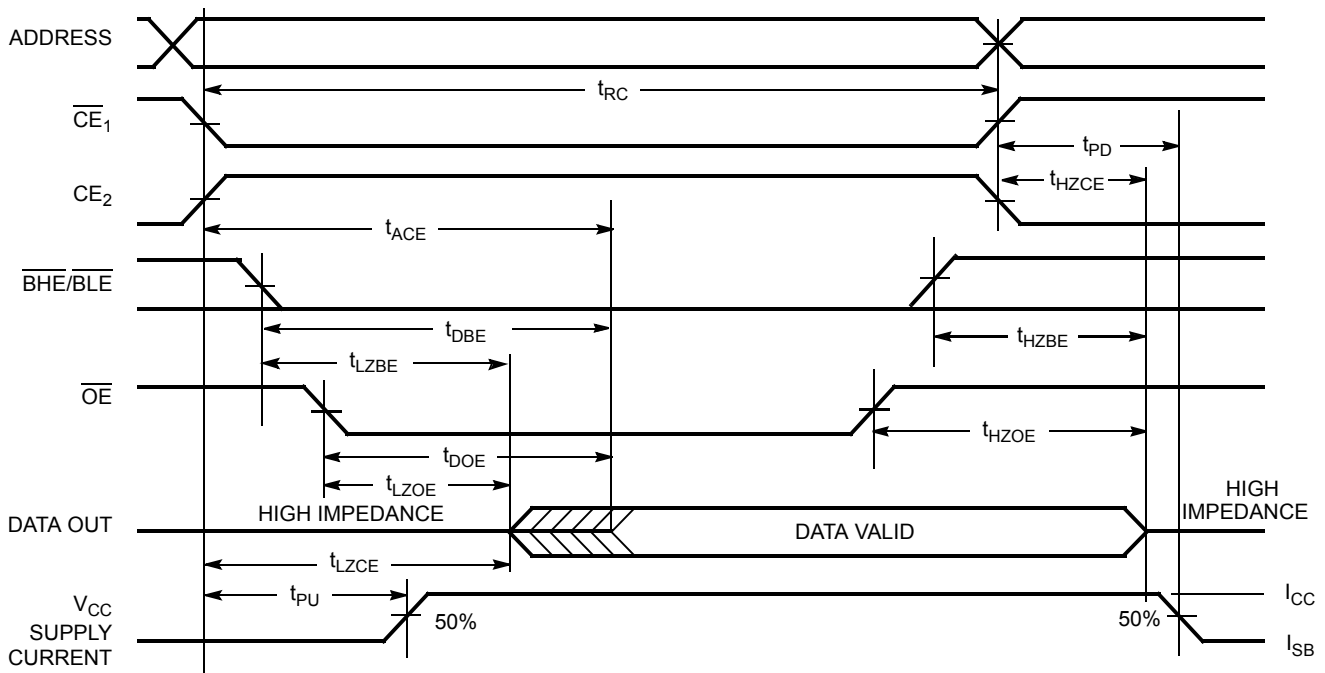


Figure 6. Read Cycle No. 2 ( $\overline{OE}$  Controlled) [23, 24]



**Notes**

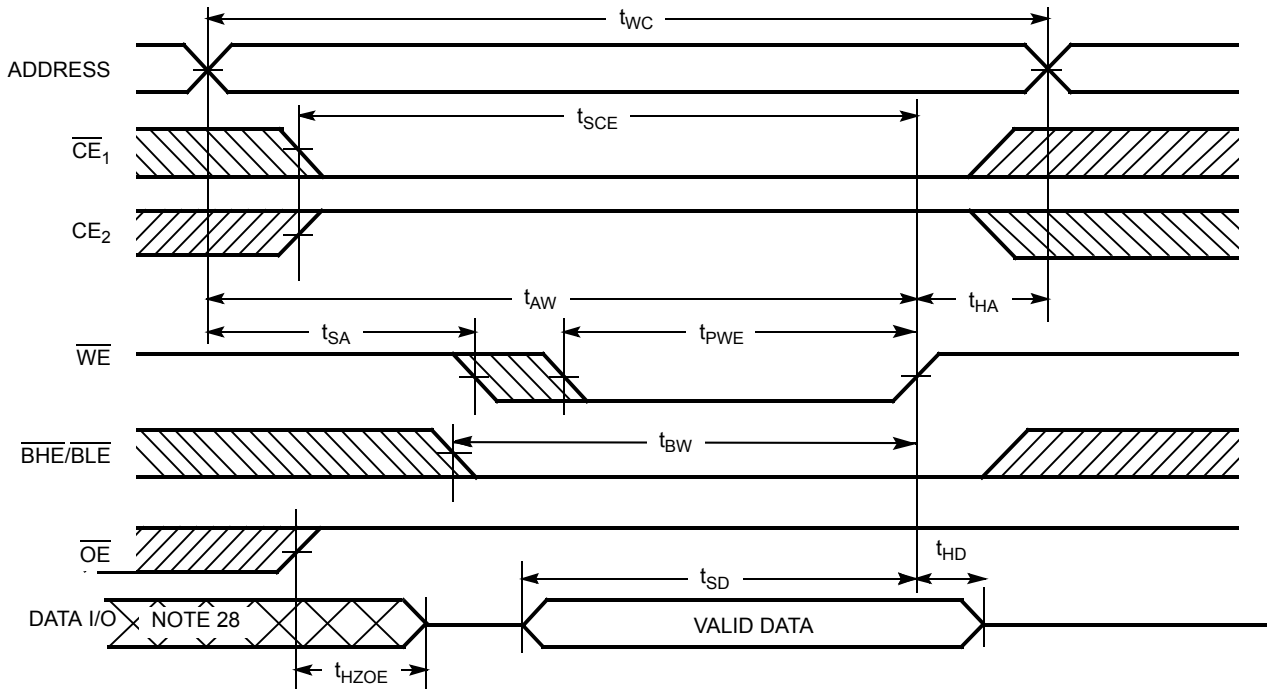
22. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .

23.  $\overline{WE}$  is HIGH for read cycle.

24. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $CE_2$  transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ( $\overline{WE}$  Controlled) [25, 26, 27]



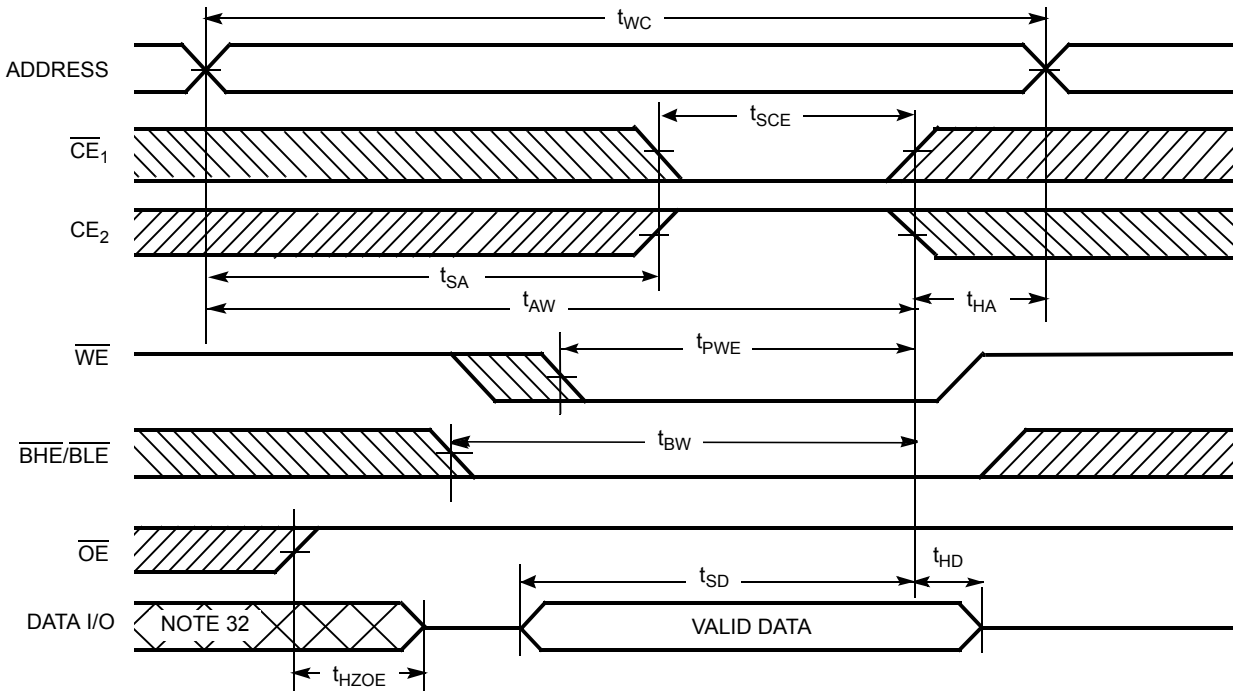
Notes

- 25. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 27. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 28. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [29, 30, 31]



Notes

29. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

30. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

31. If  $\overline{CE}_1$  goes HIGH and  $CE_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.

32. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [33, 34]

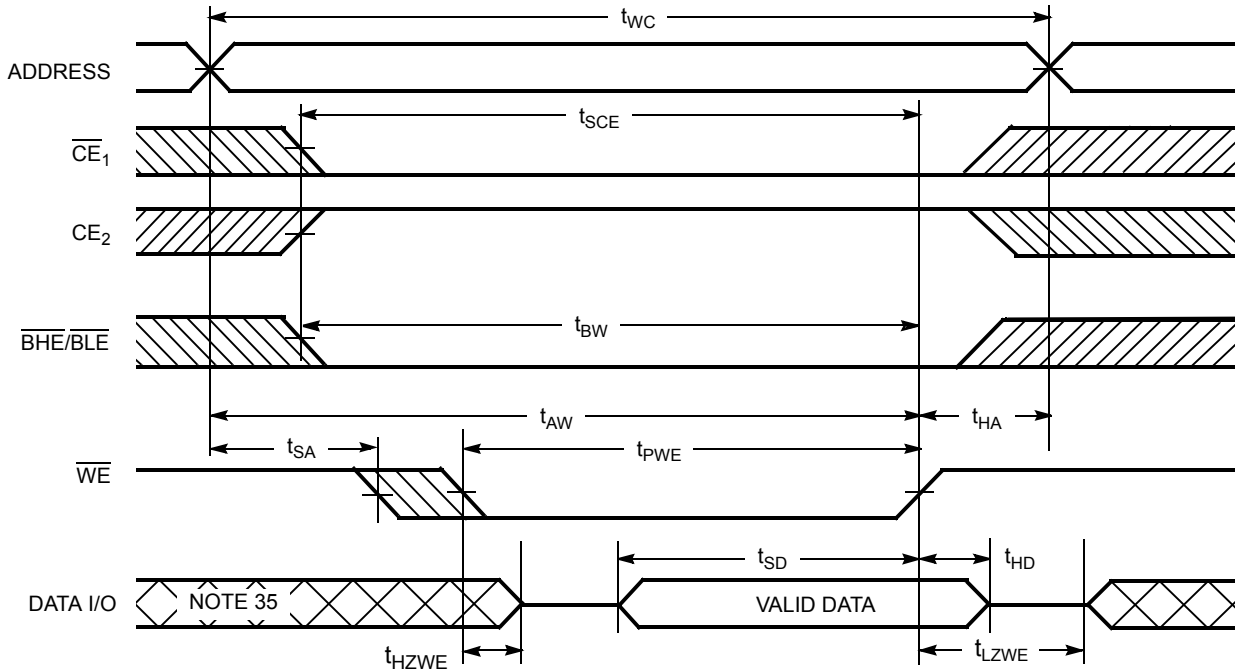
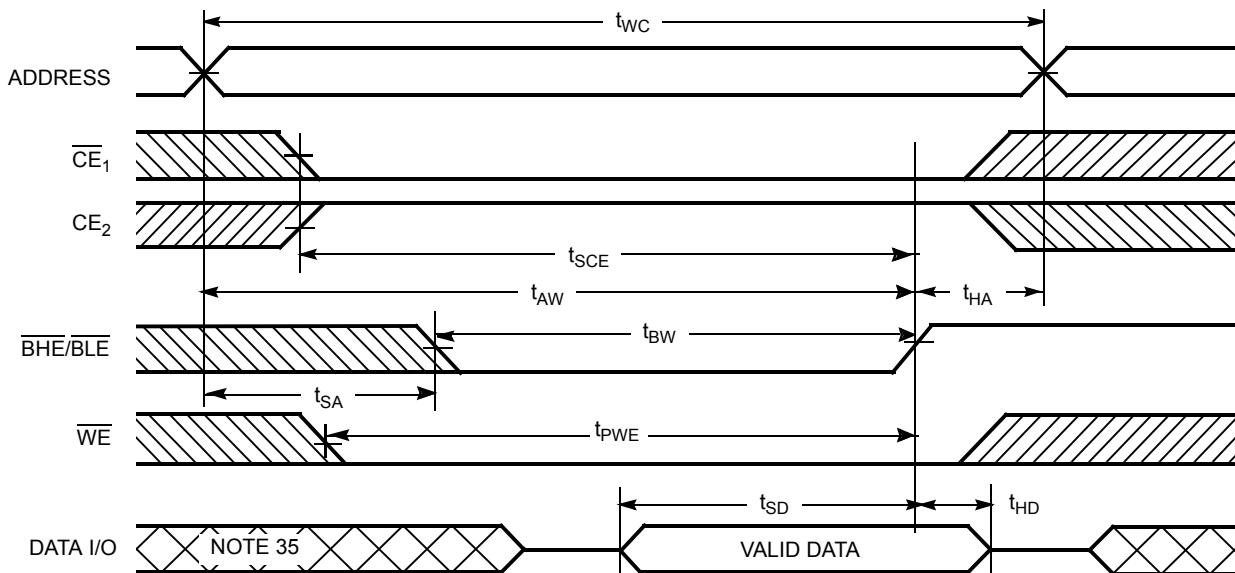


Figure 10. Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW) [33]



Notes

- 33. If  $\overline{CE}_1$  goes HIGH and  $\overline{CE}_2$  goes LOW simultaneously with  $\overline{WE} = V_{IH}$ , the output remains in a high impedance state.
- 34. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .
- 35. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X <sup>[36]</sup>	X	X	X	X	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[36]</sup>	L	X	X	X	X	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
X <sup>[36]</sup>	X <sup>[36]</sup>	X	X	H	H	High Z	Deselect/Power Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data Out ( $I/O_8$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); High Z ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High Z ( $I/O_0$ – $I/O_7$ ); Data In ( $I/O_8$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )

**Note**

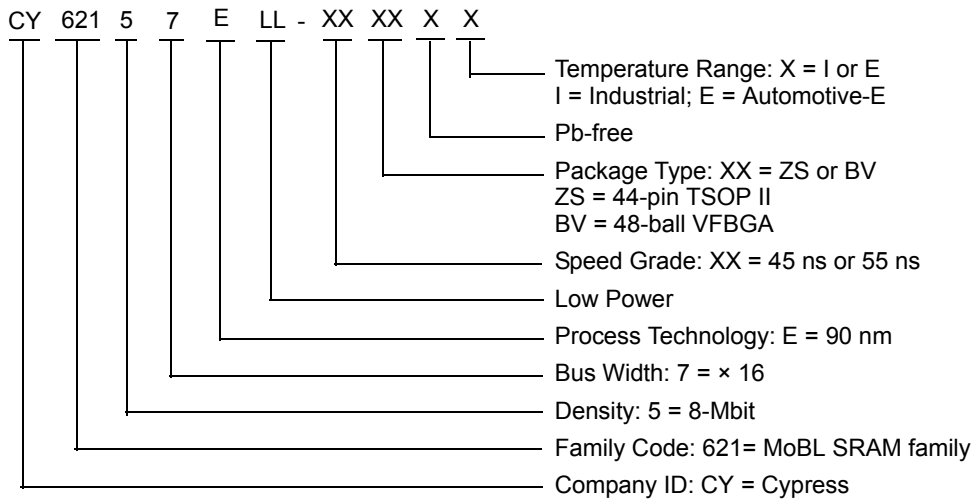
36. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ELL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	Industrial
55	CY62157ELL-55ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-E
	CY62157ELL-55BVXE	51-85150	48-ball VFBGA (Pb-free)	

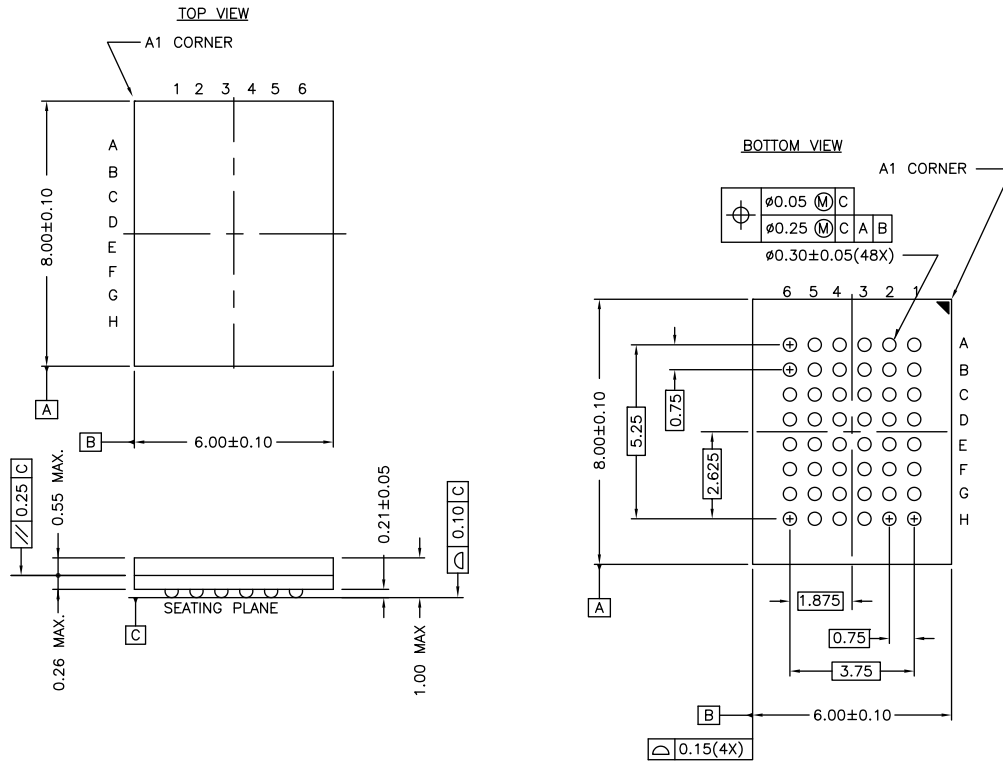
Contact your local Cypress sales representative for availability of these parts.

### Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150

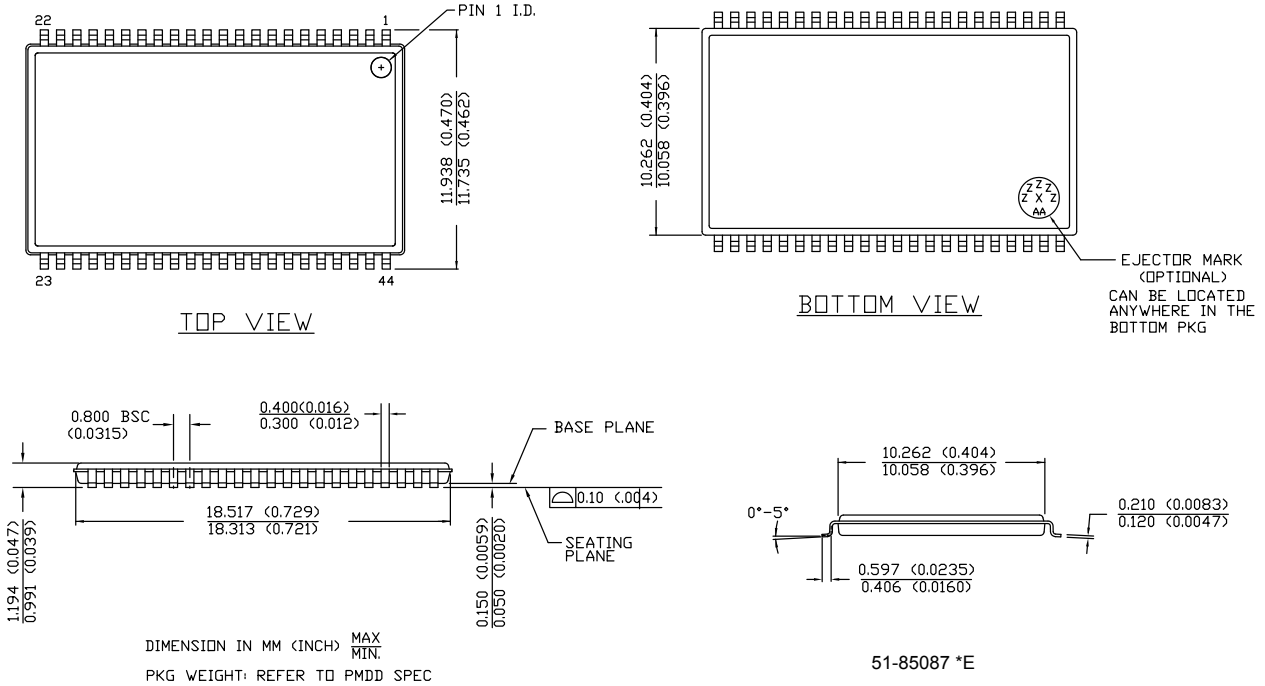


NOTE:  
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD)  
 posted on the Cypress web.

51-85150 \*H

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087



## Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY62157E MoBL <sup>®</sup> , 8-Mbit (512 K × 16) Static RAM				
Document Number: 38-05695				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	291273	See ECN	PCI	New data sheet.
*A	457689	See ECN	NXR	Added Automotive Product Removed Industrial Product Removed 35 ns and 45 ns speed bins Removed "L" bin Updated AC Test Loads table Corrected $t_R$ in Data Retention Characteristics from 100 $\mu$ s to $t_{RC}$ ns Updated the Ordering Information and replaced the Package Name column with Package Diagram
*B	467033	See ECN	NXR	Added Industrial Product (Final Information) Removed 48 ball VFBGA package and its relevant information Changed the $I_{CC(typ)}$ value of Automotive from 2 mA to 1.8 mA for $f = 1$ MHz Changed the $I_{SB2(typ)}$ value of Automotive from 5 $\mu$ A to 1.8 $\mu$ A Modified footnote #4 to include current limit Updated the Ordering Information table
*C	569114	See ECN	VKN	Added 48 ball VFBGA package Updated Logic Block Diagram Added footnote #3 Updated the Ordering Information table
*D	925501	See ECN	VKN	Added footnote #9 related to $I_{SB2}$ and $I_{CCDR}$ Added footnote #14 related AC timing parameters
*E	1045801	See ECN	VKN	Converted Automotive specs from preliminary to final
*F	2934396	06/03/10	VKN	Added footnote #23 related to chip enable Updated <a href="#">Package Diagrams</a> . Updated to new template.
*G	3110053	12/14/2010	PRAS	Changed Table Footnotes to Footnotes. Added <a href="#">Ordering Code Definitions</a> .
*H	3269641	05/30/2011	RAME	Removed the note "For best practice recommendations, please refer to the Cypress application note AN1064, SRAM System Guidelines." and its reference in <a href="#">Functional Description</a> . Updated <a href="#">Electrical Characteristics</a> . Updated <a href="#">Data Retention Characteristics</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*I	4013958	06/05/2013	MEMJ	Updated <a href="#">Functional Description</a> . Updated <a href="#">Electrical Characteristics</a> : Added one more Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA" for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition. Added Note 8 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition " $V_{CC} = 5.5$ V, $I_{OH} = -0.1$ mA". Updated <a href="#">Package Diagrams</a> : spec 51-85150 – Changed revision from *F to *H. spec 51-85087 – Changed revision from *C to *E.
*J	4102449	08/22/2013	VINI	Updated <a href="#">Switching Characteristics</a> : Updated Note 17. Updated to new template.



**Document History Page** (continued)

Document Title: CY62157E MoBL <sup>®</sup> , 8-Mbit (512 K × 16) Static RAM Document Number: 38-05695				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*K	4410589	06/17/2014	VINI	Updated <a href="#">Switching Characteristics</a> : Added Note 21 and referred the same note in "Write Cycle". Updated <a href="#">Switching Waveforms</a> : Added Note 34 and referred the same note in <a href="#">Figure 9</a> . Completing Sunset Review.
*L	4576475	11/21/2014	VINI	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end.
*M	4795615	06/12/2015	VINI	Updated <a href="#">Thermal Resistance</a> : Replaced "two-layer" with "four-layer" in "Test Conditions" column. Changed value of $\theta_{JA}$ corresponding to 44-pin TSOP II package from 77 °C/W to 55.84 °C/W. Changed value of $\theta_{JA}$ corresponding to 48-ball VFBGA package from 72 °C/W to 48.34 °C/W. Changed value of $\theta_{JC}$ corresponding to 44-pin TSOP II package from 13 °C/W to 15.79 °C/W. Changed value of $\theta_{JC}$ corresponding to 48-ball VFBGA package from 8.86 °C/W to 8.78 °C/W. Updated <a href="#">AC Test Loads and Waveforms</a> : Updated <a href="#">Figure 3</a> : Replaced "V" with "V <sub>TH</sub> " in bottom part. Updated to new template. Completing Sunset Review.
*N	5962457	11/09/2017	AESATMP8	Updated logo and Copyright.

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