The P1016 and P1025 processors have an advanced set of features for ease of use. The 256 KB L2 cache offers incremental configuration to partition the cache between the two cores or to configure it as SRAM or stashing memory. The integrated security engine supports the cryptographic algorithms commonly used in IPsec, SSL, 3GPP and other networking and wireless security protocols. The memory controller offers future-proofing against memory technology migration with support for DDR3. It also supports error correction codes, a baseline requirement for any high-reliability system.

These processors integrate a rich set of interfaces, including a multiprotocol SerDes, Gigabit Ethernet, QUICC Engine module, PCI Express® and USB. The three 10/100/1000 Ethernet ports support advanced packet parsing, flow control and quality of service features, as well as IEEE® 1588 time-stamping—all ideal for managing the data path traffic between the LAN and WAN interface. The QUICC Engine module provides UTOPIA-L2, TDM and 10/100 Ethernet interfaces as well as a programmable RISC engine to offload protocol termination from the main CPU cores. Four SerDes lanes can be portioned across two PCI Express ports and two SGMII ports. The PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support. USB or SD/MMC interfaces can be used to support local storage. Multiple memory connection ports are available, including the 16-bit local bus, a USB 2.0 controller, enhanced secure digital host controller (eSDHC) and serial peripheral interface (SPI).

Target Applications

The P1016 and P1025 processors serve in a wide variety of applications. The devices are well suited for various combinations of data plane and control plane workloads in networking and telecom applications. With an available junction temperature range of –40 ºC to +125 ºC, the devices can be used in power-sensitive defense and industrial applications and outdoor environments less protected from the elements. The devices' primary target applications are networking and telecom linecards.

A multiservice router or business gateway requires a combination of high performance and a rich set of peripherals to support the data path throughputs and required system functionality. The P1016 and P1025 devices offer a scalable platform to develop a range of products that can support the same feature set. The QUICC Engine module, as well as integrated 10/100/1000 Ethernet controllers with classification and QoS capabilities, are ideal for managing the data path traffic between the LAN and WAN interface. PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support, TDM for legacy phone interfaces to support voice and the USB or SD/MMC interfaces can be used to support local storage. The integrated security engine can provide encrypted secure communications for remote users with VPN support.

Technical Specifications

- Dual (P1025) or single (P1016 high-performance Power Architecture e500 cores
- 36-bit physical addressing
- Double-precision floating-point support
- 32 KB L1 instruction cache and 32 KB L1 data cache for each core
- 400–667 MHz core clock frequency
- 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- Three 10/100/1000 Mb/s enhanced threespeed Ethernet controllers (eTSECs)
- TCP/IP acceleration and classification capabilities
- IEEE 1588 support
- Lossless flow control
- RGMII, SGMII
- High-speed interfaces (not all available simultaneously)
- Four SerDes to 3.125 GHz multiplexed across controllers
- Two PCI Express controllers
- Two SGMII interfaces
- QUICC Engine module
- UTOPIA-L2
- Up to two 10/100 Ethernet interfaces
- Up to four T1/E1/J1/E3 or DS-3 serial interfaces
- Up to four HDLC interfaces with 128 channels of HDLC
- Up to four BISYNC interfaces
- Up to four UART interfaces
- SPI interfaces
- GPIO
- High-Speed USB controller (USB 2.0)
- Host and device support
- Enhanced host controller interface (EHCI)
- ULPI interface to PHY
- Enhanced secure digital host controller (eSDHC)
- Serial peripheral interface
- Integrated security engine (SEC 3.3)
- Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Snow 3G and FIPS deterministic RNG
- Single-pass encryption/message authentication for common security protocols (e.g., IPsec, SSL, SRTP, WiMAX)
- XOR acceleration
- 32-bit DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- Sixteen general-purpose I/O signals
- Package: 561-pin wirebond power-BGA (TEPBGA1)

For more information, please visit freescale.com/QorIQ

Document Number: QP1025FS REV 4

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

P1016NSE5BFB P1016NSE5DFB P1016NSE5FFB P1016NSN5BFB P1016NSN5DFB P1016NSN5FFB P1016NXE5BFB P1016NXE5DFB P1016NXE5FFB P1016NXN5BFB P1016NXN5DFB P1016NXN5FFB P1025NSE5BFB P1025NSE5DFB P1025NSN5BFB P1025NSN5DFB P1025NXE5BFB P1025NXE5DFB P1025NXN5BFB P1025NXN5DFB