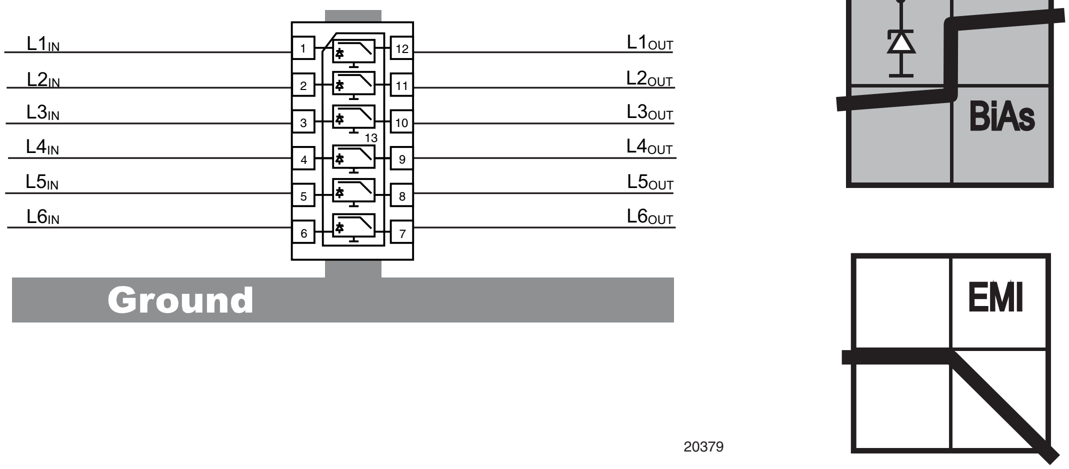
APPLICATION NOTE

With the VEMI65AC-HCI 6 different signal or data lines can be filtered and clamped to ground. Due to the different clamping levels in forward and reverse direction the clamping behaviour is Bidirectional and Asymmetric (BiAs).



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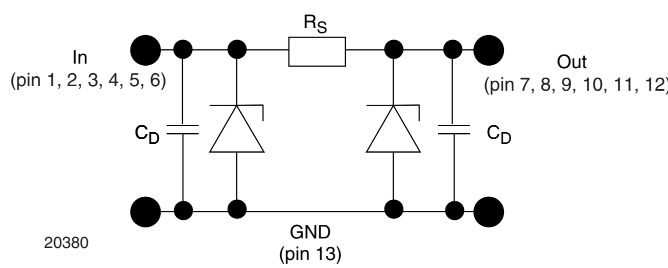
The 6 independent EMI-filter are placed between

pin 1 and pin 12,
pin 2 and pin 11,
pin 3 and pin 10,
pin 4 and pin 9,
pin 5 and pin 8 and
pin 6 and pin 7.

They all are connected to a common ground pin 13 on the backside of the package.

The circuit diagram of one EMI-filter-channel shows two identical Z-diodes at the input to ground and the output to ground. These Z-diodes are characterized by the breakthrough voltage level (V_{BR}) and the diode capacitance (C_D). Below the breakthrough voltage level the Z-diodes can be considered as capacitors. Together with these capacitors and the line resistance R_S between input and output the device works as a low pass filter. Low frequency signals ($f < f_{3dB}$) pass the filter while high frequency signals ($f > f_{3dB}$) will be shorted to ground through the diode capacitances C_D.



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Each filter is symmetrical so that both ports can be used as input or output.

ELECTRICAL CHARACTERISTICS All inputs (pin 1 to pin 6) to ground (pin 13) (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of channels which can be protected	$N_{channel}$	-	-	6	channel
Reverse stand off voltage	Max. reverse working voltage	V_{RWM}	-	-	5	V
Reverse voltage	at I_R = 1 µA	V_R	5	-	-	V
Reverse current	at $V_R = V_{RWM}$	I_R	-	< 0.1	1	µA
Reverse break down voltage	at I_R = 1 mA	V_{BR}	6	-	-	V
Pos. clamping voltage	at I_{PP} = 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	$V_{C\text{-}out}$	-	-	7	V
	at $I_{PP} = I_{PPM}$ = 2 A applied at the input, measured at the output; acc. IEC 61000-4-5	$V_{C\text{-}out}$	-	-	8	V
Neg. clamping voltage	at I_{PP} = - 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	$V_{C\text{-}out}$	-1	-	-	V
	at $I_{PP} = I_{PPM}$ = - 2 A applied at the input, measured at the output; acc. IEC 61000-4-5	$V_{C\text{-}out}$	-1.2	-	-	V
Input capacitance	at V_R = 0 V; f = 1 MHz	C_{IN}	-	20	-	pF
	at V_R = 2.5 V; f = 1 MHz	C_{IN}	-	13	-	pF
ESD-clamping voltage	at ± 10 kV ESD-pulse acc. IEC 61000-4-2	V_{CESD}	-	7.5	-	V
Line resistance	Measured between input and output; I_S = 10 mA	R_S	90	100	110	Ω
Cut-off frequency	V_{IN} = 0 V; measured in a 50 Ω system	f_{3dB}	-	240	-	MHz

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

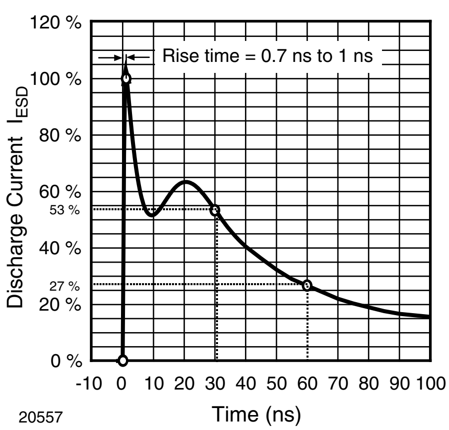


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

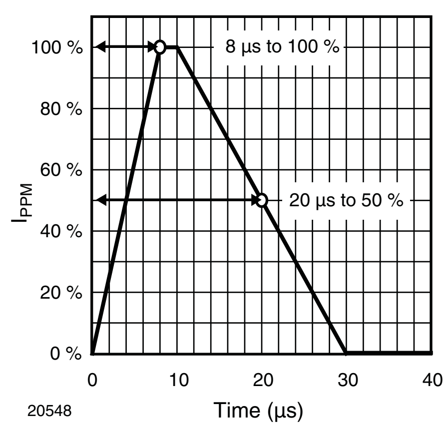


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

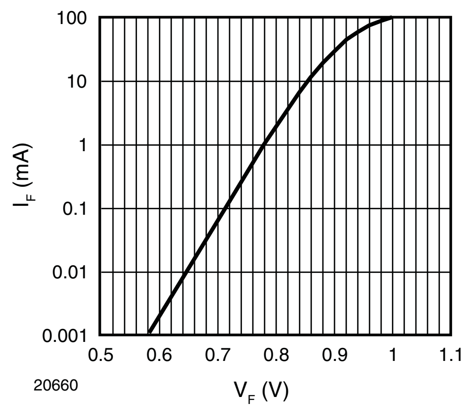


Fig. 3 - Typical Forward Current I_F vs. Forward Voltage V_F

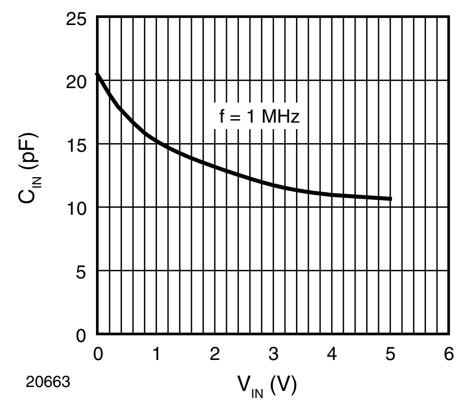


Fig. 6 - Typical Input Capacitance C_{IN} vs. Input Voltage V_{IN}

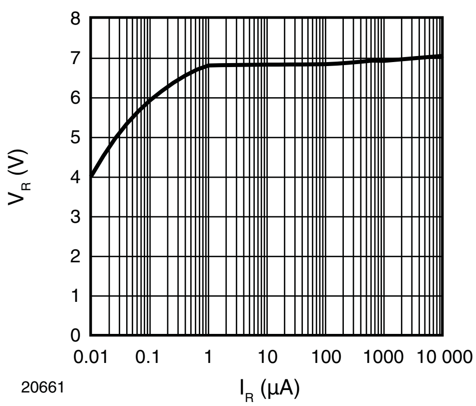


Fig. 4 - Typical Reverse Voltage V_R vs. Reverse Current I_R

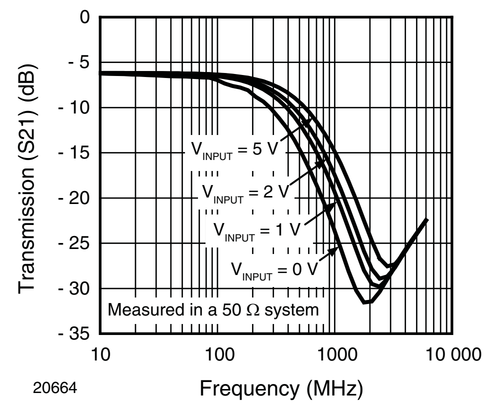


Fig. 7 - Typical Small Signal Transmission (S21) at $Z_O = 50\ \Omega$

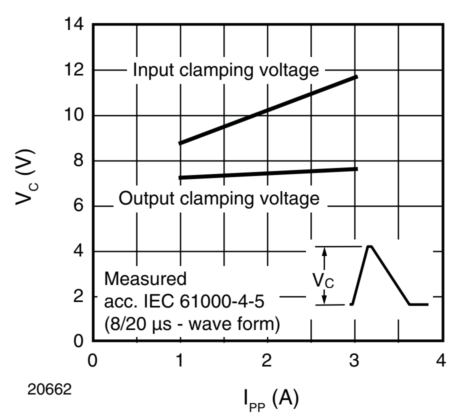
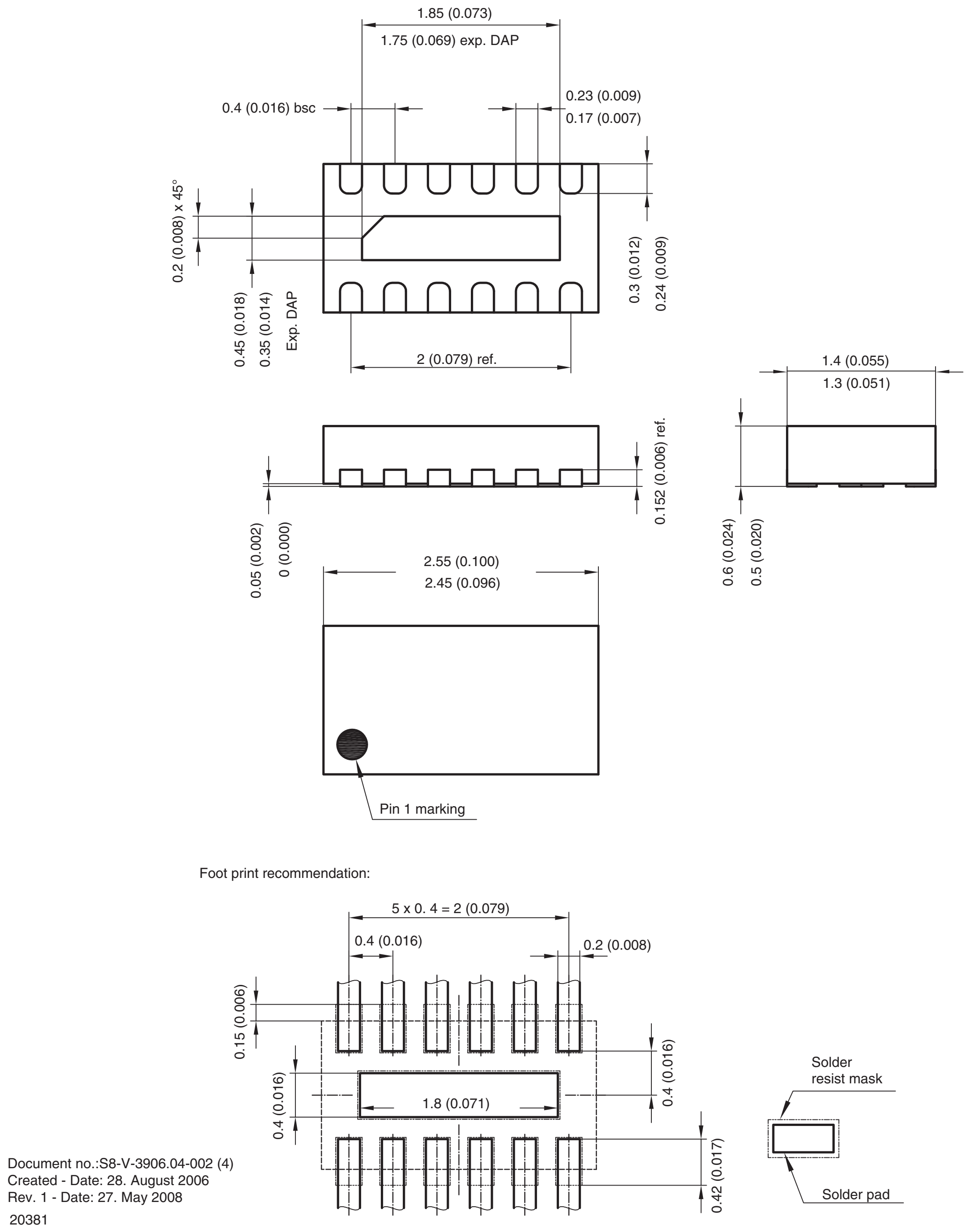


Fig. 5 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

For technical questions, contact: EMIFilter@vishay.com

PACKAGE DIMENSIONS in millimeters (inches): **LLP2513-13L**



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