Logic Block Diagram
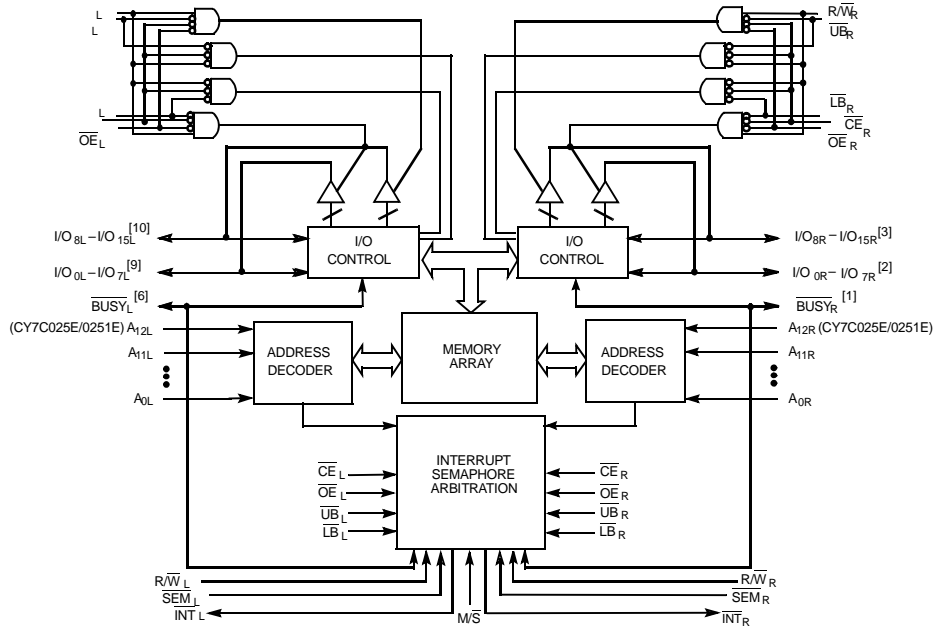

Notes
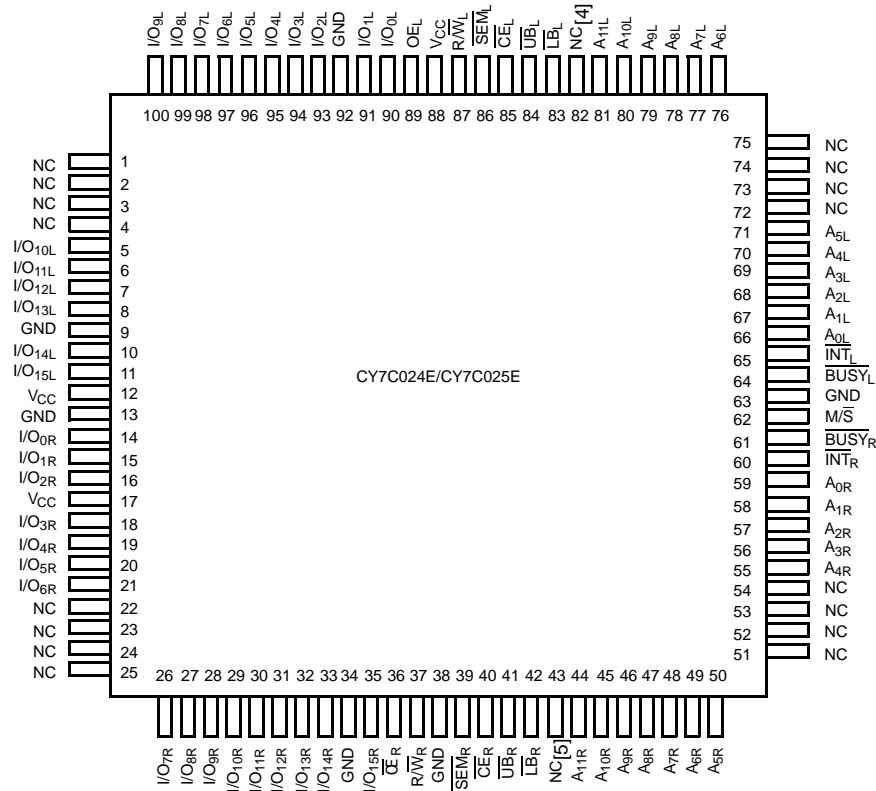1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. $I/O_0 - I/O_8$ on the CY7C0241E/CY7C0251E.
3. $I/O_9 - I/O_{17}$ on the CY7C0241E/CY7C0251E.

Contents

Pin Configurations

Figure 1. 100-Pin TQFP (Top View)

Figure 2. 100-Pin TQFP (Top View)

CY7C0241/CY7C0251E
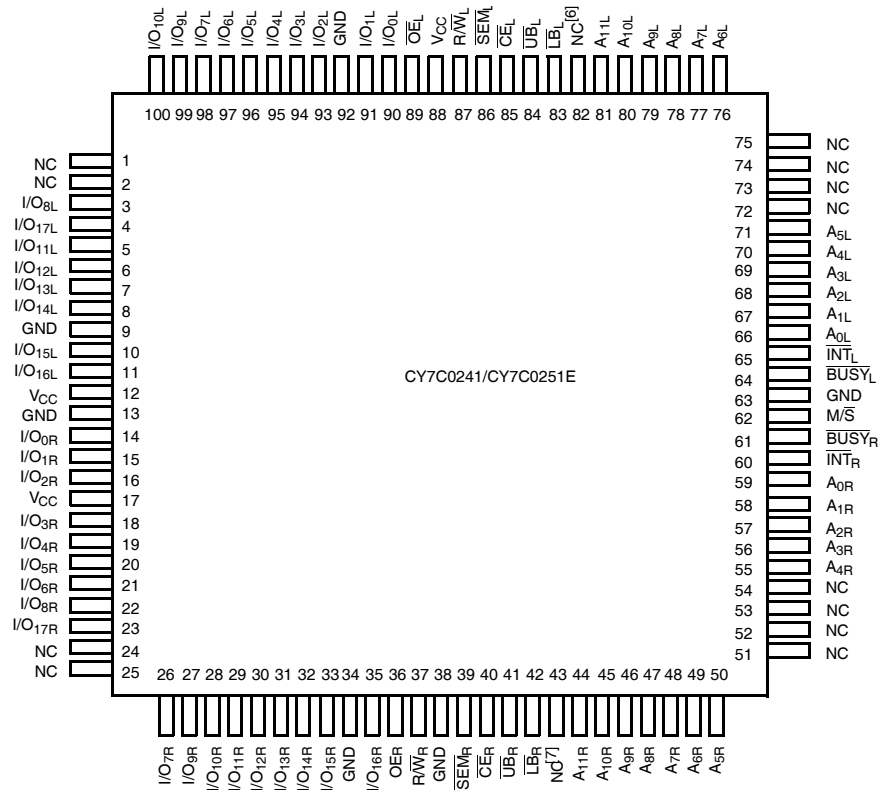
Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
A_{0L}–$A_{11/12L}$	A_{0R}–$A_{11/12R}$	Address
I/O_{0L}–$I/O_{15/17L}$	I/O_{0R}–$I/O_{15/17R}$	Data bus input/output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper byte select
$\overline{LB}_L$	$\overline{LB}_R$	Lower byte select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$[8]	$\overline{BUSY}_R$[8]	Busy flag
M/S		Master or slave select
V_{CC}		Power
GND		Ground

Notes
6. A_{12L} on the CY7C025E/CY7C0251E.
7. $\overline{A_{12R}}$ on the CY7C025E/CY7C0251E.
8. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

Architecture

The CY7C024E/CY7C0241E and CY7C025E/CY7C0251E consist of an array of 4 K words of 16/18 bits each and 8 K words of 16/18 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be used for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the CY7C024E/CY7C0241E and CY7C025E/CY7C0251E can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The CY7C024E/CY7C0241E and CY7C025E/CY7C0251E have an automatic power-down feature controlled by CE. Each port is provided with its own output enable control (OE), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W to guarantee a valid write. A write operation is controlled by either the R/W pin (see Figure 7) or the CE pin (see Figure 8). Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data is available t_{ACE} after CE or t_{DOE} after OE is asserted. If the user of the CY7C024E/CY7C0241E and CY7C025E/CY7C0251E wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin, and OE must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (FFF for the CY7C024E/CY7C0241E, 1FFF for the CY7C025E/CY7C0251E) is the mailbox for the right port and the second-highest memory location (FFE for the CY7C024E/CY7C0241E, 1FFE for the CY7C025E/CY7C0251E) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user-defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the BUSY signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active BUSY to a port prevents that port from reading its own mailbox and thus resetting the interrupt to it.

If your application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in Table 2 on page 8.

Busy

The CY7C024E/CY7C0241E and CY7C025E/CY7C0251E provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within t_{PS} of each other, the busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location, but which one is not predictable. BUSY is asserted t_{BLA} after an address match or t_{BLC} after CE is taken LOW.

Master/Slave

A M/S pin is provided to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled (t_{BLC} or t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/S pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C024E/CY7C0241E and CY7C025E/CY7C0251E provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for tSOP before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting SEM LOW. The SEM pin functions as a chip select for the semaphore latches (CE must remain HIGH during SEM LOW). A0–2 represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O$_0$ is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port immediately owns the semaphore as soon as the left port releases it. Table 3 on page 8 shows sample semaphore operations.

When reading a semaphore, all 16/18 data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Table 1. Non-Contending Read/Write

Inputs						Outputs		Operation
CE	R/W	OE	UB	LB	SEM	I/O$_0$–I/O$_7$[9]	I/O$_8$–I/O$_{15}$[10]	
H	X	X	X	X	H	High Z	High Z	Deselected: power-down
X	X	X	H	H	H	High Z	High Z	Deselected: power-down
L	L	X	L	H	H	High Z	Data in	Write to upper byte only
L	L	X	H	L	H	Data in	High Z	Write to lower byte only
L	L	X	L	L	H	Data in	Data in	Write to both bytes
L	H	L	L	H	H	High Z	Data out	Read upper byte only
L	H	L	H	L	H	Data out	High Z	Read lower byte only
L	H	L	L	L	H	Data out	Data out	Read both bytes
X	X	H	X	X	X	High Z	High Z	Outputs disabled
H	H	L	X	X	L	Data out	Data out	Read data in semaphore flag
X	H	L	H	H	L	Data out	Data out	Read data in semaphore flag
H	⌐_	X	X	X	L	Data in	Data in	Write D$_{IN0}$ into semaphore flag
X	⌐_	X	H	H	L	Data in	Data in	Write D$_{IN0}$ into semaphore flag
L	X	X	L	X	L			Not allowed
L	X	X	X	L	L			Not allowed

Notes
9. I/O$_0$ –I/O$_8$ on the CY7C0241E/CY7C0251E.
10. I/O$_9$ –I/O$_{17}$ on the CY7C0241E/CY7C0251E.

Table 2. Interrupt Operation Example (Assumes $\overline{BUSY}_L=\overline{BUSY}_R=$HIGH)[11]

Function	Left Port					Right Port				
	$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-11L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-11R}	$\overline{INT}_R$
Set right $\overline{INT}_R$ flag	L	L	X	(1)FFF	X	X	X	X	X	L[12]
Reset right $\overline{INT}_R$ flag	X	X	X	X	X	X	L	L	(1)FFF	H[13]
Set left $\overline{INT}_L$ flag	X	X	X	X	L[13]	L	L	X	(1)FFE	X
Reset left $\overline{INT}_L$ flag	X	L	L	(1)FFE	H[12]	X	X	X	X	X

Table 3. Semaphore Operation Example

Function	$I/O_0-I/O_{15/17}$ Left	$I/O_0-I/O_{15/17}$ Right	Status
No action	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore.
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore-free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore-free

Notes
11. A_{0L-12L} and A_{0R-12R}, 1FFF/1FFE for the CY7C025E/CY7C0251E.
12. If $\overline{BUSY}_L=$L, then no change.
13. $\overline{BUSY}_R=$L, then no change.lf

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.[14]

Storage temperature .... –65 °C to +150 °C

Ambient temperature with
power applied .... –55 °C to +125 °C

Supply voltage to ground potential ....–0.3 V to +7.0 V

DC voltage applied to outputs
in high Z state ....–0.5 V to +7.0 V

DC input voltage[15] ....–0.5 V to +7.0 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage.. > 2001 V
(per MIL-STD-883, Method 3015)

Latch-up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		–15 Min	–15 Typ	–15 Max	–25 Min	–25 Typ	–25 Max	–55 Min	–55 Typ	–55 Max	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 4.0 mA		–	–	0.4	–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage			2.2	–		2.2	–		2.2	–		V
V_{IL}	Input LOW voltage			–0.7	–	0.8	–0.7	–	0.8	–0.7	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–10	–	+10	–10	–	+10	–10	–	+10	μA
I_{OZ}	Output leakage current	Output disabled, GND ≤ V_O ≤ V_{CC}		–10	–	+10	–10	–	+10	–10	–	+10	μA
I_{CC}	Operating current	V_{CC} = Max, I_{OUT} = 0 mA, Outputs Disabled	Commercial	–	190	285	–	170	250	–	150	230	mA
			Industrial	–	215	305	–	180	290	–	180	290	
I_{SB1}	Standby current (both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[16]	Commercial	–	50	70	–	40	60	–	20	50	mA
			Industrial	–	65	95	–	55	80	–	55	80	
I_{SB2}	Standby current (one port TTL level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[16]	Commercial	–	120	180	–	100	150	–	75	135	mA
			Industrial	–	135	205	–	120	175	–	120	175	
I_{SB3}	Standby current (both ports CMOS levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0[16]	Commercial	–	0.05	0.5	–	0.05	0.50	–	0.05	0.50	mA
			Industrial	–	0.05	0.5	–	0.05	0.50	–	0.05	0.50	
I_{SB4}	Standby current (both ports CMOS levels)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, Active Port Outputs, f = f_{MAX}[16]	Commercial	–	110	160	–	90	130	–	70	120	mA
			Industrial	–	125	175	–	110	150	–	110	150	

Capacitance

Parameter[17]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

Notes
14. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
15. Pulse width < 20 ns.
16. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
17. Tested initially and after any design or process changes that may affect these parameters.

Figure 3. AC Test Loads and Waveforms

(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 3)

Load (Load 2)

ALL INPUT PULSES
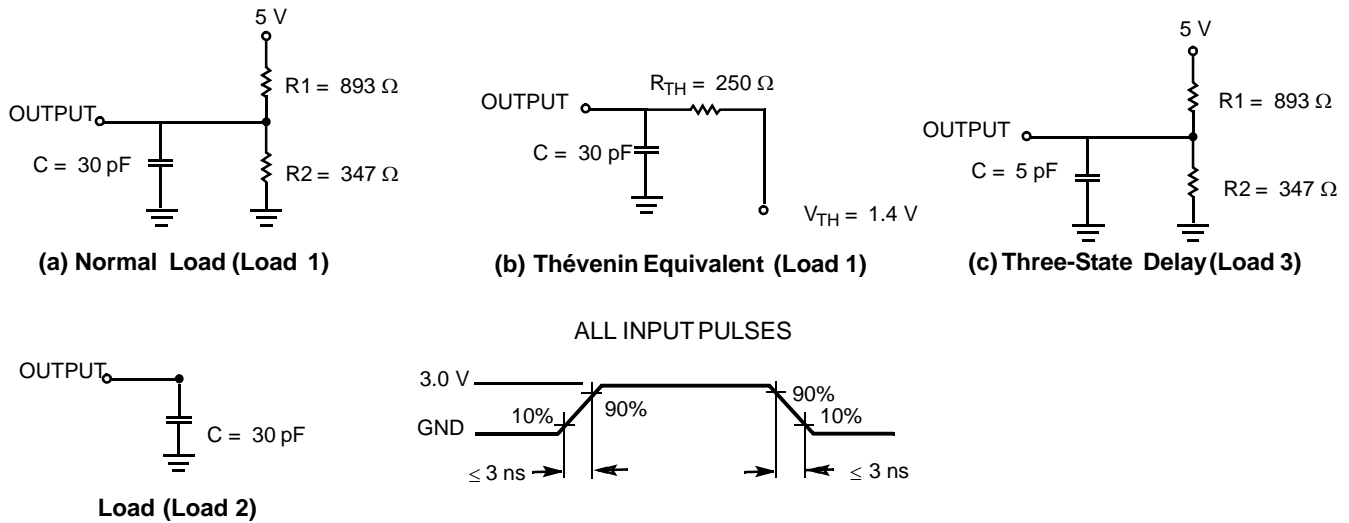
Switching Characteristics Over the Operating Range [18]

Parameter	Description	−15		−25		−55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	15	–	25	–	55	–	ns
t_{AA}	Address to data valid	–	15	–	25	–	55	ns
t_{OHA}	Output hold from address change	3	–	3	–	3	–	ns
t_{ACE}[19]	$\overline{CE}$ LOW to data valid	–	15	–	25	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	–	13	–	25	ns
t_{LZOE}[20, 21, 22]	$\overline{OE}$ low to low Z	3	–	3	–	3	–	ns
t_{HZOE}[20, 21, 22]	$\overline{OE}$ HIGH to high Z	–	10	–	15	–	25	ns
t_{LZCE}[20, 21, 22]	$\overline{CE}$ LOW to low Z	3	–	3	–	3	–	ns
t_{HZCE}[20, 21, 22]	$\overline{CE}$ HIGH to High Z	–	10	–	15	–	25	ns
t_{PU}[22]	$\overline{CE}$ LOW to power-up	0	–	0	–	0	–	ns
t_{PD}[22]	$\overline{CE}$ HIGH to power-down	–	15	–	25	–	55	ns
t_{ABE}[19]	Byte enable access time	–	15	–	25	–	55	ns
Write Cycle								
t_{WC}	Write cycle time	15	–	25	–	55	–	ns
t_{SCE}[19]	$\overline{CE}$ LOW to write end	12	–	20	–	35	–	ns

Notes
18. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{Ol}/I_{OH} and 30 pF load capacitance.
19. To access RAM, $\overline{CE}$=L, $\overline{UB}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire t_{SCE} time.
20. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
21. Test conditions used are Load 3.
22. This parameter is guaranteed but not tested.

Switching Characteristics Over the Operating Range (continued)[18]

Parameter	Description	−15 Min	−15 Max	−25 Min	−25 Max	−55 Min	−55 Max	Unit
t_{AW}	Address setup to write end	12	–	20	–	35	–	ns
t_{HA}	Address hold from write end	0	–	0	–	0	–	ns
t_{SA}[23]	Address setup to write start	0	–	0	–	0	–	ns
t_{PWE}	Write pulse width	12	–	20	–	35	–	ns
t_{SD}	Data setup to write end	10	–	15	–	20	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{HZWE}[24, 25]	R/$\overline{W}$ LOW to high Z	–	10	–	15	–	25	ns
t_{LZWE}[24, 25]	R/$\overline{W}$ HIGH to low Z	3	–	3	–	3	–	ns
t_{WDD}[26]	Write pulse to data delay	–	30	–	50	–	70	ns
t_{DDD}[26]	Write data valid to read data valid	–	25	–	35	–	45	ns
Busy Timing[27]								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match	–	15	–	20	–	45	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch	–	15	–	20	–	40	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	15	–	20	–	40	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	15	–	20	–	35	ns
t_{PS}	Port Setup for Priority	5	–	5	–	5	–	ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0	–	0	–	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	13	–	20	–	40	–	ns
t_{BDD}[28]	$\overline{BUSY}$ HIGH to Data Valid	–	Note 28		Note 28		Note 28	ns
Interrupt Timing[27]								
t_{INS}	$\overline{INT}$ Set Time	–	15	–	20	–	30	ns
t_{INR}	$\overline{INT}$ Reset Time	–	15	–	20	–	30	ns
Semaphore Timing								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	–	12	–	20	–	ns
t_{SWRD}	SEM Flag Write to Read Time	5	–	10	–	15	–	ns
t_{SPS}	SEM Flag Contention Window	5	–	10	–	15	–	ns
t_{SAA}	SEM Address Access Time	–	15		25	–	55	ns

Notes
23. To access RAM, $\overline{CE}$=L, $\overline{UB}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire t_{SCE} time.
24. Test conditions used are Load 3.
25. This parameter is guaranteed but not tested.
26. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 11 on page 16.
27. Test conditions used are Load 2.
28. t_{BDD} is a calculated parameter and is the greater of t_{WDD}− t_{PWE} (actual) or t_{DDD}− t_{SD} (actual).

Data Retention Mode

The CY7C024E/CY7C0241E is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to $V_{CC} - 0.2$ V.

2. $\overline{CE}$ must be kept between $V_{CC} - 0.2$ V and 70% of V_{CC} during the power up and power down transitions.

3. The RAM can begin operation $> t_{RC}$ after V_{CC} reaches the minimum operating voltage (4.5 V).

Data Retention Timing
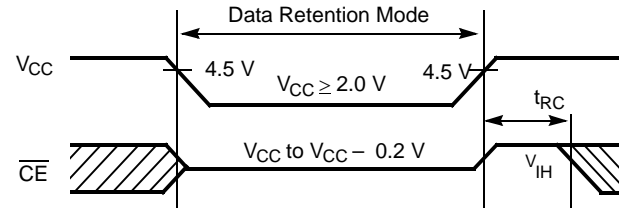
Parameter	Test Conditions[29]	Max	Unit
ICC$_{DR1}$	At VCC$_{DR}$ = 2 V	1.5	mA

Note
29. $\overline{CE} = V_{CC}$, V_{in} = GND to V_{CC}, $T_A = 25°C$. This parameter is guaranteed but not tested.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Either Port Address Access)[30, 31, 32]
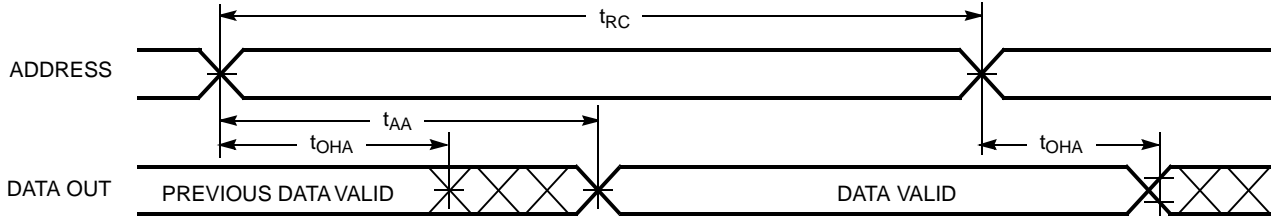
Figure 5. Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[30, 33, 34]
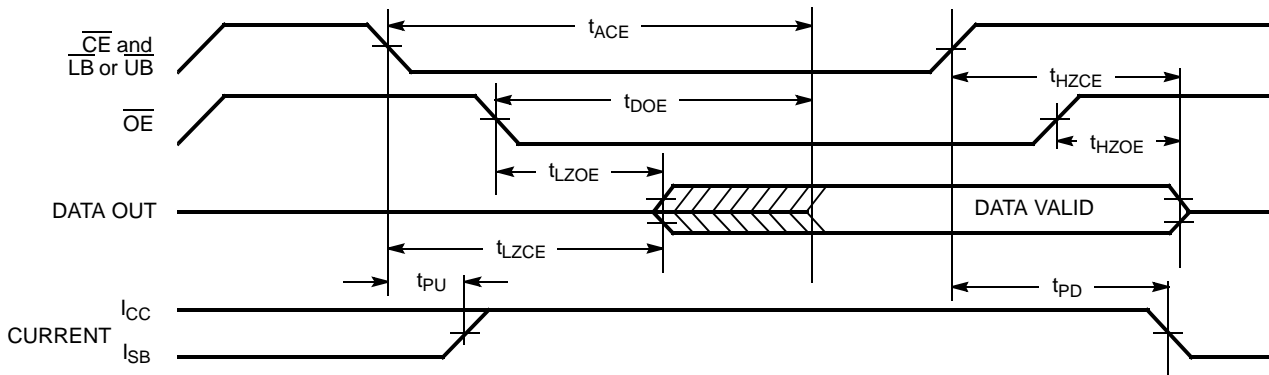
Figure 6. Read Cycle No. 3 (Either Port)[30, 32, 33, 33, 34]
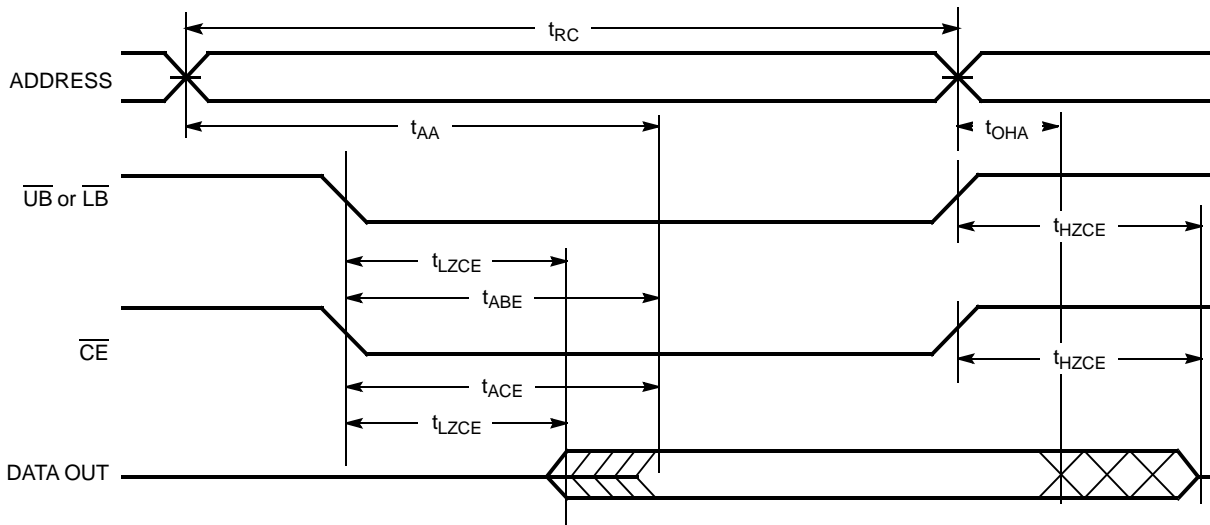
Notes
30. R/$\overline{W}$ is HIGH for read cycles.
31. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
32. $\overline{OE}$ = V_{IL}.
33. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
34. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[35, 36, 37, 38]
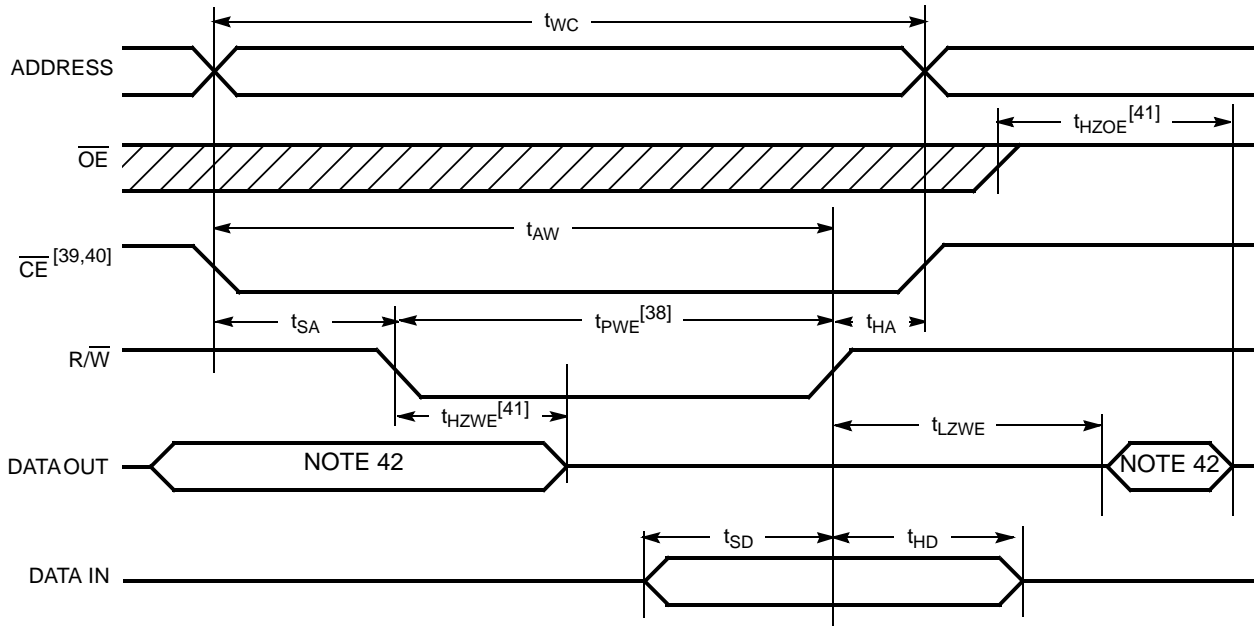
Figure 8. Write Cycle No. 2: $\overline{CE}$ Controlled Timing[35, 36, 37, 43]
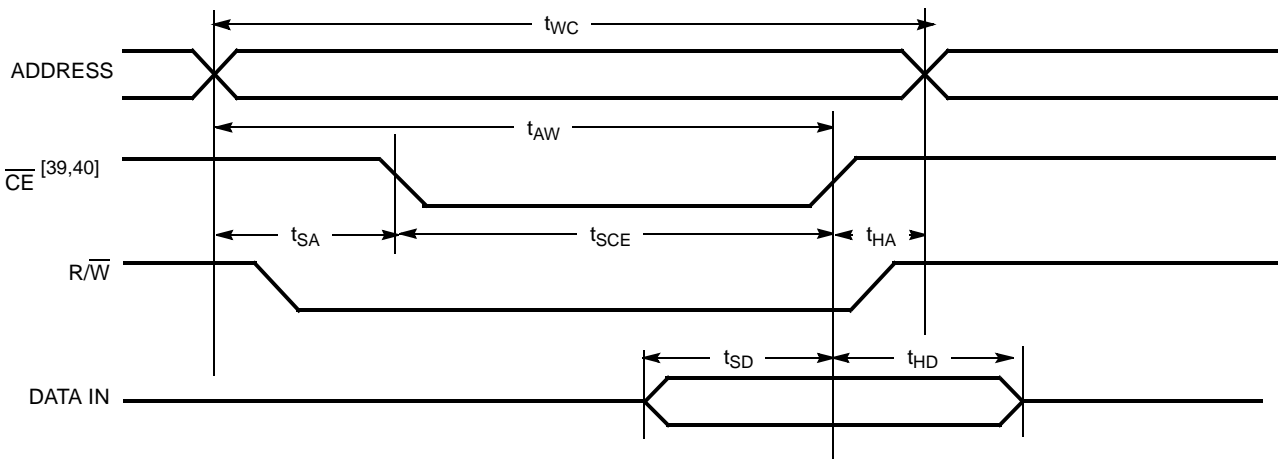
Notes
35. R/$\overline{W}$ must be HIGH during all address transitions.
36. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
37. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
38. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
39. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
40. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
   To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
41. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
42. During this period, the I/O pins are in the output state, and input signals must not be applied.
43. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high impedance state.

Switching Waveforms (continued)

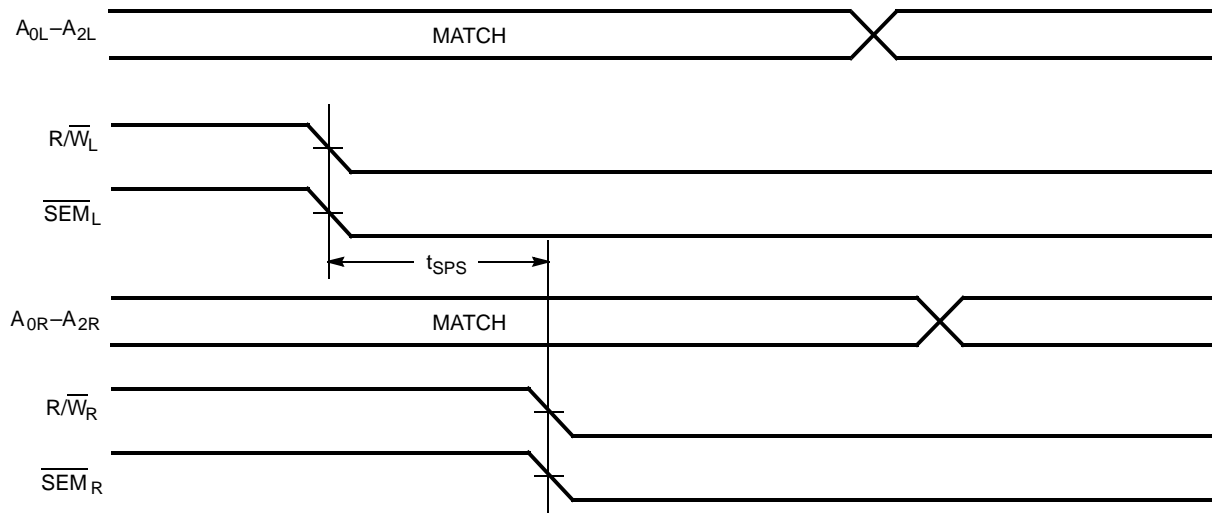**Figure 9. Semaphore Read After Write Timing, Either Side**[44]
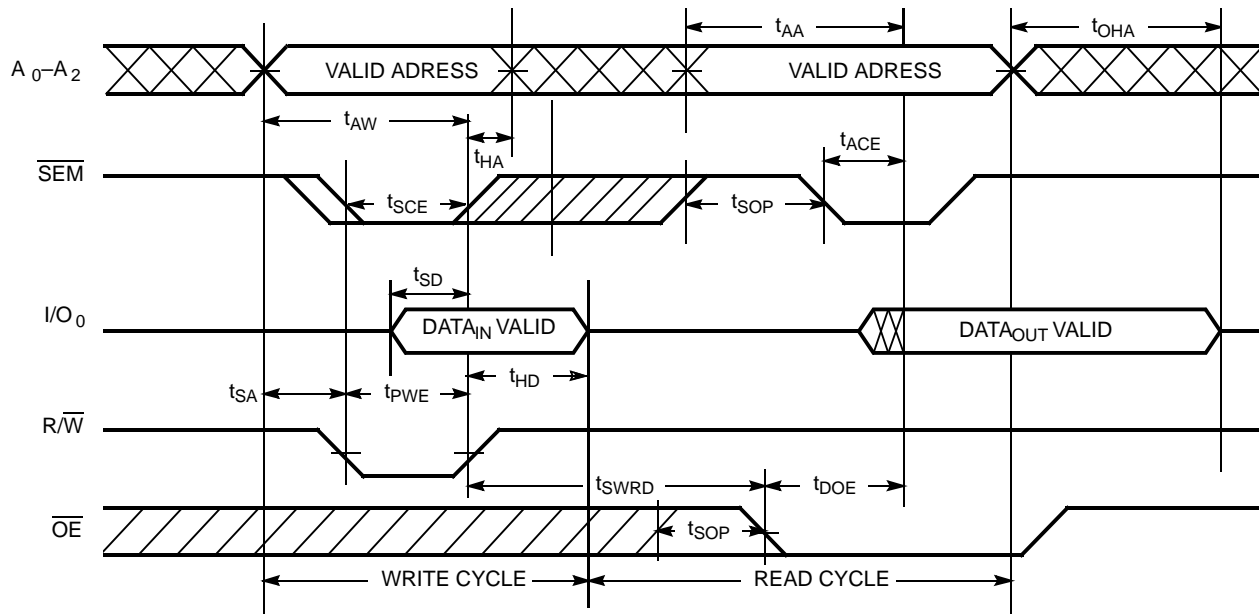
Figure 10. Timing Diagram of Semaphore Contention[45, 46, 47]

Notes
44. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
45. I/O_{0R} = I/O_{0L} = LOW (request semaphore); $\overline{CE}_R$ = $\overline{CE}_L$ = HIGH.
46. Semaphores are reset (available to both ports) at cycle start.
47. If t_{SPS} is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

Switching Waveforms (continued)

Figure 11. Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[48]
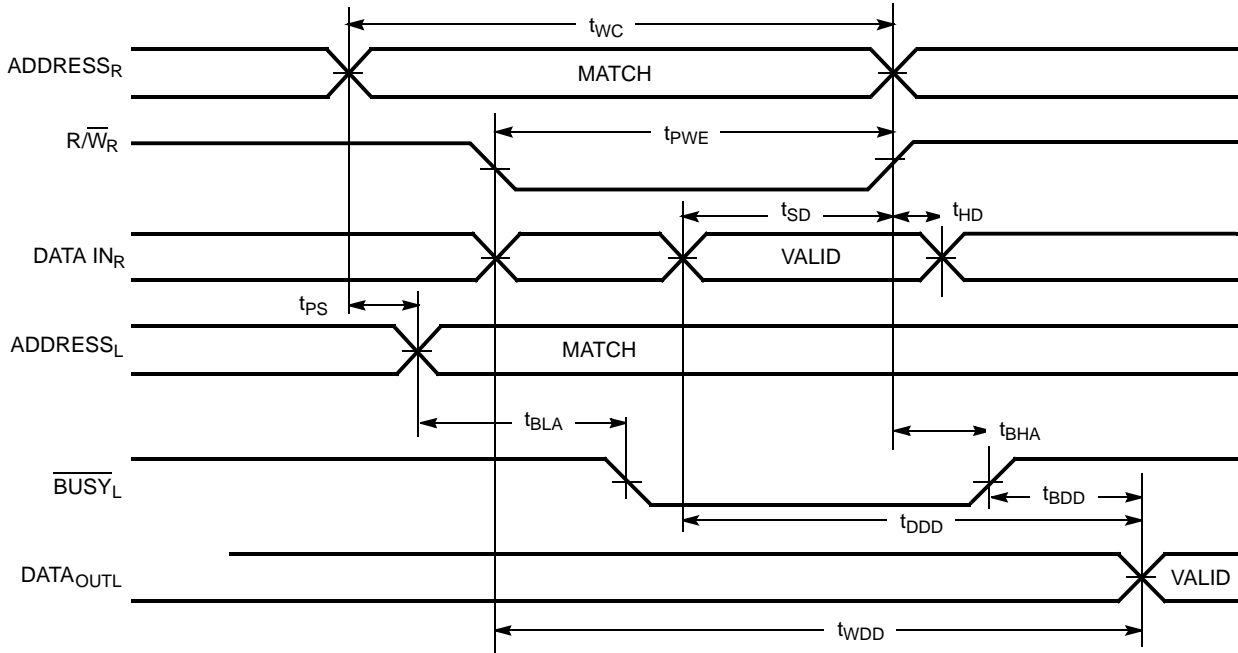
Figure 12. Write Timing with Busy Input (M/$\overline{S}$=LOW)
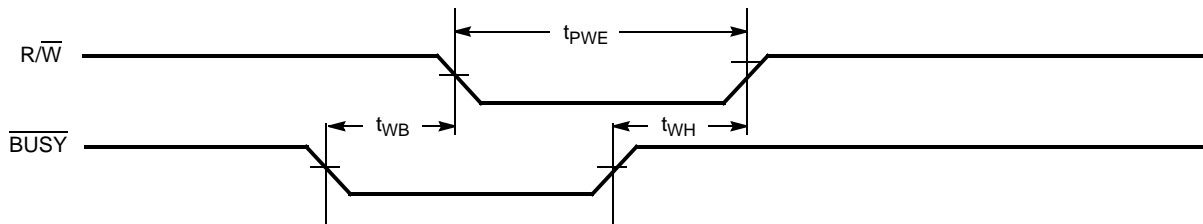
Note
48. $\overline{CE}_L = \overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 13. Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)[49]

$\overline{CE}_L$ Valid First:

CE_R Valid First:
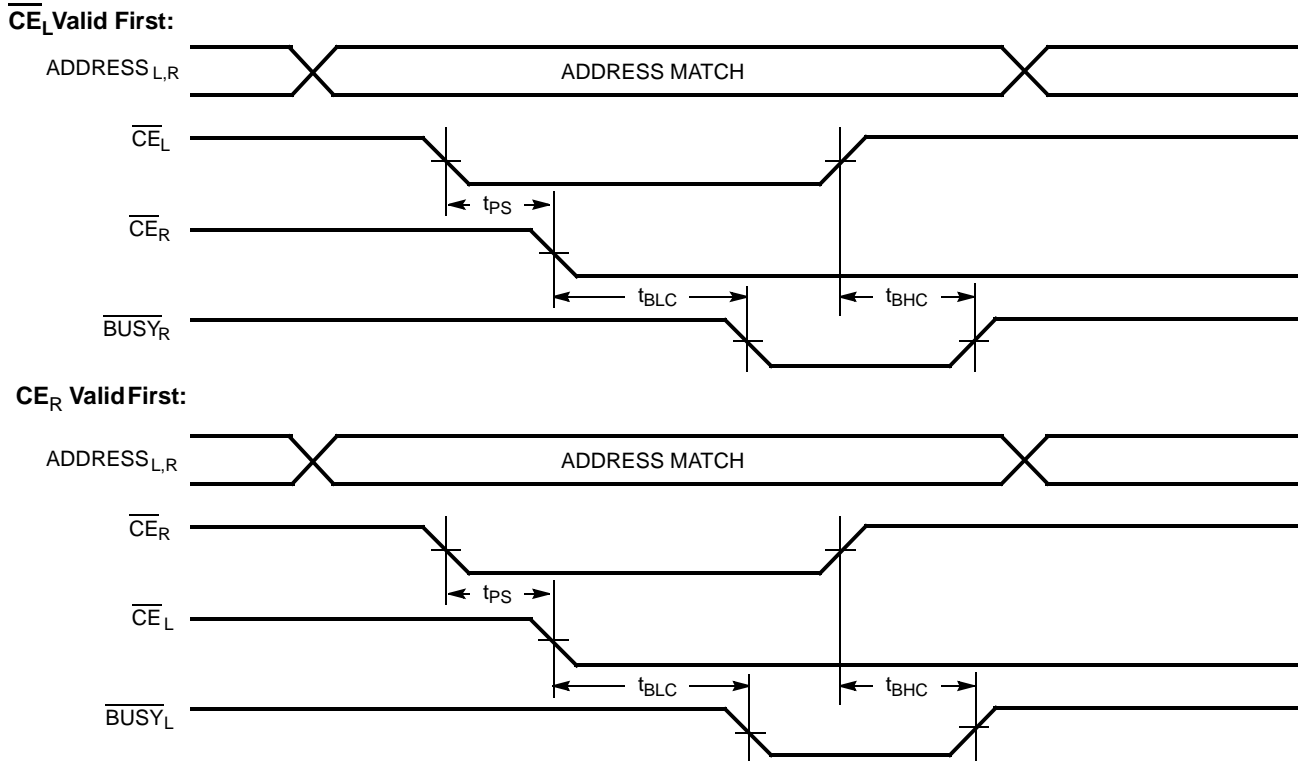
Figure 14. Busy Timing Diagram No.2 (Address Arbitration)[49]

Left Address Valid First:

Right Address Valid First:
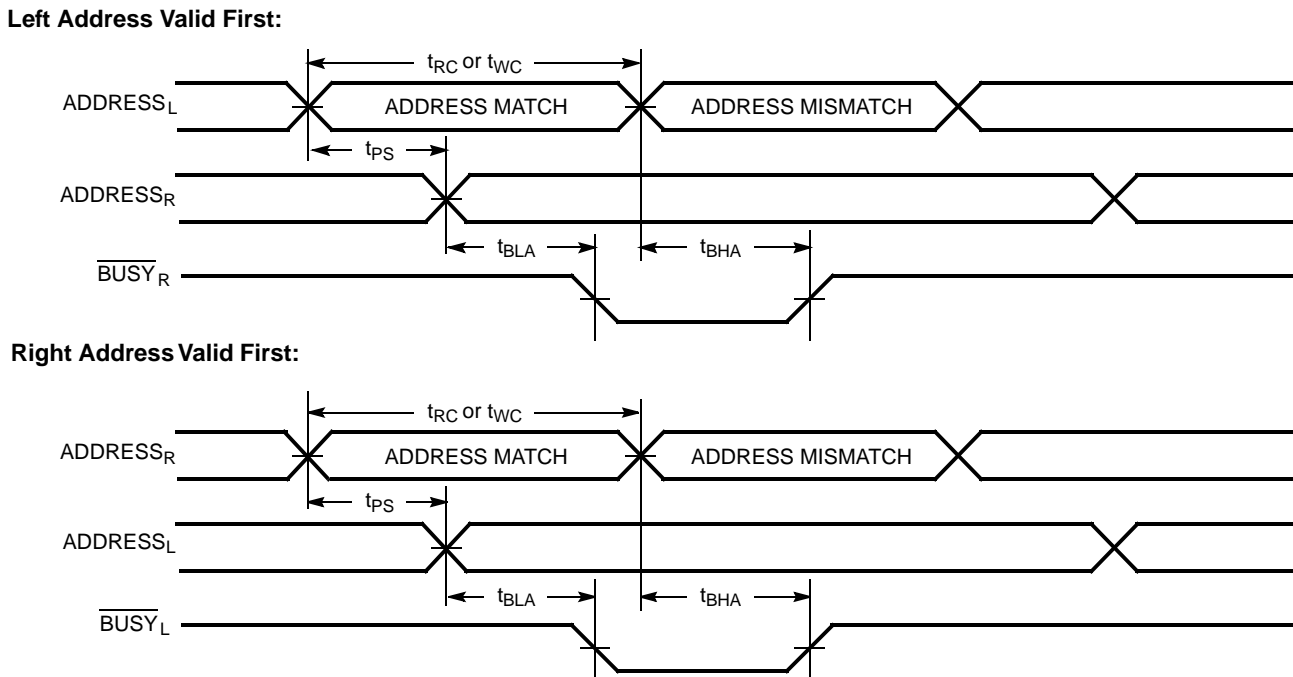
Note
49. If t_{PS} is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ is asserted.

Switching Waveforms (continued)

Figure 15. Interrupt Timing Diagrams
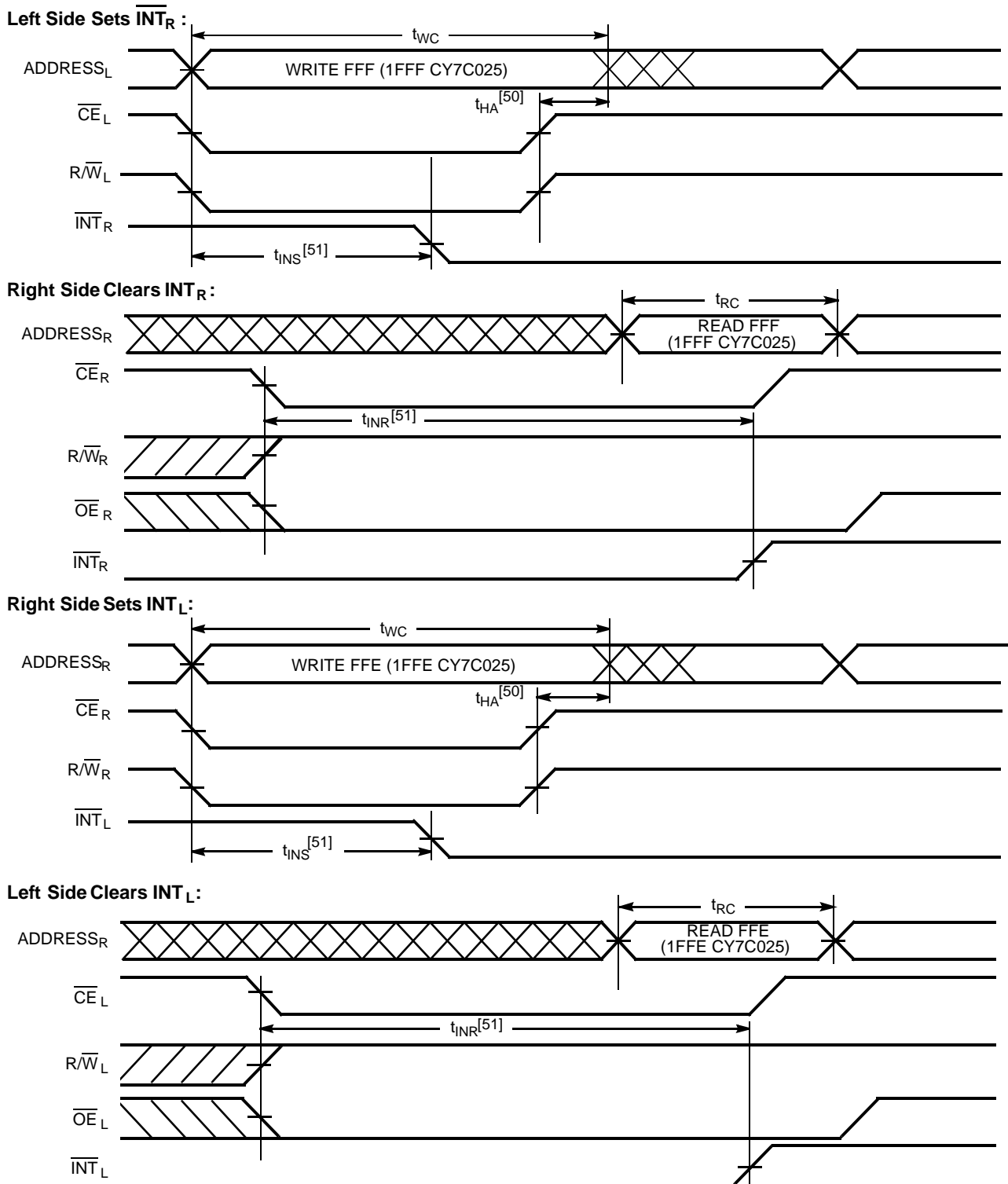
Notes
50. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
51. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

Ordering Information (4K x16 Dual-Port SRAM)

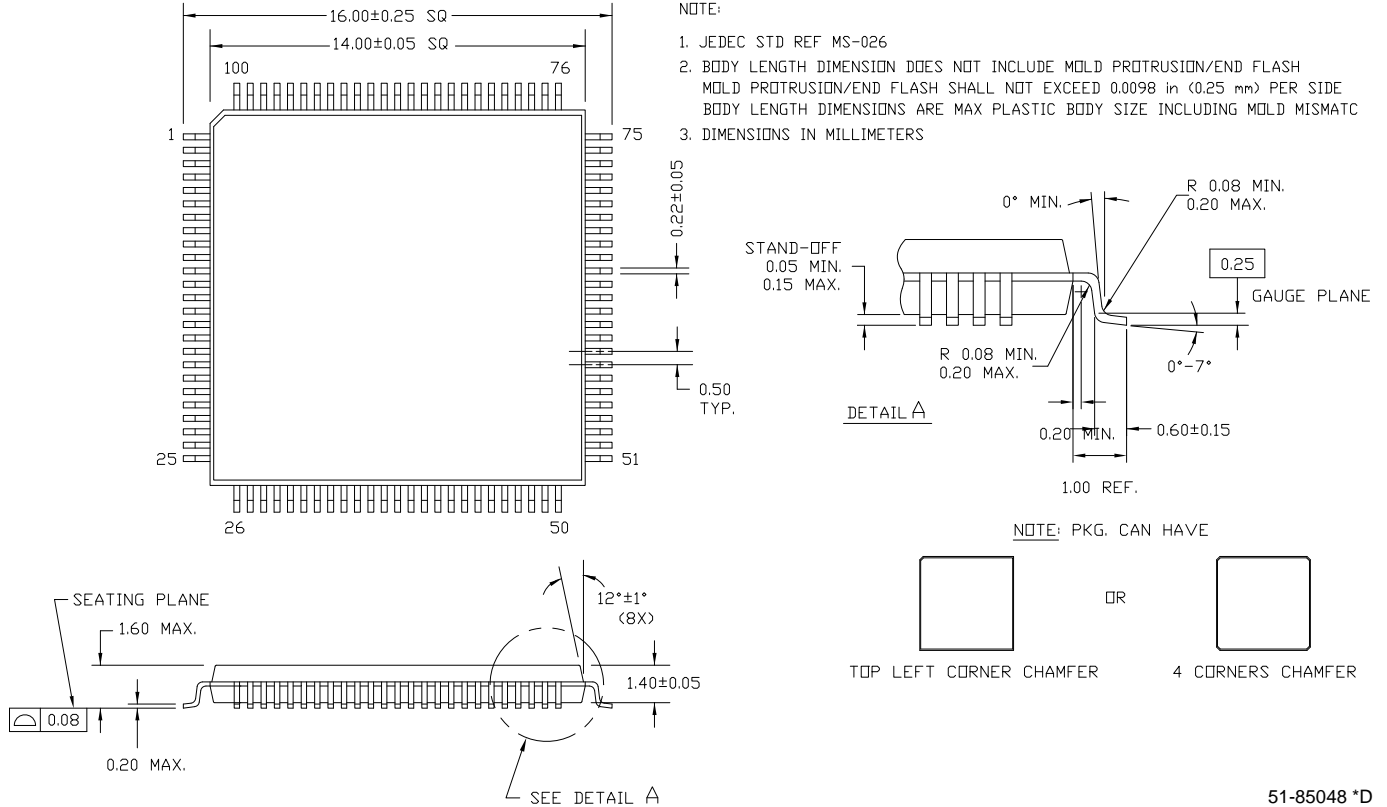| Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C024E-15AXC	A100	100-Pin Pb-free TQFP	Commercial
25	CY7C024E-25AXC	A100	100-Pin Pb-free TQFP	Commercial
	CY7C024E-25AXI	A100	100-Pin Pb-free TQFP	Industrial
55	CY7C024E-55AXC	A100	100-Pin Pb-free TQFP	Commercial

Ordering Information (8K x 16 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C025E-25AXC	A100	100-Pin Pb-free TQFP	Commercial
	CY7C025E-25AXI	A100	100-Pin Pb-free TQFP	Industrial
55	CY7C025E-55AXC	A100	100-Pin Pb-free TQFP	Commercial

Ordering Information (4K x 18 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0241E-15AXC	A100	100-Pin Pb-free TQFP	Commercial
	CY7C0241E-15AXI	A100	100-Pin Pb-free TQFP	Industrial
25	CY7C0241E-25AXC	A100	100-Pin Pb-free TQFP	Commercial

Ordering Information (8K x 18 Dual-Port SRAM)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C0251E–15AXC	A100	100-Pin Pb-free TQFP	Commercial

Ordering Code Definition

CY 7 C 02X 1 E

E — Die revision

1 — X18 data width

02X — 64 /128 KB Dual Port Family

C — Technology: CMOS

7 — Marketing Code: 7 = SRAM

CY — Company ID: CY=Cypress
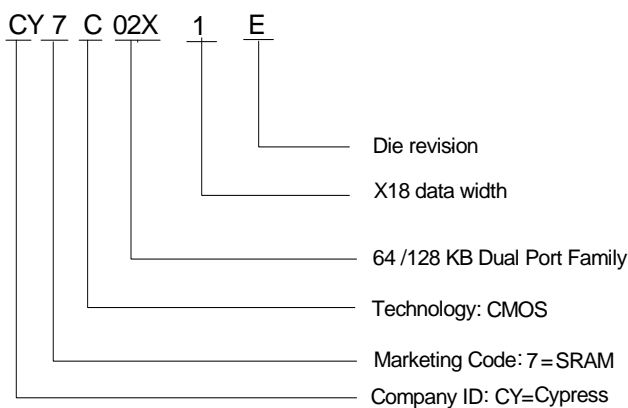
Package Diagrams

Figure 16. 100-Pin Pb-free Thin Quad Flat Pack (TQFP) A100

NOTE:

1. JEDEC STD REF MS-026

2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATC

3. DIMENSIONS IN MILLIMETERS

16.00±0.25 SQ
14.00±0.05 SQ

0.22±0.05

0.50 TYP.

R 0.08 MIN.
0.20 MAX.

0° MIN.

STAND-OFF
0.05 MIN.
0.15 MAX.

0.25

GAUGE PLANE

R 0.08 MIN.
0.20 MAX.

0°-7°

DETAIL A

0.20 MIN.

0.60±0.15

1.00 REF.

SEATING PLANE
1.60 MAX.

12°±1°
(8X)

1.40±0.05

0.08

0.20 MAX.

SEE DETAIL A

NOTE: PKG. CAN HAVE

OR

TOP LEFT CORNER CHAMFER   4 CORNERS CHAMFER

51-85048 *D

Acronyms

Acronym	Description
CMOS	Complementary metal oxide semiconductor
CE	Chip enable
OE	Output enable
RAM	Random access memory
TQFP	Thin quad plastic flatpack

Document History Page

Document Title: CY7C024E, CY7C0241E, CY7C025E, CY7C0251E, 4K x 16/18 and 8K x 16/18 Dual-Port Static RAM with SEM, INT, BUSY Document Number: 001-62932				

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2975554	RAME	07/09/2010	New Datasheet
*A	3056347	ADMU	10/28/2010	Updated "Selection Guide" on page 1: For speed bin -25: Typical Operating current(mA) changed from 180 to 170, Typical standby current for ISB1 (mA) changed from 45 to 40 For speed bin -55: Typical Operating current(mA) changed from 180 to 150, Typical standby current for ISB1 (mA) changed from 45 to 20 Updated "Electrical Characteristics Over the Operating Range" on page 9: The values for the speed bins -25 and -55 have been put into separate columns. The values for Commercial parts have been modified for the following parameters: (no degradation of spec) Operating Current ICC: "180(typ) / 275(max)" changed to "170(typ) / 250(max) for speed bin -25" and "150(typ) / 230(max) for speed bin -55" Standby Current ISB1 (both ports TTL levels): "45(typ) / 65(max)" changed to "40(typ) / 60(max) for speed bin -25", and "20(typ) / 50(max) for speed bin -55" Standby Current ISB2 (one port TTL level) : "110(typ) / 160(max)" changed to "100(typ) / 150(max) for speed bin -25", and "75(typ) / 135(max) for speed bin -55" Standby Current ISB4 (both ports CMOS Levels) : "100(typ) / 140(max)" changed to "90(typ) / 130(max) for speed bin -25", and "70(typ) / 120(max) for speed bin -55" Updated "Ordering Information (4K x 18 Dual-Port SRAM)" on page 19: Removed part CY7C0241E - 55AXI from ordering information.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products		PSoC Solutions
Automotive	cypress.com/go/automotive	psoc.cypress.com/solutions
Clocks & Buffers	cypress.com/go/clocks	PSoC 1	PSoC 3	PSoC 5
Interface	cypress.com/go/interface	
Lighting & Power Control	cypress.com/go/powerpsoc	
	cypress.com/go/plc	
Memory	cypress.com/go/memory	
Optical & Image Sensing	cypress.com/go/image	
PSoC	cypress.com/go/psoc	
Touch Sensing	cypress.com/go/touch	
USB Controllers	cypress.com/go/USB	
Wireless/RF	cypress.com/go/wireless	

All product and company names mentioned in this document are the trademarks of their respective holders.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Cypress Semiconductor](#):

  [CY7C0241E-25AXC](#) [CY7C0241E-25AXCT](#) [CY7C0241E-15AXC](#) [CY7C0241E-15AXI](#) [CY7C0241E-15AXCT](#)