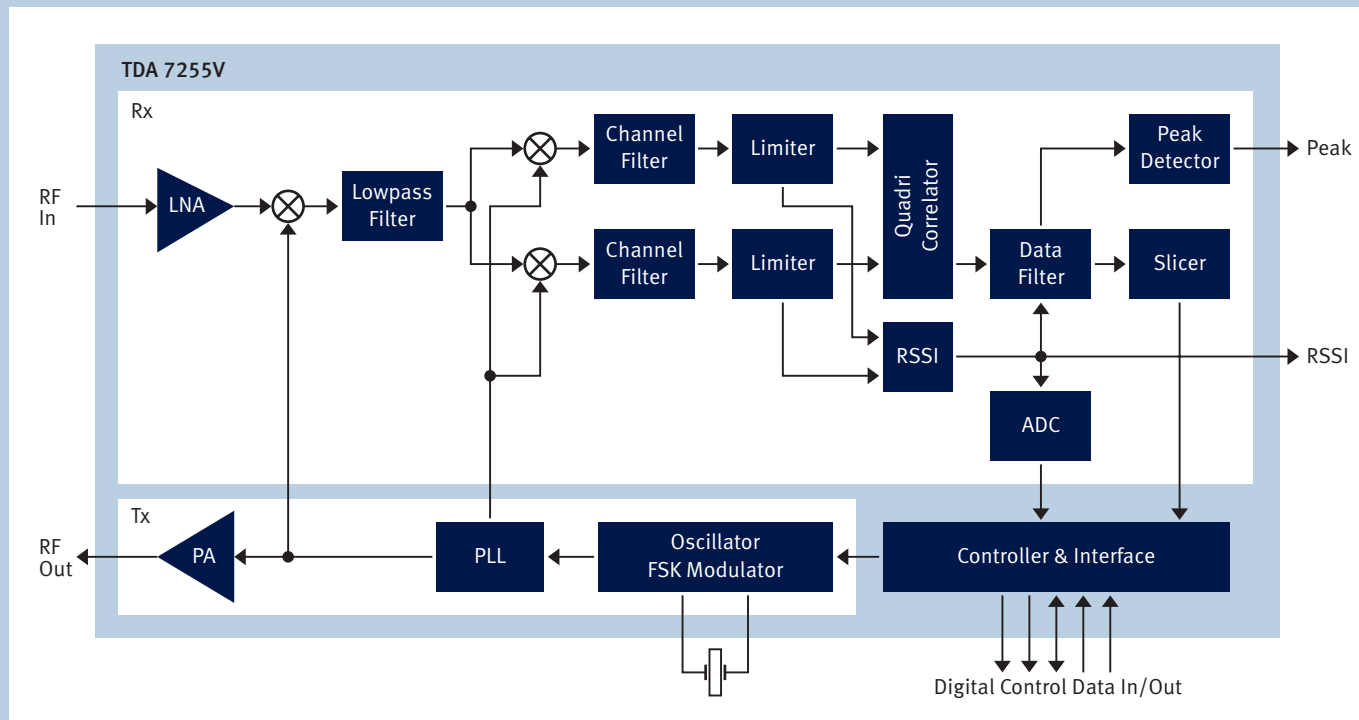


# TDA 7255V

Block Diagram TDA 7255V



## Product Summary

Feature	TDA 7255V
Frequency Range	433 ... 435MHz
Supply Voltage	2.1 ... 5.5V
Temperature Range	-40 ... +85°C
Package	PG-VQFN-40
<b>Rx</b>	
Supply Current typ. @ 3V	8.6mA (ASK) 9.0mA (FSK)
Sensitivity @ 4kbit/s Manchester	-112dBm (ASK) -115dBm (FSK)
<b>Tx</b>	
Supply Current typ. @ 3V	13.5mA
RF transmit Power typ.	9dBm

## Major Blocks and its Key Benefits

The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator with FSK modulator, a limiter with RSSI generator, an FSK demodulator, a data filter, a data comparator (slicer), a positive and a negative peak detector, a highly efficient class C power amplifier and a complex digital timing and control unit with I<sup>2</sup>C/3-wire microcontroller interface. Additionally there is a power down feature to save battery power.

The transmit section uses direct ASK modulation by switching the power amplifier, and crystal oscillator detuning for FSK modulation. The necessary detuning load capacitors are external. The capacitors for fine tuning are integrated. The receive section is using a novel single-conversion/direct-conversion scheme that is combining the advantages of both receive topologies. The IF is contained on the chip, no RF channel filters are necessary as the channel filter is also on the chip. The self-polling logic can be used to let the device operate autonomously as a master for a decoding microcontroller.

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