ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
CS51031YD8	−40°C < T_A < 85°C	SOIC−8	98 Units / Rail
CS51031YD8G		SOIC−8 (Pb−Free)	98 Units / Rail
CS51031YDR8		SOIC−8	2500 / Tape & Reel
CS51031YDR8G		SOIC−8 (Pb−Free)	2500 / Tape & Reel
CS51031GD8	0°C < T_A < 70°C	SOIC−8	98 Units / Rail
CS51031GD8G		SOIC−8 (Pb−Free)	98 Units / Rail
CS51031GDR8		SOIC−8	2500 / Tape & Reel
CS51031GDR8G		SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Rating		Value	Unit
Power Supply Voltage, V_{CC}		20	V
Driver Supply Voltage, V_C		20	V
Driver Output Voltage, V_{GATE}		20	V
C_{OSC}, CS, V_{FB} (Logic Pins)		6.0	V
Peak Output Current		1.0	A
Steady State Output Current		200	mA
Operating Junction Temperature, T_J		150	°C
Operating Temperature Range, T_A		−40 to 85	°C
Storage Temperature Range, T_S		−65 to 150	°C
ESD (Human Body Model)		2.0	kV
Lead Temperature Soldering:	Wave Solder: (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 10 sec. maximum.
2. 60 sec. max above 183°C.

PACKAGE LEAD DESCRIPTION

Package Pin Number	Pin Symbol	Function
1	V_{GATE}	Driver pin to gate of external P−Ch FET.
2	PGND	Output power stage ground connection.
3	C_{OSC}	Oscillator frequency programming capacitor.
4	GND	Logic ground.
5	V_{FB}	Feedback voltage input.
6	V_{CC}	Logic supply voltage.
7	CS	Soft−Start and fault timing capacitor.
8	V_C	Driver supply voltage.

ELECTRICAL CHARACTERISTICS (Specifications apply for $4.5 \le V_{CC} \le 16$ V, $3.0\ V \le V_C \le 16$ V; Industrial Grade: $-40°C < T_A < 85°C$; $-40°C < T_J < 125°C$: Commercial Grade: $0°C < T_A < 70°C$; $0°C < T_J < 125°C$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Oscillator	**V_{FB} = 1.2 V**				
Frequency	C_{OSC} = 470 pF	160	200	240	kHz
Charge Current	1.4 V < V_{COSC} < 2.0 V	−	110	−	μA
Discharge Current	2.7 V > V_{COSC} > 2.0 V	−	660	−	μA
Maximum Duty Cycle	1 − (t_{OFF}/t_{ON})	80.0	83.3	−	%
Short Circuit Timer	**V_{FB} = 1.0 V; CS = 0.1 μF; V_{COSC} = 2.0 V**				
Charge Current	1.0 V < V_{CS} < 2.0 V	175	264	325	μA
Fast Discharge Current	2.55 V > V_{CS} > 2.4 V	40	66	80	μA
Slow Discharge Current	2.4 V > V_{CS} > 1.5 V	4.0	6.0	10	μA
Start Fault Inhibit Time	0 V < V_{CS} < 2.5 V	0.70	0.85	1.40	ms
Valid Fault Time	2.6 V > V_{CS} > 2.4 V	0.2	0.3	0.45	ms
GATE Inhibit Time	2.4 V > V_{CS} > 1.5 V	9.0	15	23	ms
Fault Duty Cycle	−	2.5	3.1	4.6	%
CS Comparator	**V_{FB} = 1.0 V**				
Fault Enable CS Voltage	−	−	2.5	−	V
Max CS Voltage	V_{FB} = 1.5 V	−	2.6	−	V
Fault Detect Voltage	V_{CS} when GATE goes high	−	2.4	−	V
Fault Inhibit Voltage	Minimum V_{CS}	−	1.5	−	V
Hold Off Release Voltage	V_{FB} = 0 V	0.4	0.7	1.0	V
Regulator Threshold Voltage Clamp	V_{CS} = 1.5 V	0.725	0.866	1.035	V
V_{FB} Comparators	**V_{COSC} = V_{CS} = 2.0 V**				
Regulator Threshold Voltage	T_J = 25°C (Note 3) T_J = −40 to 125°C	1.225 1.210	1.250 1.250	1.275 1.290	V V
Fault Threshold Voltage	T_J = 25°C (Note 3) T_J = −40 to 125°C	1.12 1.10	1.15 1.15	1.17 1.19	V V
Threshold Line Regulation	$4.5\ V \le V_{CC} \le 16$ V	−	6.0	15	mV
Input Bias Current	V_{FB} = 0 V	−	1.0	4.0	μA
Voltage Tracking	(Regulator Threshold − Fault Threshold Voltage)	70	100	120	mV
Input Hysteresis Voltage	−	−	4.0	20	mV
Power Stage	**V_{CC} = V_C = 10 V; V_{FB} = 1.2 V**				
GATE DC Low Saturation Voltage	V_{COSC} = 1.0 V; 200 mA Sink	−	1.2	1.5	V
GATE DC High Saturation Voltage	V_{COSC} = 2.7 V; 200 mA Source; $V_C = V_{GATE}$	−	1.5	2.1	V
Rise Time	C_{GATE} = 1.0 nF; 1.5 V < V_{GATE} < 9.0 V	−	25	60	ns
Fall Time	C_{GATE} = 1.0 nF; 9.0 V > V_{GATE} > 1.5 V	−	25	60	ns
V_{CC} Monitor					
Turn−On Threshold	−	4.200	4.400	4.600	V
Turn−Off Threshold	−	4.085	4.300	4.515	V
Hysteresis	−	65	130	200	mV
Current Drain					
I_{CC}	4.5 V < V_{CC} < 16 V, Gate switching	−	4.5	6.0	mA
I_C	3.0 V < V_C < 16 V, Gate non−switching	−	2.7	4.0	mA
Shutdown I_{CC}	V_{CC} = 4.0	−	500	900	μA

3. Guaranteed by design, not 100% tested in production.

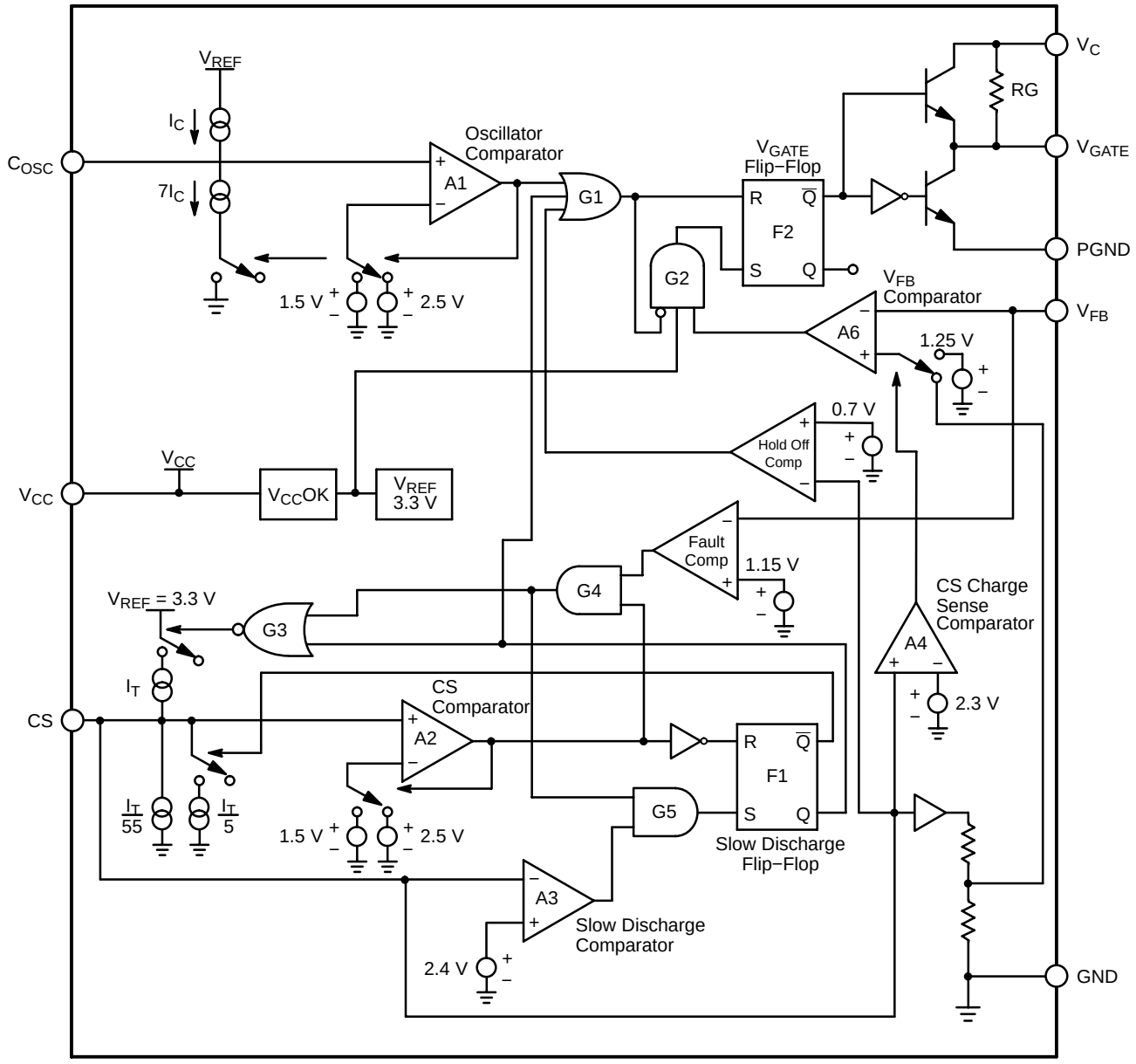


Figure 2. Block Diagram

CIRCUIT DESCRIPTION

THEORY OF OPERATION

Control Scheme

The CS51031 monitors the output voltage to determine when to turn on the P−Ch FET. If V_{FB} falls below the internal reference voltage of 1.25 V during the oscillator's charge cycle, the P−Ch FET is turned on and remains on for the duration of the charge time. The P−Ch FET gets turned off and remains off during the oscillator's discharge time with the maximum duty cycle to 80%. It requires 7.0 mV typical, and 20 mV maximum ripple on the V_{FB} pin is required to operate. This method of control does not require any loop stability compensation.

Startup

The CS51031 has an externally programmable Soft−Start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As V_{CC} rises, the V_C voltage along with the internal resistor R_G keeps the P−Ch FET off. As V_{CC} and V_C continue to rise, the oscillator capacitor (C_{OSC}) and the Soft−Start/Fault Timing capacitor (CS) charges via internal current sources. C_{OSC} gets charged by the current source IC and CS gets charged by the I_T source combination described by:

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5}\right)$$

The internal Holdoff Comparator ensures that the external P−Ch FET is off until V_{CS} > 0.7 V, preventing the GATE flip−flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft−Start is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 of the voltage at the CS pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7 V, the low feedback to the V_{FB} Comparator sets the GATE flip−flop during C_{OSC}'s charge cycle. Once the GATE flip−flop is set, V_{GATE} goes low and turns on the P−Ch FET. When V_{CS} exceeds 2.3 V, the CS charge sense comparator (A4) sets the V_{FB} comparator reference to 1.25 V completing the startup cycle.

Lossless Short Circuit Protection

The CS51031 has "lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage) reaches 2.5 V during startup, the fault timing circuitry is enabled by A2. During normal operation the CS voltage is 2.6 V. During a short circuit or a transient condition, the output voltage moves lower and the voltage at V_{FB} drops. If V_{FB} drops below 1.15 V, the output of the fault comparator goes high and the CS51031 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4 V. If the V_{FB} voltage is still below 1.15 V when the CS pin reaches 2.4 V, a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip−flop. The V_{GATE} flip−flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5 V. The CS51031 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5 V, the fast and slow discharge cycles repeat as shown in figure 3.

If the V_{FB} voltage is above 1.15 V when CS reaches 2.4 V a fault condition is not detected, normal operation resumes and CS charges back to 2.6 V. This reduces the chance of erroneously detecting a load transient as a fault condition.

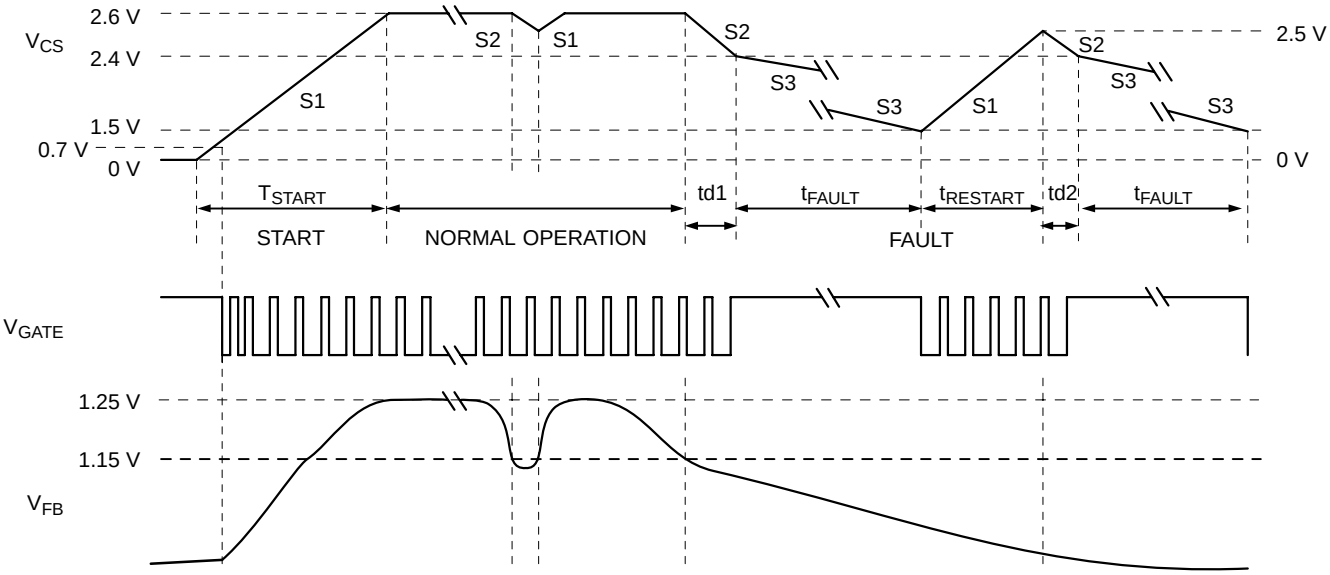


Figure 3. Voltage on Start Capacitor (V_{GS}), the Gate (V_{GATE}), and in the Feedback Loop (V_{FB}), During Startup, Normal and Fault Conditions

Buck Regulator Operation

A block diagram of a typical buck regulator is shown in Figure 4. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O. When the voltage across C_O drops below the threshold established by the feedback resistors R1 and R2 and the reference voltage V_{REF}, the power transistor Q1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $(V_{IN} - V_{OUT})/L$. The duty cycle (or "on" time) for the CS51031 is limited to 80%. If output voltage remains higher than nominal during the entire C_{OSC} change time, the Q1 does not turn on, skipping the pulse.

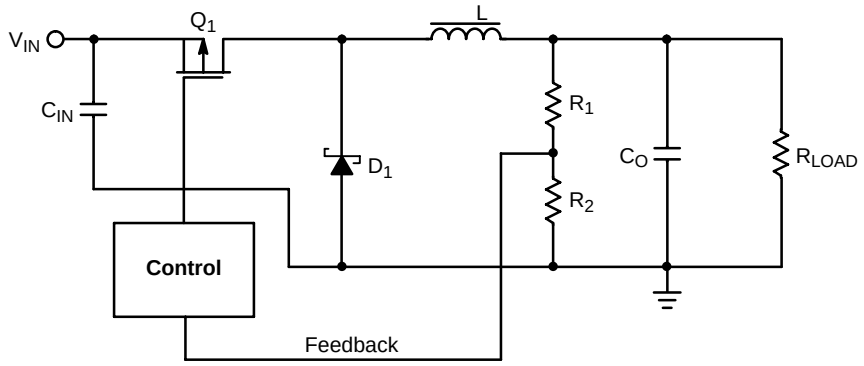


Figure 4. Buck Regulator Block Diagram

APPLICATIONS INFORMATION

CS51031 DESIGN EXAMPLE

Specifications 12 V to 5.0 V, 3.0 A Buck Controller

- V_{IN} = 12 V ±20% (i.e. 14.4 V max, 12 V nom, 9.6 V min)
- V_{OUT} = 5.0 V ±2%
- I_{OUT} = 0.3 A to 3.0 A
- Output ripple voltage < 50 mV max
- Efficiency > 80%
- f_{SW} = 200 kHz

1) Duty Cycle Estimates

Since the maximum duty cycle D, of the CS51031 is limited to 80% min, it is necessary to estimate the duty cycle for the various input conditions over the complete operating range.

The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$D = \frac{V_{OUT} + V_F}{V_{IN} - V_{SAT}}$$

where:

$V_{SAT} = R_{DS(ON)} \times I_{OUT}$ max and $R_{DS(ON)}$ is the value at T_J 100°C.

If V_F = 0.60 V and V_{SAT} = 0.60 V then the above equation becomes:

$$D_{MAX} = \frac{5.6}{9.0} = 0.62$$

$$D_{MIN} = \frac{5.6}{13.8} = 0.40$$

2) Switching Frequency and On and Off Time Calculations

Given that f_{SW} = 200 kHz and D_{MAX} = 0.80

$$T = \frac{1.0}{f_{SW}} = 5.0\ \mu s$$

$$T_{ON(max)} = T \times D_{MAX} = 5.0\ \mu s \times 0.62 \cong 3.0\ \mu s$$

$$T_{ON(min)} = T \times D_{MIN} = 5.0\ \mu s \times 0.40 \cong 2.0\ \mu s$$

$$T_{OFF(max)} = T_{ON(min)} = 5.0\ \mu s - 2.0\ \mu s = 3.0\ \mu s$$

3) Oscillator Capacitor Selection

The switching frequency is set by C_{OSC}, whose value is given by:

$$C_{OSC}\ \text{in pF} = \frac{95 \times 10^{+6}}{F_{SW}\left(1 + \frac{F_{SW}}{3 \times 10^6} - \left(\frac{30 \times 10^3}{F_{SW}}\right)^2\right)}$$

4) Inductor Selection

The inductor value is chosen for continuous mode operation down to 0.3 Amps.

The ripple current $\Delta I = 2 \times I_{OUT}min = 2 \times 0.3\ A = 0.6\ A$.

$$L_{min} = \frac{(V_{OUT} + V_D) \times T_{OFF(max)}}{\Delta I} = \frac{5.6\ V \times 3.0\ \mu s}{0.6\ A} = 28\ \mu H$$

This is the minimum value of inductor to keep the ripple current < 0.6 A during normal operation.

A smaller inductor will result in larger ripple current. Ripple current at a minimum off time is:

$$\Delta I = \frac{(V_{OUT} + V_F) \times T_{OFF(min)}}{L_{MIN}} = \frac{5.6\ V \times 2.0\ \mu s}{28\ \mu H} = 0.4\ A$$

The core must not saturate with the maximum expected current, here given by:

$$I_{MAX} = I_{OUT} + \Delta I/2 = 3.0\ A + 0.4\ A/2 = 3.2\ A$$

5) Output Capacitor

The output capacitor and the inductor form a low pass filter. The output capacitor should have a low ESL and ESR. Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are less expensive. Solid tantalum chip capacitors are available from a number of suppliers and are the best choice for surface mount applications.

The output capacitor limits the output ripple voltage. The CS51031 needs a maximum of 20 mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50 mV peak−to−peak is given by:

$$C = \frac{\Delta I}{8.0 \times f_{SW} \times \Delta V} = \frac{0.6\ A}{8.0 \times (200 \times 10^3 Hz) \times (50 \times 10^{-3}\ V)} = 7.5 \mu F$$

The minimum ESR needed to limit the output voltage ripple to 50 mV peak−to−peak is:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.6\ A} = 83\ m\Omega$$

The output capacitor should be chosen so that its ESR is less than 83 mΩ.

During the minimum off time, the ripple current is 0.4 A and the output voltage ripple will be:

$$\Delta V = ESR \times \Delta I = 83m\ \Omega \times 0.4 = 33\ mV$$

6) V_{FB} Divider

$$V_{OUT} = 1.25\ V\left(\frac{R1 + R2}{R2}\right) = 1.25\ V\left(\frac{R1}{R2} + 1.0\right)$$

The input bias current to the comparator is 4.0 μA. The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this permits a divider current of 1.0 mA and simplifies the calculations.

$$\frac{5.0\ V}{1.0\ mA} = R1 + R2 = 5.0\ K\Omega$$

Let R2 = 1.0 K

Rearranging the divider equation gives:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1.0\right) = 1.0\ k\Omega\left(\frac{5.0\ V}{1.25} - 1.0\right) = 3.0\ k\Omega$$

7) Divider Bypass Capacitor C_{RR}

Since the feedback resistors divide the output voltage by a factor of 4.0, i.e. 5.0 V/1.25 V = 4.0, it follows that the output ripple is also divided by four. This would require that the output ripple be at least 60 mV (4.0 × 15 mV) to trip the feedback comparator. We use a capacitor C_{RR} to act as an AC short.

The ripple voltage frequency is equal to the switching frequency so we choose C_{RR} = 1.0 nF.

8) Soft−Start and Fault Timing Capacitor CS

CS performs several important functions. First it provides a delay time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides Soft−Start by clamping the reference voltage during startup, allowing it to rise slowly, and, finally it controls the hiccup short circuit protection circuitry. This reduces the duty cycle to approximately 0.035 during short circuit conditions.

An important consideration in calculating CS is that it's voltage does not reach 2.5 V (the voltage at which the fault detect circuitry is enabled) before V_{FB} reaches 1.15 V otherwise the power supply will never start.

If the V_{FB} pin reaches 1.15 V, the fault timing comparator will discharge CS and the supply will not start. For the V_{FB} voltage to reach 1.15 V the output voltage must be at least 4 × 1.15 = 4.6 V.

If we choose an arbitrary startup time of 900 μs, the value of CS is:

$$t_{Startup} = \frac{CS \times 2.5\ V}{I_{Charge}}$$

$$CS_{min} = \frac{900\ \mu s \times 264\ \mu A}{2.5\ V} = 950\ nF \cong 0.1\ \mu F$$

The fault time is the sum of the slow discharge time the fast discharge time and the recharge time. It is dominated by the slow discharge time.

The first parameter is the slow discharge time, it is the time for the CS capacitor to discharge from 2.4 V to 1.5 V and is given by:

$$t_{SlowDischarge(t)} = \frac{CS \times (2.4\ V - 1.5\ V)}{I_{Discharge}}$$

where $I_{Discharge}$ is 6.0 μA typical.

$$t_{SlowDischarge(t)} = CS \times 1.5 \times 10^5$$

The fast discharge time occurs when a fault is first detected. The CS capacitor is discharged from 2.5 V to 2.4 V.

$$t_{FastDischarge(t)} = \frac{CS \times (2.5\ V - 2.4\ V)}{I_{FastDischarge}}$$

where $I_{FastDischarge}$ is 66 μA typical.

$$t_{FastDischarge(t)} = CS \times 1515$$

The recharge time is the time for CS to charge from 1.5 V to 2.5 V.

$$t_{Charge(t)} = \frac{CS \times (2.5\ V - 1.5\ V)}{I_{Charge}}$$

where I_{Charge} is 264 μA typical.

$$t_{Charge(t)} = CS \times 3787$$

The fault time is given by:

$$t_{Fault} = CS \times (3787 + 1515 + 1.5 \times 10^5)$$

$$t_{Fault} = CS \times (1.55 \times 10^5)$$

For this circuit

$$t_{Fault} = 0.1 \times 10^{-6} \times 1.55 \times 10^5 = 15.5\ \mu s$$

A larger value of CS will increase the fault time out time but will also increase the Soft−Start time.

9) Input Capacitor

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on the V_{CC} and V_C pins. This capacitor must also ensure that the V_{CC} remains above the UVLO voltage in the event of an output short circuit. A low ESR capacitor of at least 100 μF is good. A ceramic surface mount capacitor should also be connected between V_{CC} and ground to filter high frequency noise.

10) MOSFET Selection

The CS51031 drives a P−Channel MOSFET. The V_{GATE} pin swings from GND to V_C. The type of P−Ch FET used depends on the operating conditions but for input voltages below 7.0 V a logic level FET should be used.

A P−Ch FET with a continuous drain current (I_D) rating greater than the maximum output current is required.

The Gate−to−Source voltage V_{GS} and the Drain−to Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$P_D = I_{OUT}^2 \times R_{DS(ON)} \times D$$

where

$$R_{DS(ON)} \text{ is the value at } T_J = 100^\circ C$$

The power dissipation of the P−Ch FET due to the switching losses is given by:

$$P_D = 0.5 \times V_{IN} \times I_{OUT} \times (t_r) \times f_{SW}$$

where t_r = Rise Time.

11) Diode Selection

The flyback or catch diode should be a Schottky diode because of it's fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20 V for this 12 V application.

The diode power dissipation is given by:

$$P_D = I_{OUT} \times V_D \times (1.0 - D_{min})$$

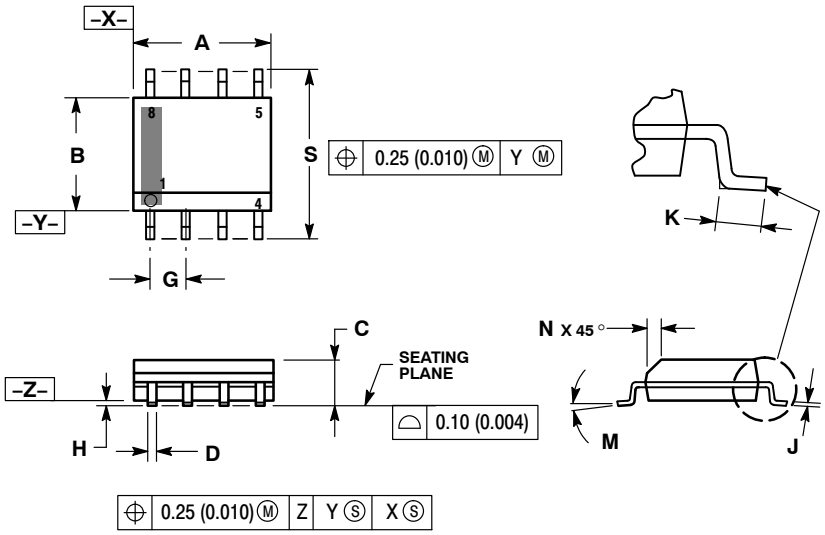
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

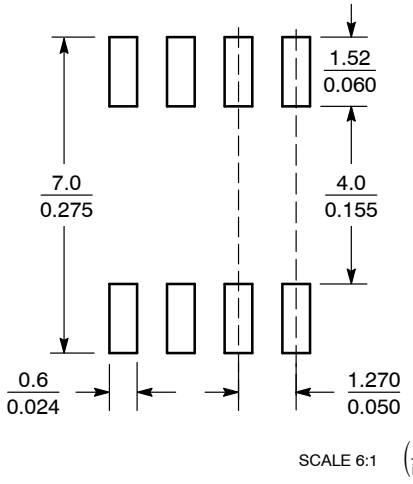
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

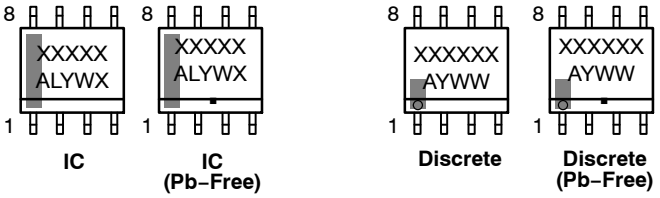
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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