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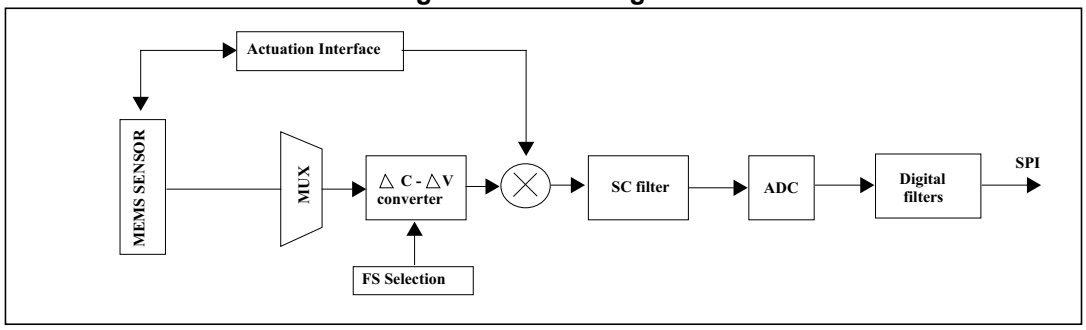
1 Block diagram and pin description

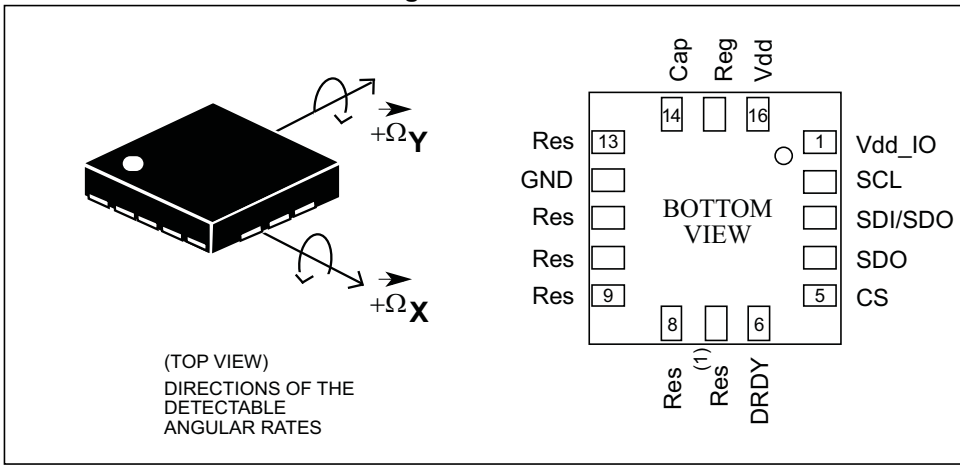
1.1 System block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections



1. Leave pin electrically unconnected and soldered to PCB.

Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL	Clock line for SPI interface
3	SDI/SDO	Serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO	Serial data output (SDO)
5	CS	Chip-select line
6	DRDY	Data ready signal
7	Res(1)	Leave unconnected
8	Res	Connect to GND
9	Res	Connect to GND
10	Res	Connect to GND
11	Res	Connect to GND
12	GND	0 V power supply
13	Res	Connect to GND
14	Cap	Capacitance connection pin for internal charge pump
15	Reg	Capacitance connection pin for internal regulator
16	Vdd	Power supply

1. Leave pin electrically unconnected and soldered to PCB.

2 Terminology & functionality

2.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.2 Zero-rate level

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of highly accurate MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor on a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

2.3 Data-ready interrupt and synchronous reading

On the L2G2IS the angular rate data can be retrieved using a synchronous read. To perform a synchronous read, *CTRL_REG3 (0Dh)* (DRDY_EN) has to be set to '1' in order to enable the data-ready interrupt on the DRDY pin (refer to *Figure 4*). To properly perform a synchronous read, the angular rate data have to be read every time the DRDY pin goes high.

The DRDY signal can be latched (default condition) or pulsed if the *CTRL_REG1 (0Bh)* (P_DRDY) is set to ‘1’. When a latched condition is selected, the interrupt goes low when the high part of one of the output channels is read (OUT_X_H (04h) or OUT_Y_H (06h)) and returns high when new data is generated. When a pulsed condition is selected, the interrupt behavior is independent from the reading operations and remains high for 75 µsec every time new data is generated. The DRDY pin is set by default as push-pull output, but it can be configured as open-drain output by setting *CTRL_REG3 (0Dh)* (PP_OD) to ‘1’.

2.4 Temperature sensor

The temperature data can be retrieved from the *TEMP_OUT_L (01h), TEMP_OUT_H (02h)* register, as two’s complement data in 12-bit format left-justified. The output of the temperature sensor is 0 at 25 °C.

3 Mechanical and electrical characteristics

3.1 Mechanical characteristics

Vdd = 2.4 V and T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
FS	Measurement range			±100		dps
				±200		
So	Sensitivity	FS = ±100 dps		262		LSb/dps
		FS = ±200 dps		131		
DVoff	Digital zero-rate level			±5		dps
Rn	Rate noise density[2]	0 - 20 Hz bandwidth		0.006		$dps/(\sqrt{Hz})$
PhDl	Phase delay[3]	At 20 Hz (280 Hz BW selected)		7		deg
ODR	Digital output data rate			9.09		kHz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Guaranteed by design.
3. Refer to *Figure 9: LPF chain block diagram* and *Table 24: Low-pass filter cutoff frequency selection*.

a. The product is factory calibrated at 2.4 V. The operational power supply range is specified in *Table 4*.

3.2 Electrical characteristics

@ Vdd = 2.4 V, T = 25 °C unless otherwise noted[b].

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		1.71	2.4	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.71		Vdd	V
Idd	Supply current in normal mode			3.8		mA
IddSL	Supply current in sleep mode[3]			1.85		mA
IddPdn	Supply current in power-down mode				20	µA
IcapIO	I/O pad driving current capability				4	mA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
3. Sleep mode introduces a faster turn-on time relative to power-down mode.

b. The product is factory calibrated at 2.4 V.

3.3 Temperature sensor characteristics

@ AVdd = 2.4 V, T = 25 °C unless otherwise noted[c].

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature			0.0625		°C/digit
TODR	Temperature refresh rate			70		Hz
TACC	Temperature absolute accuracy(2)			±4		°C
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 at 25 °C. Refer to *Section 2.4: Temperature sensor* on how to read the temperature sensor output data.

c. The product is factory calibrated at 2.4 V.

3.4 SPI - serial peripheral interface

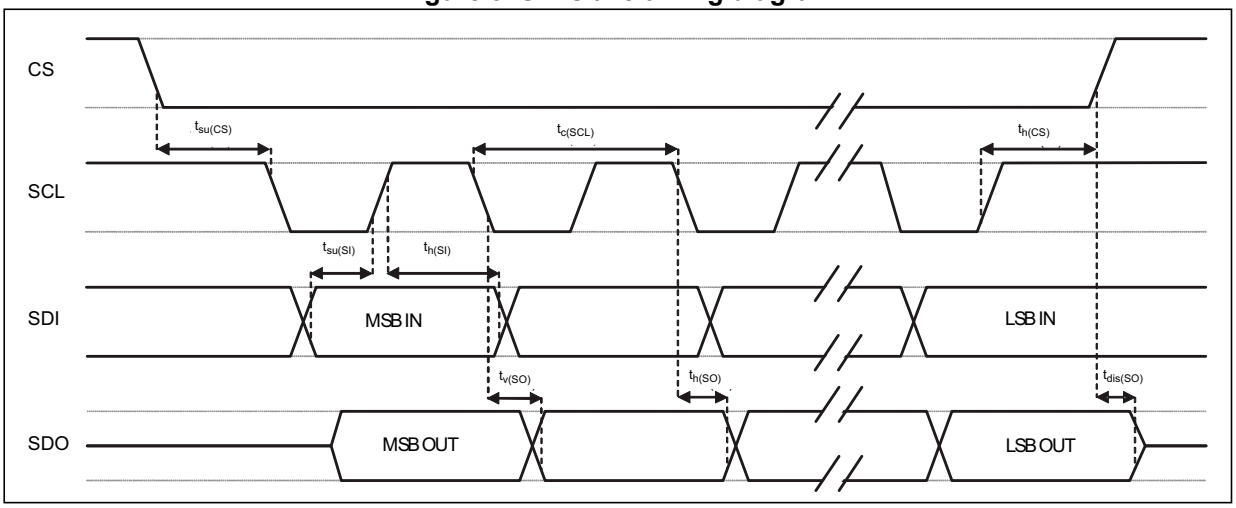
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SCL)}$	SPI clock cycle	100		ns
$f_{c(SCL)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	6		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

3.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Power supply	-0.3 to 4.8	V
Vdd_IO	Power supply for I/O pins	-0.3 to Vdd	V
Vin	Input voltage on: (CS, SDI/SDO, SDO, SCL)	-0.3 to Vdd_IO +0.1	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.2 ms	10,000	*g*
ESD	Electrostatic discharge protection	2 (HBM)	kV

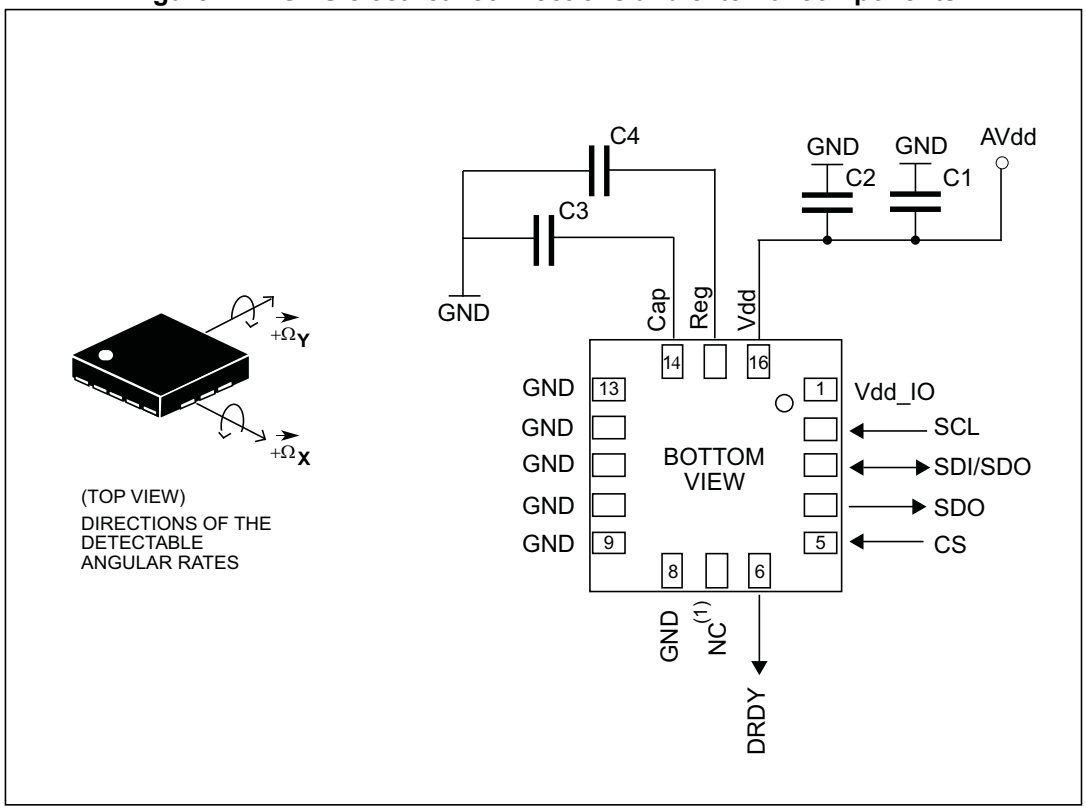
Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4 Application hints

Figure 4. L2G2IS electrical connections and external components



1. Leave pin electrically unconnected and soldered to PCB.

Table 8. External component values

Name	Value	Purpose
C1	1 µF	Decoupling
C2	100 pF	Decoupling
C3(1)	10 nF (16 V class)	Charge pump
C4	100 nF (5 V class)	Internal regulator

1. This value must guarantee a minimum of 1 nF value under 12 V bias condition.

Power supply decoupling capacitors (100 pF + 1 µF) should be placed as near as possible to the device (common design practice).

5 Digital interfaces

The registers embedded inside the L2G2IS may be accessed through the SPI serial interfaces.

Table 9. Serial interface pin description

Pin name	Pin description
CS	Chip-select line
SCL	SPI serial port clock
SDI/SDO	Serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	Serial data output (SDO)

5.1 SPI bus interface

The SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface connects to applications using 4 wires: **CS**, **SCL**, **SDI** and **SDO**.

CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SCL** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SCL** and should be captured at the rising edge of **SCL**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SCL**. The first bit (bit 0) starts at the first falling edge of **SCL** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SCL** just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive SDO at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

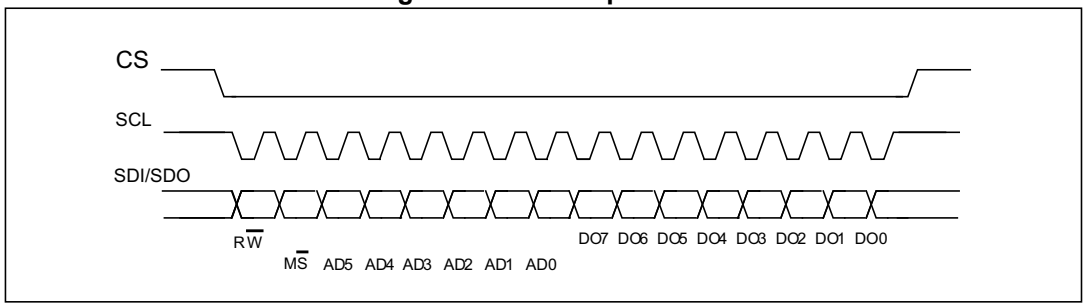
bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The function and the behavior of SDI and SDO remain unchanged.

5.1.1 SPI read

Figure 5. SPI read protocol



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

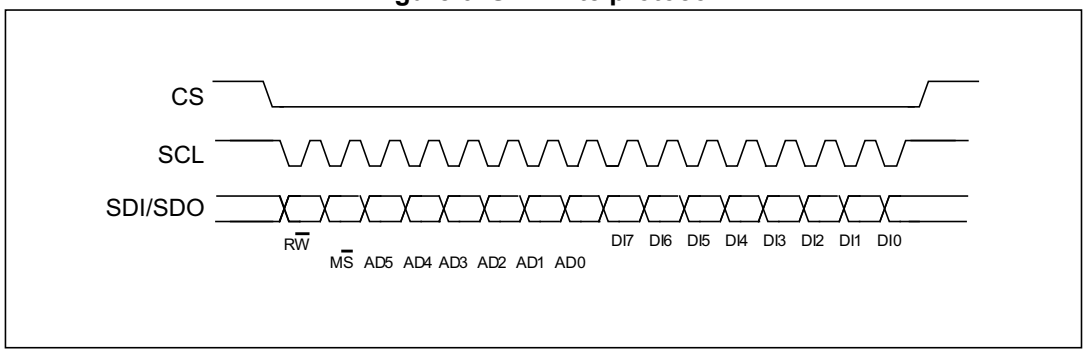
bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

A multiple read command is also available.

5.1.2 SPI write

Figure 6. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

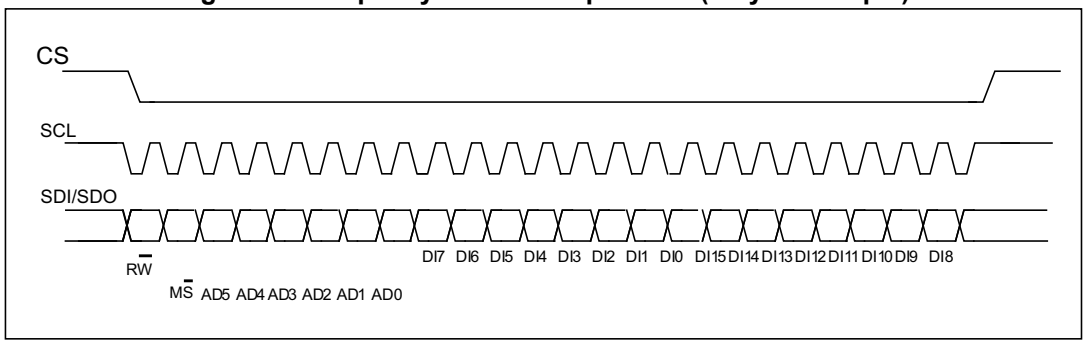
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

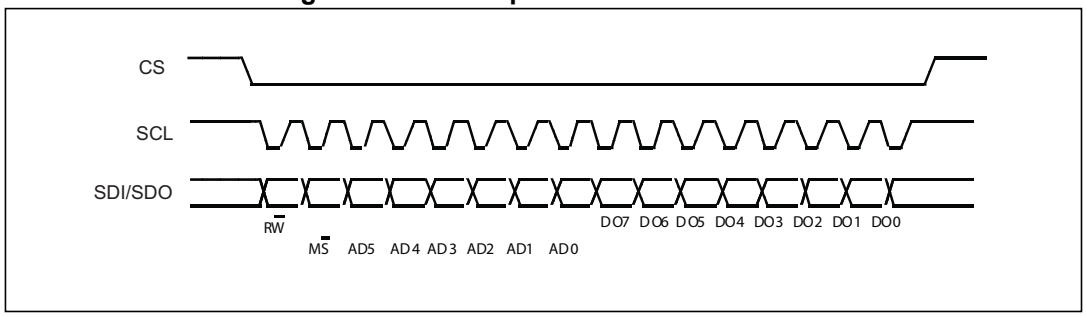
Figure 7. Multiple byte SPI write protocol (2-byte example)



5.1.3 SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL_REG1 (0Bh)* (SIM) bit equal to '1' (SPI serial interface mode selection).

Figure 8. SPI read protocol in 3-wire mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

6 Output register mapping

The table given below provides a listing of the 8-bit registers embedded in the device and the related addresses.

Table 10. Register address map

Name	Type	Register address [Hex]	Default [Hex]	Comment
WHO_AM_I	r	00	D9	
TEMP_OUT_L	r	01	output	
TEMP_OUT_H	r	02	output	
OUT_X_L	r	03	output	
OUT_X_H	r	04	output	
OUT_Y_L	r	05	output	
OUT_Y_H	r	06	output	
Reserved	--	07-08	--	
STATUS_REG	r	09	output	
Reserved	--	0A	--	Reserved
CTRL_REG1	r/w	0B	00	
CTRL_REG2	r/w	0C	00	
CTRL_REG3	r/w	0D	00	
Reserved	--	0E-0F	--	Reserved
ORIENT_CONFIG	r/w	10	00	
OFF_X	r/w	11	00	
OFF_Y	r/w	12	00	
Reserved	--	13-1E	--	Reserved
CTRL_REG4	r/w	1F	00	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

7.1 WHO_AM_I (00h)

Table 11. WHO_AM_I register

1	1	0	1	1	0	0	1

7.2 TEMP_OUT_L (01h), TEMP_OUT_H (02h)

Table 12. TEMP_OUT_L register

Temp3	Temp2	Temp1	Temp0	0	0	0	0

Table 13. TEMP_OUT_H register

Temp11	Temp10	Temp9	Temp8	Temp7	Temp6	Temp5	Temp4

Table 14. TEMP_OUT resolution

Temp11-Temp0	Temperature data. Refer to: *Section 2.4: Temperature sensor* on how to read the temperature sensor output data.

7.3 OUT_X_L (03h), OUT_X_H (04h)

X-axis angular rate data. The value is expressed as two’s complement.

7.4 OUT_Y_L (05h), OUT_Y_H (06h)

Y-axis angular rate data. The value is expressed as two’s complement.

7.5 STATUS_REG (09h)

Table 15. STATUS_REG register

YXOR	XOR	YOR	0	YXDA	XDA	YDA	0

Table 16. STATUS_REG description

YXOR	X-, Y-axis data overrun. (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
XOR	X-axis data overrun. (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
YOR	Y-axis data overrun. (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
YXDA	X-, Y-axis new data available. (0: a new set of data is not yet available; 1: a new set of data is available)
XDA	X-axis new data available. (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)
YDA	Y-axis new data available. (0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available)

7.6 CTRL_REG1 (0Bh)

Table 17. CTRL_REG1 register

BOOT	P_DRDY	BLE	SIM	ODU	0(1)	PW1	PW0

1. This bit must be set to ‘0’ for proper operation of the device.

Table 18. CTRL_REG1 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content(1))
P_DRDY	DRDY signal pulsed. Default value: 0 (0: DRDY is latched; 1: DRDY is pulsed)
BLE	Big/little endian data selection. Default value: 0 (0: Data LSB @ lower address; 1: Data MSB @ lower address)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).
ODU	Output data update. Default value: 0 (0: output registers not updated until MSB and LSB have been read; 1: output registers updated continuously)
PW[1:0]	Operating mode selection. Default value: 00 Refer to *Table 19: Operating mode selection*.

1. Boot request is executed as soon as internal oscillator is turned-on. It is possible to set this bit while in power-down mode, in this case it will be served at the next normal mode or sleep mode.

Table 19. Operating mode selection

PW1	PW0	Operating mode selection
0	0	Power-down
0	1	Power-down
1	0	Sleep mode
1	1	Normal mode

7.7 CTRL_REG2 (0Ch)

Table 20. CTRL_REG2 register

LPF_O	0(1)	0(1)	0(1)	0(1)	HPreset	SWreset	HPF

1. These bits must be set to '0' for proper operation of the device.

Table 21. CTRL_REG2 description

LPF_O	Low-pass filter order selection. Default value: 0 (0: 2nd order; 1: 1st order). Refer to *Figure 9: LPF chain block diagram* and *Table 24: Low-pass filter cutoff frequency selection*
HPreset	High-pass filter reset. Default value: 0 (1: HPF reset on X and Y-axis)
SWreset	Software reset. Default value: 0 (1: all the configuration register values are restored to default values).
HPF	High-pass filter enable. Default value: 0 (0: high-pass filter is disabled; 1: high-pass filter is enabled)

7.8 CTRL_REG3 (0Dh)

Table 22. CTRL_REG3 register

0(1)	ST	0(1)	PP_OD	0(1)	0(1)	DRDY _EN	LPF_D

1. These bits must be set to '0' for proper operation of the device.

Table 23. CTRL_REG3 description

ST	Self-test enable. Default value: 0 (0: Self-test disabled; 1: Self-test enabled)
PP_OD	DRDY pin configuration. Default value: 0 (0: push-pull; 1: open drain)
DRDY_EN	Data ready enable on DRDY pin. Default: 0 (1: DRDY on pin). *Section 2.3: Data-ready interrupt and synchronous reading*.
LPF_D	Digital low-pass filter enable. Default value: 0 (0: digital low-pass filter disabled; 1: digital low-pass filter enabled). Refer to *Figure 9: LPF chain block diagram* and *Table 24: Low-pass filter cutoff frequency selection*.

Figure 9. LPF chain block diagram

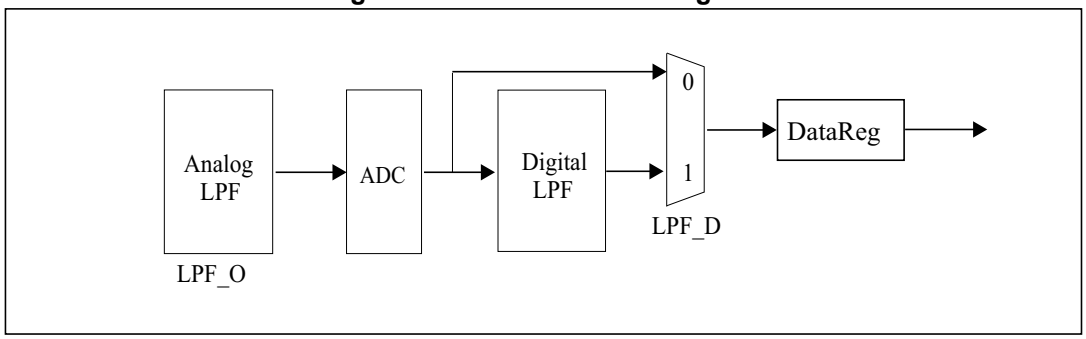


Table 24. Low-pass filter cutoff frequency selection

LPF_O (*CTRL_REG2 (0Ch)*)	LPF_D (*CTRL_REG3 (0Dh)*)	BW (Hz)	Phase delay @ 20 Hz
0	0	280	7 deg (default)
0	1	140	13.5 deg
1	0	350	5 deg
1	1	150	11.5 deg

7.9 ORIENT_CONFIG (10h)

Table 25. ORIENT_CONFIG register

0(1)	0(1)	Sign_x	Sign_y	0(1)	0(1)	0(1)	Orient

1. These bits must be set to '0' for proper operation of the device.

Table 26. ORIENT_CONFIG description

Sign_x	X-axis angular rate sign. Default value: 0 (0: sign unvaried; 1: sign inverted)
Sign_y	Y-axis angular rate sign. Default value: 0 (0: sign unvaried; 1: sign inverted)
Orient	Directional orientation selection. Default value: 0 (0: X-axis - Y-axis; 1: Y-axis - X-axis)

7.10 OFF_X (11h)

Table 27. OFF_X register

OFFX7	OFFX6	OFFX5	OFFX4	OFFX3	OFFX2	OFFX1	OFFX0

Table 28. OFF_X description

OFFX[7:0]	User offset correction register for X-axis. Default value: 0000 0000 The value is expressed as two's complement.

7.11 OFF_Y(12h)

Table 29. OFF_Y register

OFFY7	OFFY6	OFFY5	OFFY4	OFFY3	OFFY2	OFFY1	OFFY0

Table 30. OFF_Y description

OFFY[7:0]	User offset correction register for Y-axis. Default value: 0000 0000 The value is expressed as two's complement.

7.12 CTRL_REG4 (1Fh)

Table 31. CTRL_REG4 register

0(1)	0(1)	0(1)	0(1)	FS	0(1)	0(1)	HPF_BW

1. These bits must be set to '0' for proper operation of the device.

Table 32. CTRL_REG4 description

FS	Full-scale selection. Default value: 0 (0: ±100 dps; 1: ±200 dps)
HPF_BW	Digital high-pass filter cutoff frequency selection. Default value: 0 Refer to *Table 33: High-pass filter cutoff frequency selection*

Table 33. High-pass filter cutoff frequency selection

HPF_BW0	HP cutoff frequency selection
0	0.02 Hz
1	0.09 Hz

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at *www.st.com/mems*.

8.2 LGA-16 package

Figure 10. LGA-16 package outline and dimensions

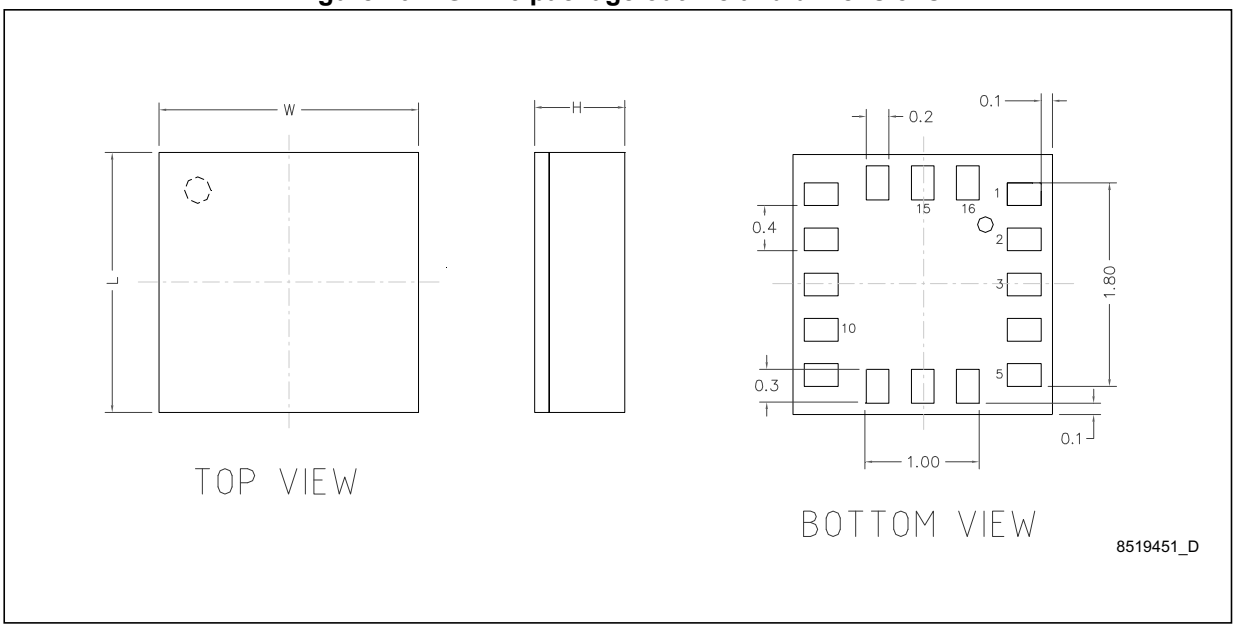


Table 34. LGA-16 package outer dimensions

Item	Dimension [mm]	Tolerance [mm]
Length [L]	2.30	±0.1
Width [W]	2.30	±0.1
Height [H]	0.70	MAX

9 Revision history

Table 35. Document revision history

Date	Revision	Changes
16-Mar-2015	1	Initial release
17-Feb-2016	2	Added footnote to pin 7 in *Figure 2*, *Table 2*, and *Figure 4* Updated *Section 2.3: Data-ready interrupt and synchronous reading* Updated Sg in *Table 7: Absolute maximum ratings*

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