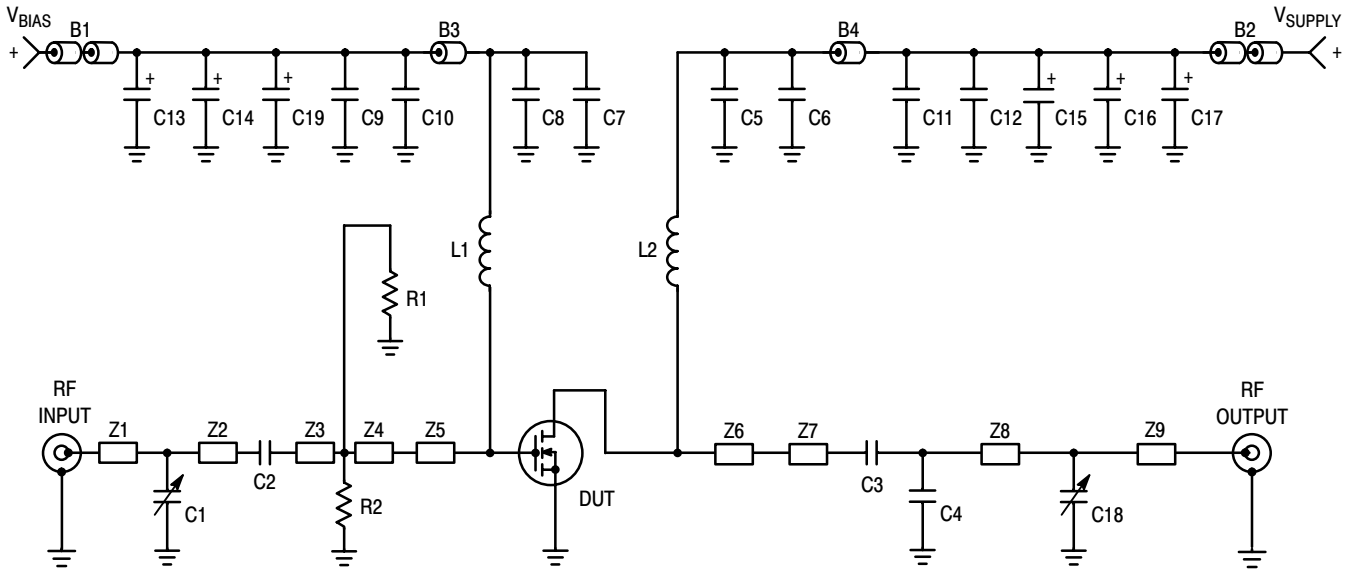
Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

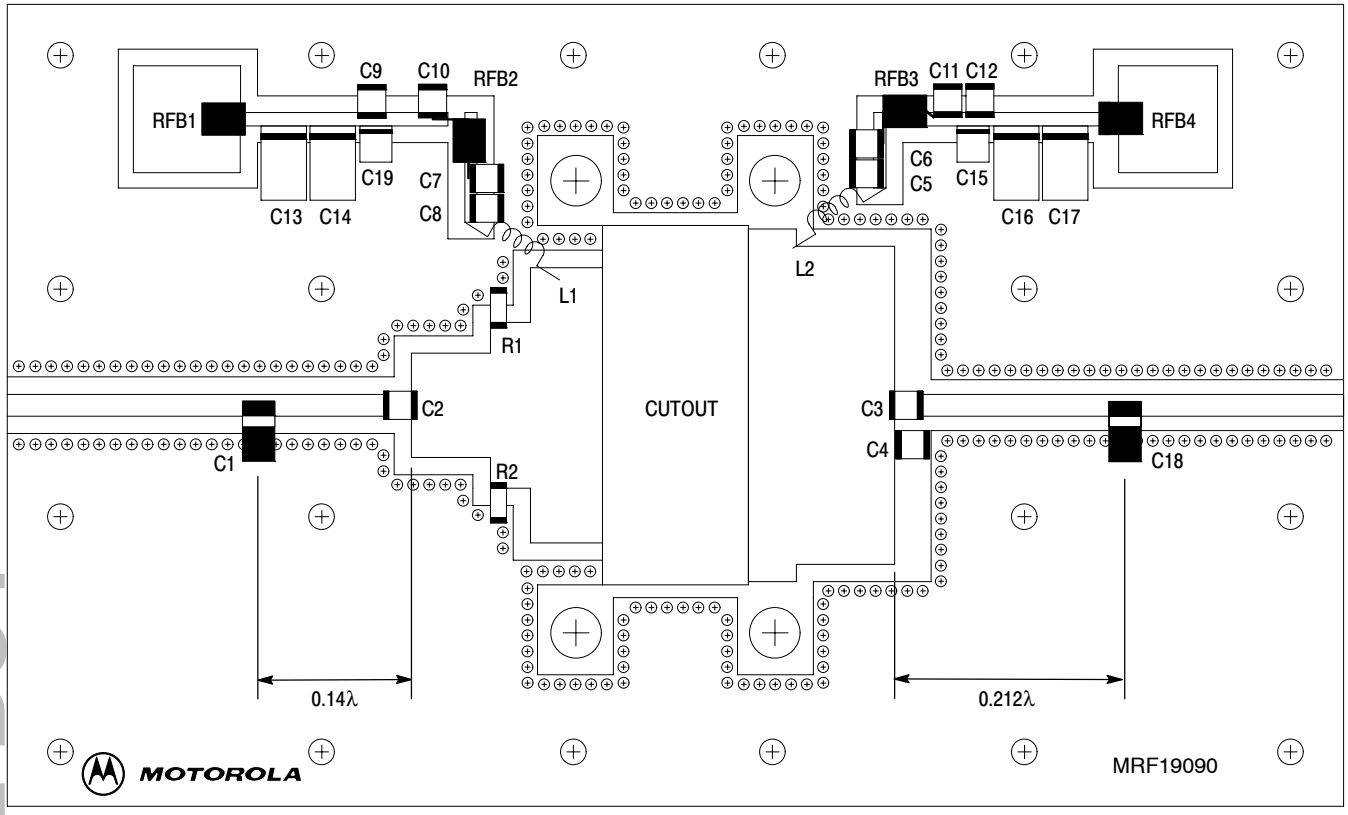
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$VGS_{(th)}$	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.8	4.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.10	—	Vdc
Dynamic Characteristics					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
Functional Tests (In Freescale Test Fixture)					
Two-Tone Common-Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz, Tone Spacing = 100 kHz)	G_{ps}	10	11.5	—	dB
Two-Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz, Tone Spacing = 100 kHz)	η	33	35	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz, Tone Spacing = 100 kHz)	IMD	—	-30	-28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 90 W PEP, I_{DQ} = 750 mA, f = 1930 MHz, Tone Spacing = 100 kHz)	IRL	—	-12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, P_{out} = 90 W CW, f = 1930 MHz)	P1dB	—	90	—	W

1. Part is internally matched both on input and output.



B1, B2	2 Ferrite Beads, Round, Ferroxcube #56-590-65-3B	L1, L2	8 Turns, #26 AWG, 0.085″ OD, 0.330″ Long, Copper Wire
B3, B34	Ferrite Beads, Surface Mount, Fair-Rite 2743019447		
C1, C18	0.4 - 2.5 pF Variable Capacitors, Johanson Gigatrim #27280	R1, R2	270 Ω, 1/4 W Chip Resistors, Garrett Instruments #RM73B2B271JT
C2, C5, C8	10 pF Chip Capacitors, ATC #100B100CT500XT		
C3	12 pF Chip Capacitor, ATC #100B120CT500XT	Z1	ZO = 50 Ohms
C4	0.3 pF Chip Capacitor, ATC #100B0R3CT500XT	Z2	ZO = 50 Ohms, Lambda = 0.123
C6, C7	120 pF Chip Capacitors, ATC #100B12R1CT500XT	Z3	ZO = 15.24 Ohms, Lambda = 0.0762
C9, C12	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKYS	Z4	ZO = 10.11 Ohms, Lambda = 0.0392
C10, C11	1000 pF Chip Capacitors, ATC #100B102JT50XT	Z5	ZO = 6.34 Ohms, Lambda = 0.0711
C13, C17	22 μF, 35 V Tantalum Chip Capacitors, Kemet #T491X226K035AT	Z6	ZO = 5.02 Ohms, Lambda = 0.0476
		Z7	ZO = 5.54 Ohms, Lambda = 0.0972
C14, C16	10 μF, 35 V Tantalum Chip Capacitors, Kemet #T495X106K035AT	Z8	ZO = 50.0 Ohms, Lambda = 0.194
		Z9	ZO = 50.0 Ohms
C15, C19	1 μF, 35 V Tantalum Chip Capacitors, Kemet #T495X105K035AT	Raw PCB Material	0.030″ Glass Teflon®, ε_r = 2.55, 2 oz Copper, 3″ x 5″ Dimensions

Figure 1. MRF19090 Test Circuit Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF19090 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

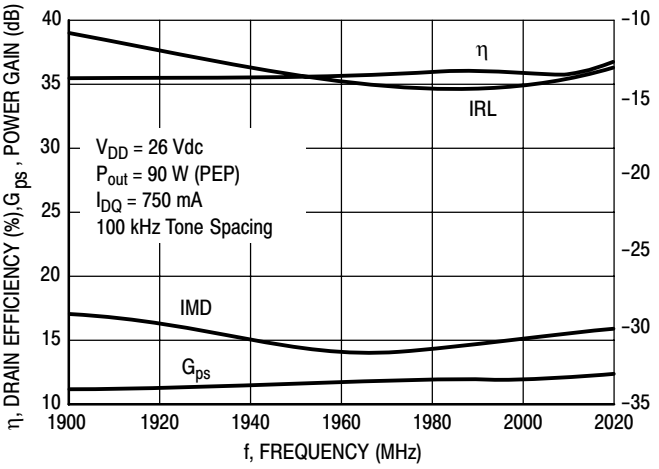


Figure 3. Class AB Performance versus Frequency

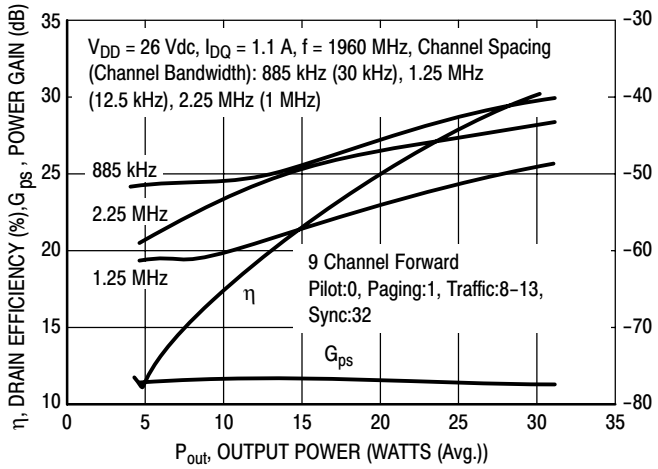


Figure 4. CDMA Performance ACPR, Gain and Drain Efficiency versus Output Power

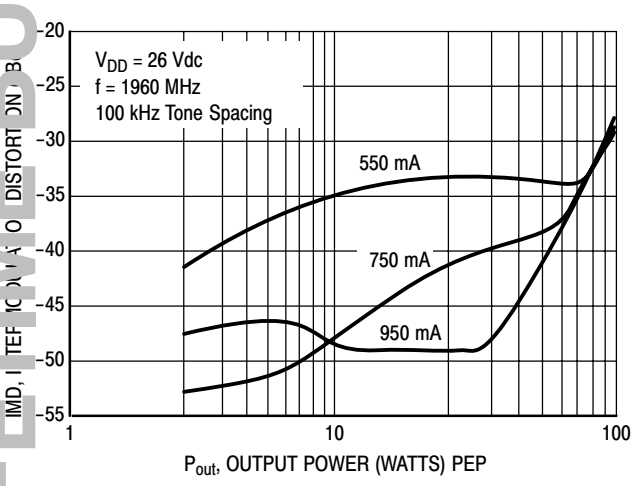


Figure 5. Third Order Intermodulation Distortion versus Output Power

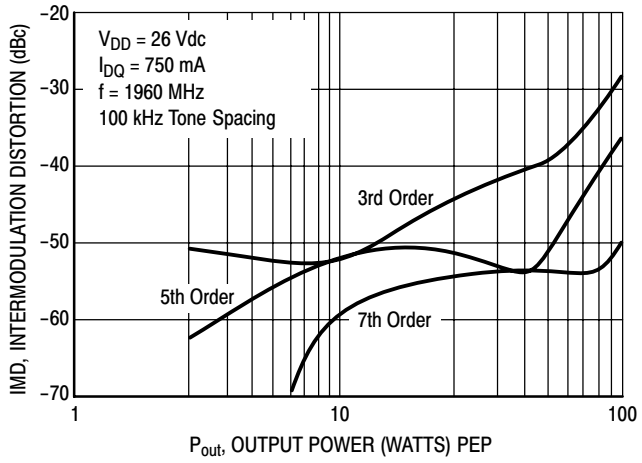


Figure 6. Intermodulation Products versus Output Power

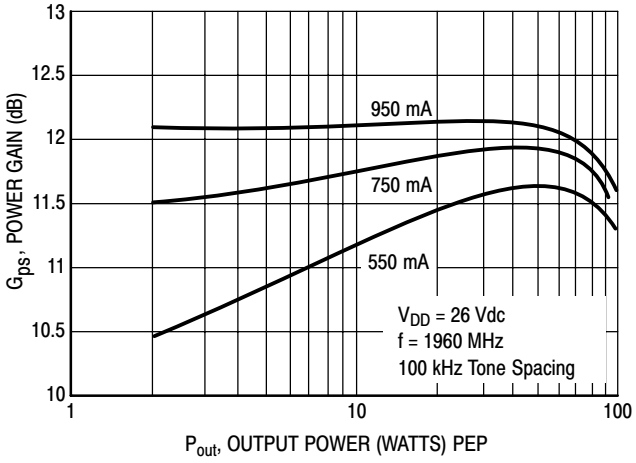


Figure 7. Power Gain versus Output Power

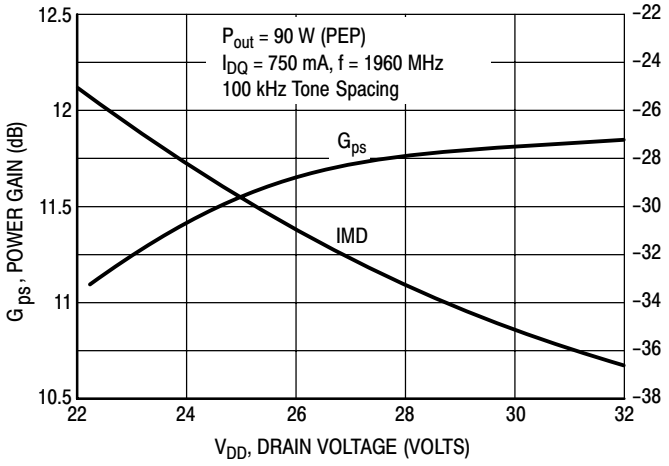
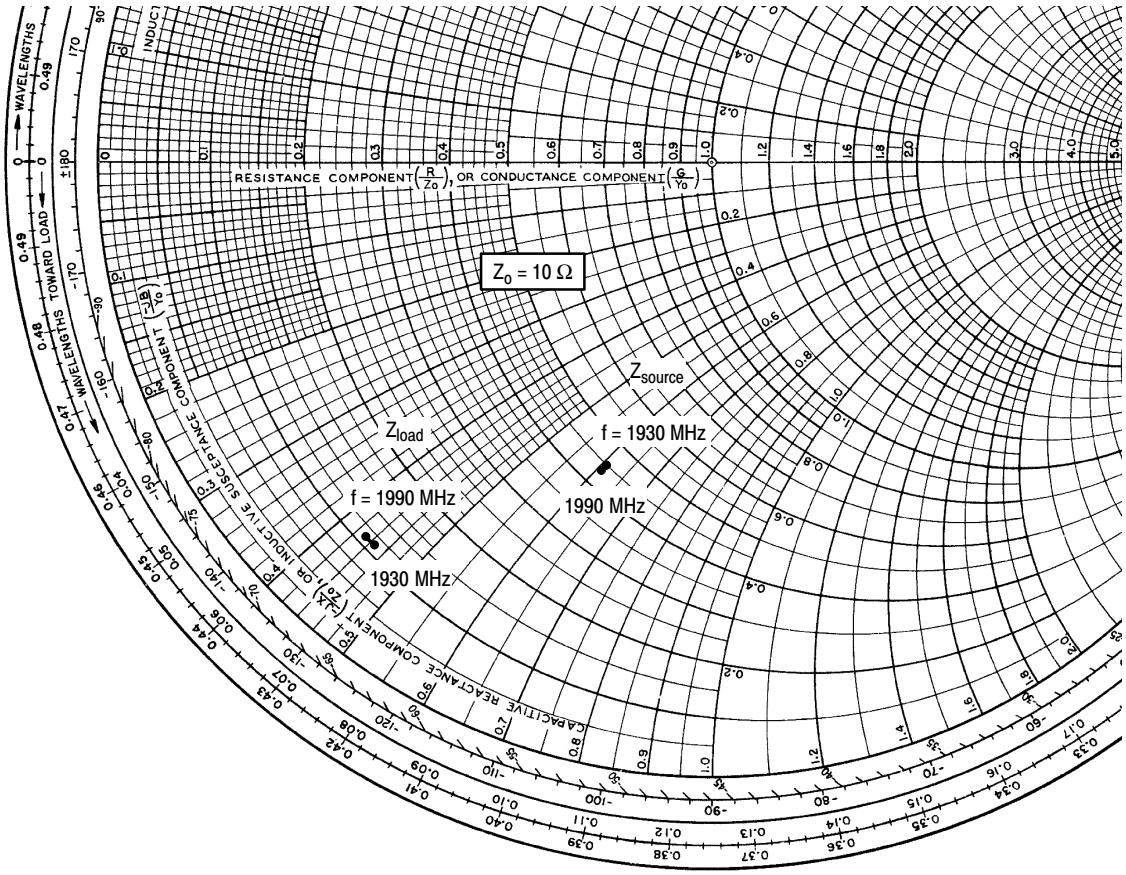


Figure 8. Third Order Intermodulation Distortion and Gain versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (PEP)

f MHz	Z_{source} Ω	Z_{load} Ω
1930	4.5 - j6.1	1.1 - j4.5
1960	4.4 - j6.0	1.1 - j4.4
1990	4.3 - j6.1	1.1 - j4.3

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

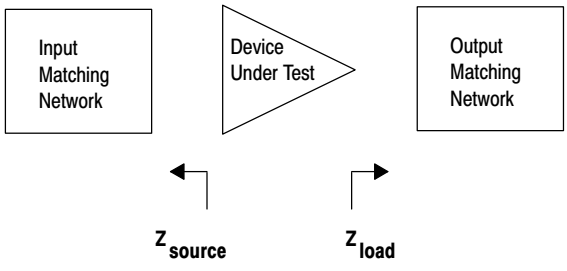
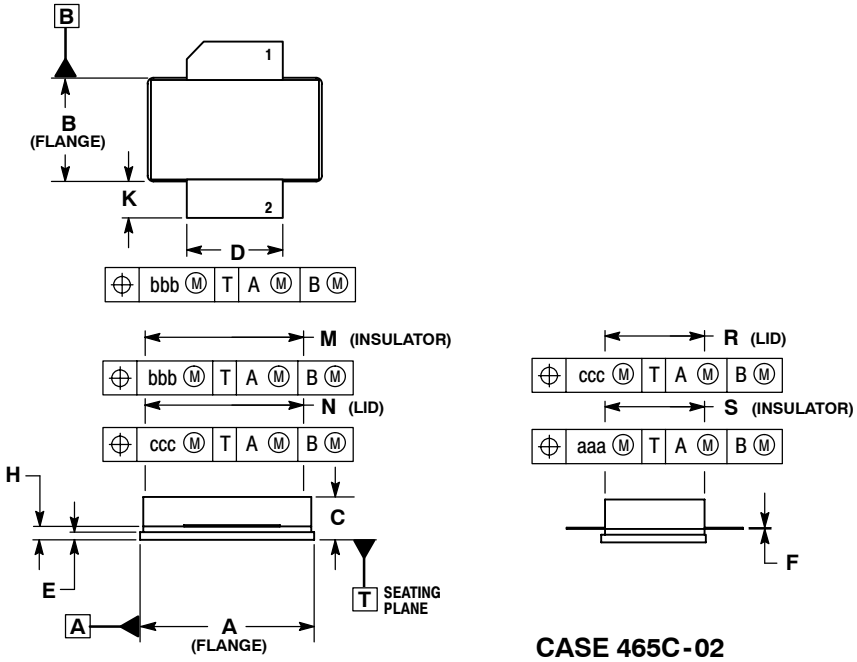


Figure 9. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



CASE 465C-02
ISSUE D
NI-880S
MRF19090SR3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.60	13.80
C	0.147	0.200	3.73	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.872	0.888	22.15	22.55
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30
S	0.515	0.525	13.10	13.30
aaa	0.007 REF		0.178 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
8	Oct. 2008	• Data sheet revised to reflect part status change, p. 1, including use of applicable overlay. • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2 • Updated Part Numbers in Figure 1, Test Circuit Schematic, to RoHS compliant part numbers, p. 3 • Added Product Documentation and Revision History, p. 8

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