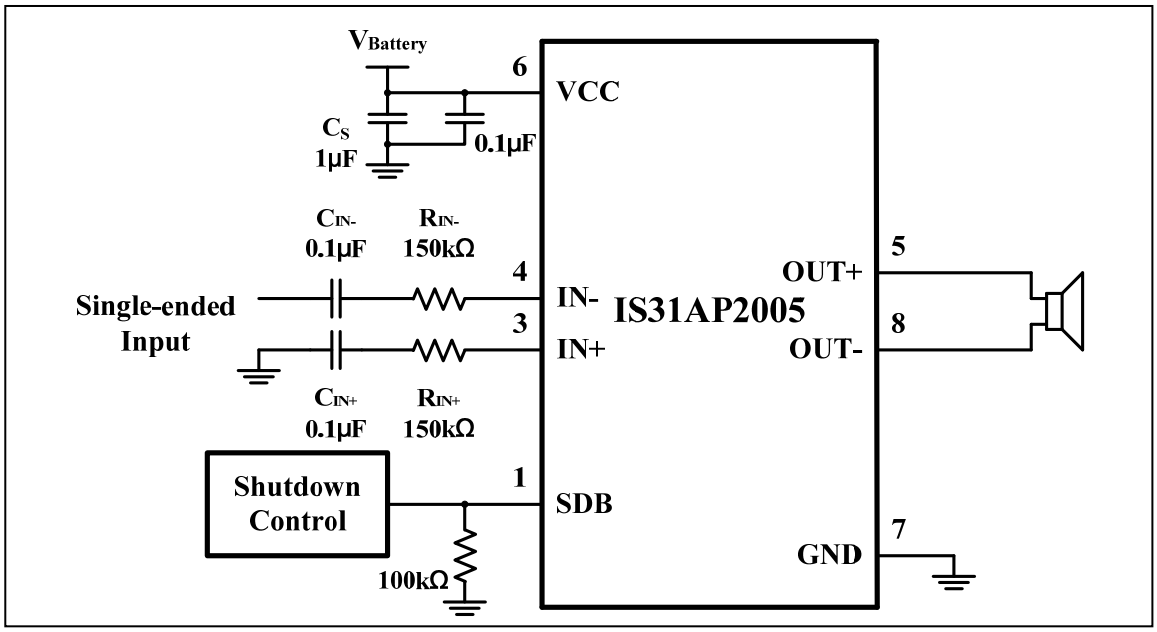
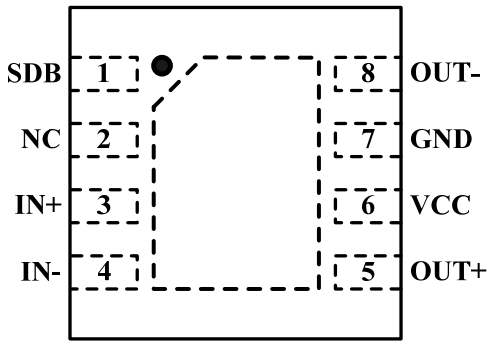
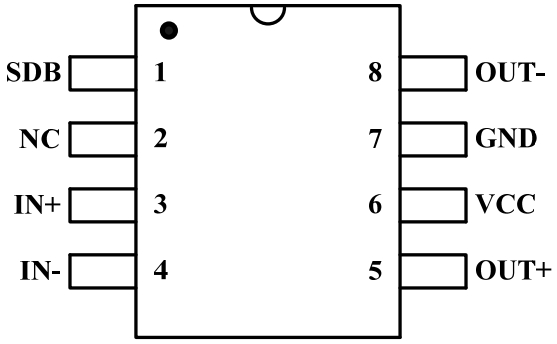


Figure 2 Typical Application Schematic with Single-ended Input

PIN CONFIGURATION

Package	Pin Configuration (Top view)
DFN-8	
MSOP-8	

PIN DESCRIPTION

No.		Pin	Description
DFN-8	MSOP-8		
1		SDB	Shutdown terminal, active low logic.
2		NC	No internal connection.
3		IN+	Positive differential input.
4		IN-	Negative differential input.
5		OUT+	Positive BTL output.
6		VCC	Power supply.
7		GND	High-current ground.
8		OUT-	Negative BTL output.
	-	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP2005-DLS2-TR	DFN-8, Lead-free	2500
IS31AP2005-SLS2-TR	MSOP-8, Lead-free	

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
Thermal resistance, θ_{JA} (DFN-8) θ_{JA} (MSOP-8)	70°C /W 211.4°C /W
ESD (HBM) ESD (CDM)	±7kV ±500V

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC}= 2.7V ~ 5.5V, T_A= 25°C, unless otherwise noted. (Note 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_{SDB}= 0V, A_V= 2V/V		10		mV
I_{CC}	Quiescent current	V_{CC}= 5.5V, no load		2.6		mA
		V_{CC}= 2.7V, no load		1.2		
I_{SD}	Shutdown current	V_{SDB}= 0.4V			1	μA
f_{SW}	Switching frequency			250		kHz
R_{IN}	Input resistor	Gain≤ 20V/V	15			kΩ
Gain	Audio input gain	R_{IN}= 150kΩ		2		V/V
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.4	V

ELECTRICAL CHARACTERISTICS

T_A= 25°C, Gain= 2V/V. (Note 2)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
P_O	Output power	THD+N= 10% f= 1kHz, R_L= 8Ω	V_{CC}= 5.0V		1.70		W
			V_{CC}= 4.2V		1.20		
			V_{CC}= 3.6V		0.83		
		THD+N= 10% f= 1kHz, R_L= 4Ω	V_{CC}= 5.0V		2.95		W
			V_{CC}= 4.2V		2.05		
			V_{CC}= 3.6V		1.55		
		THD+N= 1% f= 1kHz, R_L= 8Ω	V_{CC}= 5.0V		1.45		W
			V_{CC}= 4.2V		0.95		
			V_{CC}= 3.6V		0.66		
		THD+N= 1% f= 1kHz, R_L= 4Ω	V_{CC}= 5.0V		2.50		W
			V_{CC}= 4.2V		1.70		
			V_{CC}= 3.6V		1.25		
THD+N	Total harmonic distortion plus noise	V_{CC}= 5.0V, P_O=1.0W, R_L= 8Ω, f= 1kHz			0.28		%
		V_{CC}= 5.0V, P_O=1.2W, R_L= 4Ω, f= 1kHz			0.31		
V_{NO}	Output voltage noise	V_{CC}= 3.6V~5V, f= 20Hz to 20kHz, inputs ac-grounded with C_{IN}= 1μF A-Weighting			68		μVrms
t_{WU}	Wake-up time from shutdown	V_{CC}= 3.6V			36		ms
SNR	Signal-to-noise ratio	P_O=1.0W, R_L= 8Ω, V_{CC}= 5.0V			92		dB
PSRR	Power supply rejection ratio	V_{CC}= 3.6V ~ 5.5V, f= 217kHz			-65		dB

Note 1: All parts are production tested at T_A= 25°C. Other temperature limits are guaranteed by design.

Note 2: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

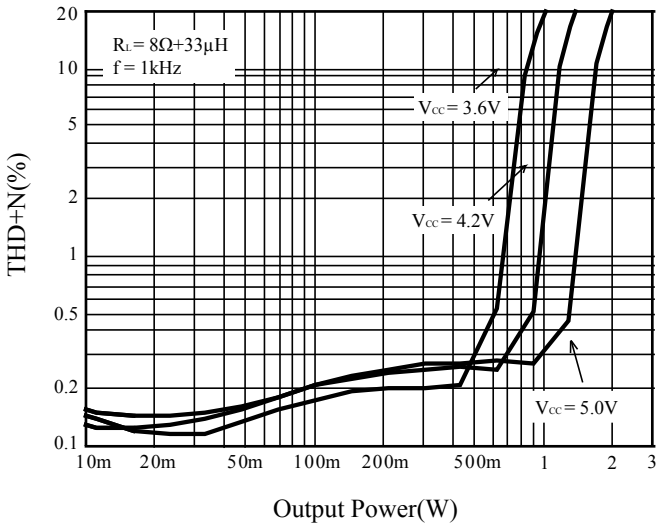


Figure 3 THD+N vs. Output Power

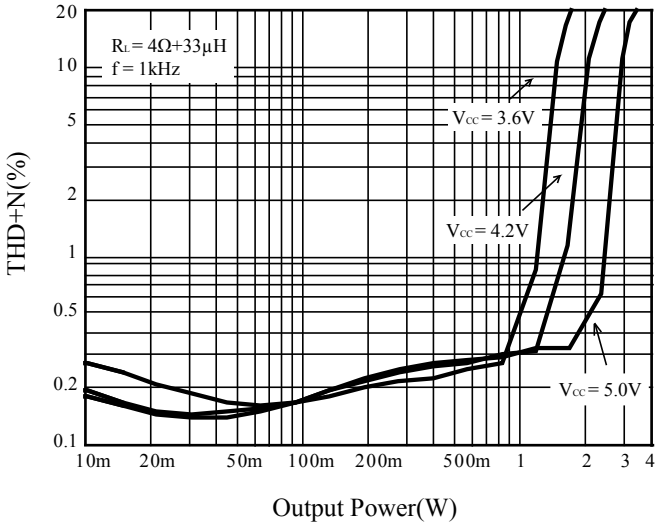


Figure 4 THD+N vs. Output Power

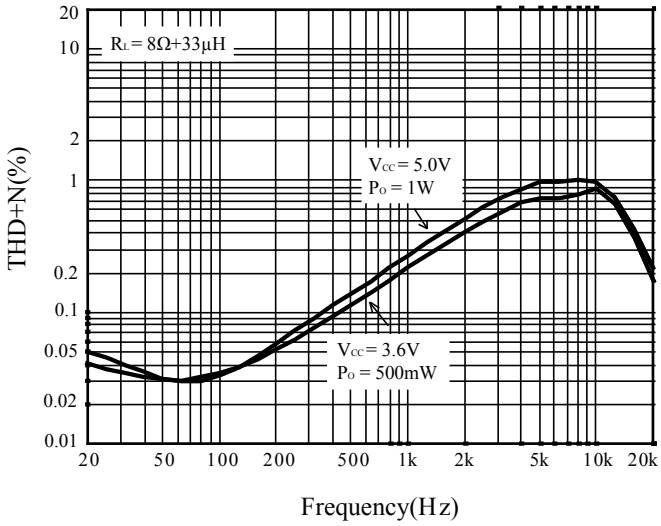


Figure 5 THD+N vs. Frequency

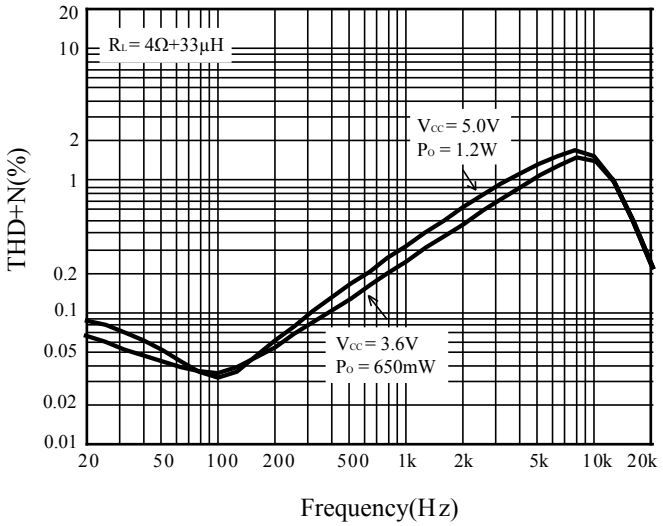


Figure 6 THD+N vs. Frequency

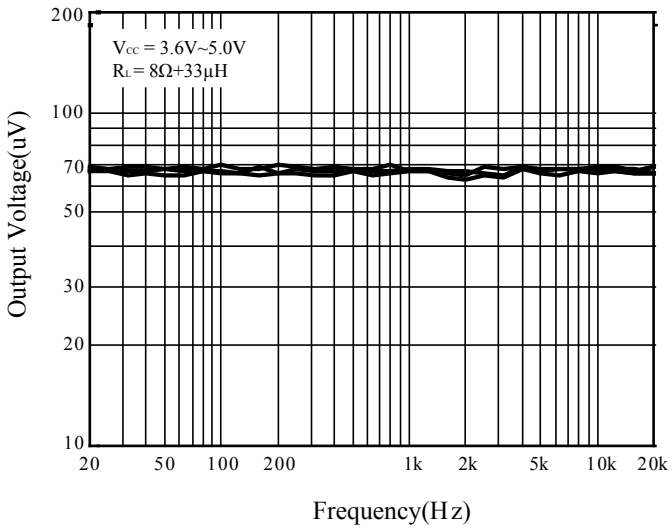


Figure 7 Noise

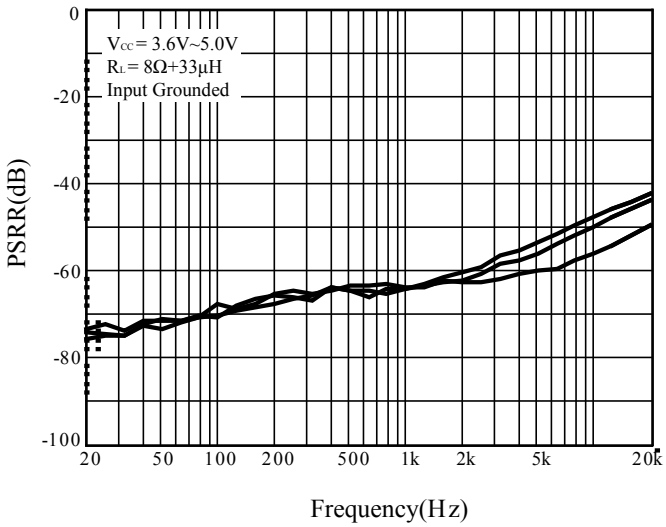


Figure 8 PSRR vs. Frequency

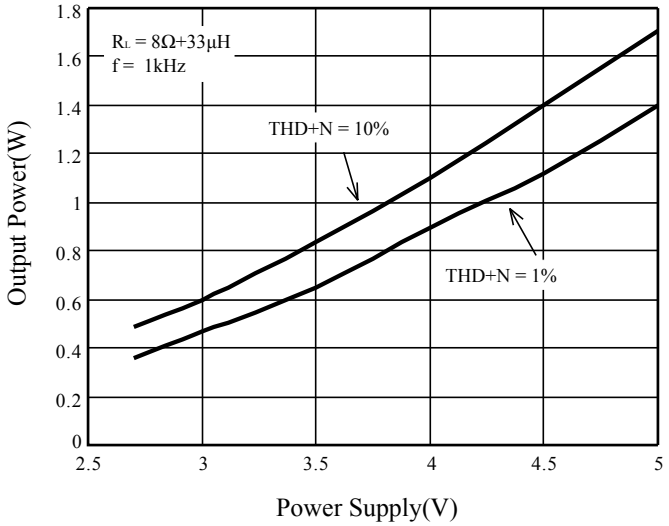


Figure 9 Output Power vs. Supply Voltage

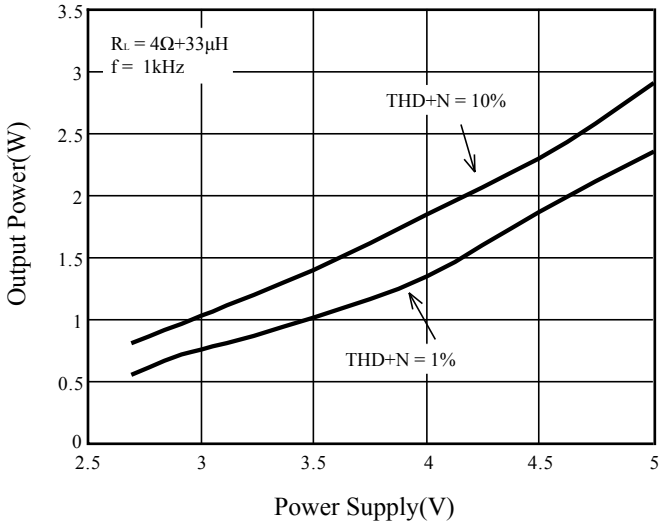


Figure 10 Output Power vs. Supply Voltage

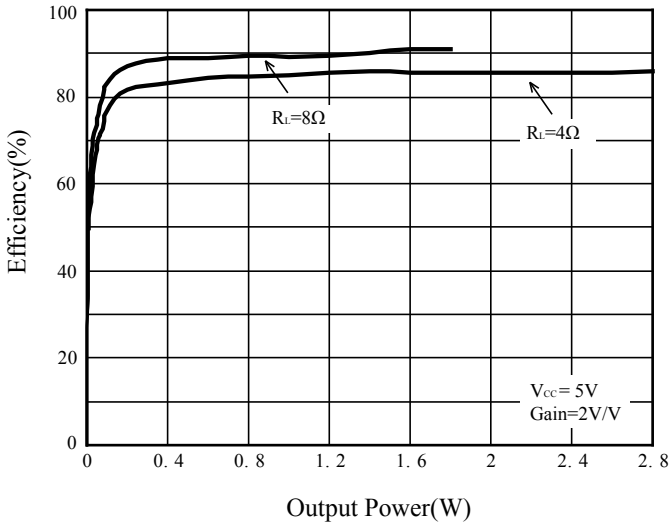
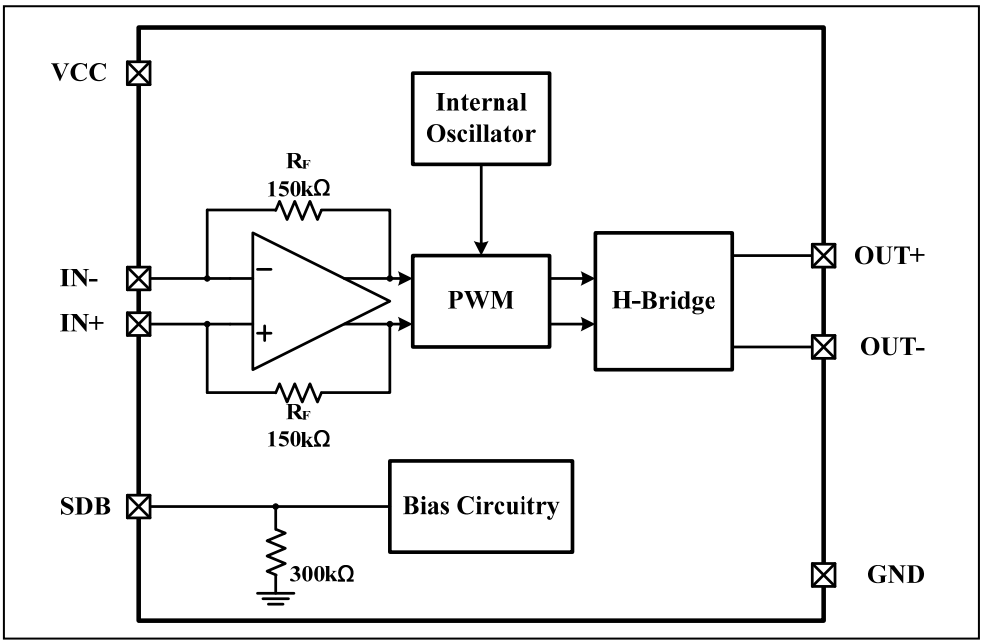


Figure 11 Efficiency vs. Output Power

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The IS31AP2005 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{CC}/2$ regardless of the common-mode voltage at the input. The fully differential IS31AP2005 can still be used with a single-ended input; however, the IS31AP2005 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

ADVANTAGES OF FULLY DIFFERENTIAL AMPLIFIERS

The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.

GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

COMPONENT SELECTION

Figure 12 shows the IS31AP2005 with differential inputs and optional input capacitors. Input capacitors are used when the common mode input voltage range specs can not be guaranteed or high pass filter is considered.

Figure 13 shows the IS31AP2005 with single-ended inputs. The input capacitors have to be used in the single ended case because it is much more susceptible to noise in this case.

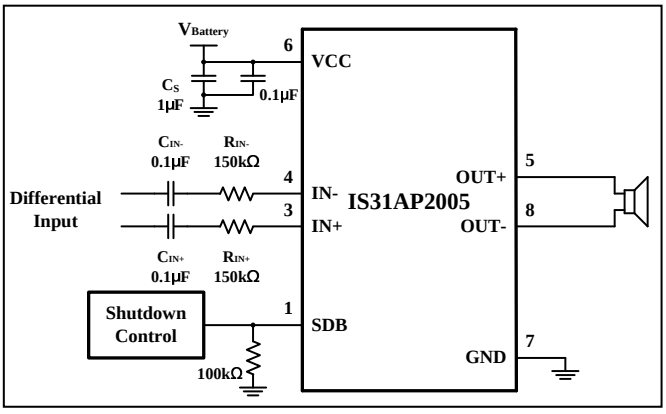


Figure 12 Typical Application Circuit with Differential Input

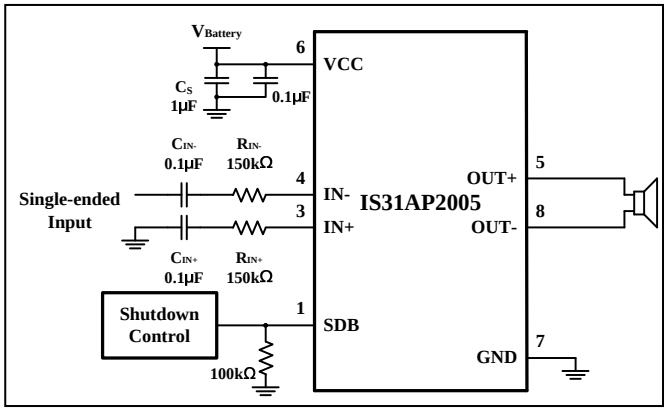


Figure 13 Typical Application Circuit with Single-Ended Input

INPUT RESISTORS (R_{IN})

The input resistors (R_{IN}) set the gain of the amplifier according to Equation (1).

$$Gain = \frac{2 \times 150k\Omega}{R_{IN}} \left(\frac{V}{V}\right) \qquad (1)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% accuracy resistors or better to keep the performance optimized. Matching is more important than overall accuracy.

Place the input resistors close to the IS31AP2005 to reduce noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2V/V or lower. Lower gain allows the IS31AP2005 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

DECOUPLING CAPACITOR (C_S)

The IS31AP2005 is a high-performance Class-D audio amplifier that requires adequate power supply decoupling to ensure high efficiency and low total harmonic distortion (THD). For higher frequency transients, spikes, or digital noises on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{CC} pin works best. Placing this decoupling capacitor close to the IS31AP2005 is also important for the efficiency of the Class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also be helpful, but it is not required in most applications because of better PSRR of this device.

INPUT CAPACITORS (C_{IN})

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_C, determined in Equation (2).

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \qquad (2)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_{IN} = \frac{1}{2\pi R_{IN} f_C} \qquad (3)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For a flat low-frequency response, use large input coupling capacitors (1μF). However, in a GSM phone the ground signal is fluctuating at 217Hz, but the signal from the codec does not have the same 217Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217Hz hum.

SUMMING INPUT SIGNALS

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The IS31AP2005 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

SUMMING TWO DIFFERENTIAL INPUT SIGNALS

Two extra resistors are needed for summing differential signals (Figure 14). The gain for each input source can be set independently by Equations (4) and (5).

$$Gain1 = \frac{V_O}{V_{IN1}} = \frac{2 \times 150k\Omega}{R_{IN1}} \left(\frac{V}{V}\right) \qquad (4)$$

$$Gain2 = \frac{V_O}{V_{IN2}} = \frac{2 \times 150k\Omega}{R_{IN2}} \left(\frac{V}{V}\right) \qquad (5)$$

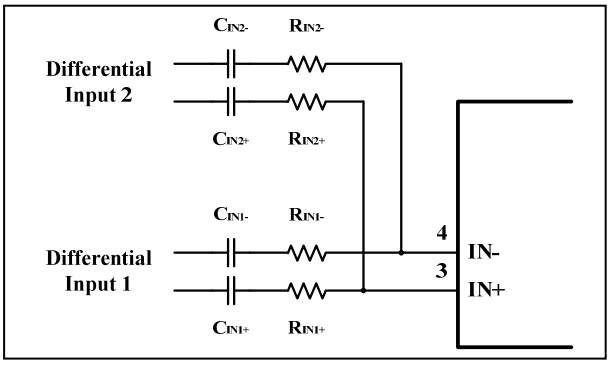


Figure 14 Application Circuit with Summing Two Differential Inputs

If summing left and right inputs with a gain of 1V/V, use R_{IN1}= R_{IN2}= 300kΩ.

If summing a ring tone and a phone signal, set the ring-tone gain to Gain2= 2V/V, and the phone gain to Gain1= 0.1V/V. The resistor values would be.

R_{IN1}= 3MΩ, and R_{IN2}= 150kΩ.

SUMMING A DIFFERENTIAL INPUT SIGNAL AND A SINGLE-ENDED INPUT SIGNAL

Figure 15 shows how to sum a differential input signal and a single-ended input signal. Ground noise may couple in through IN- with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{IN2}, shown in Equation (6). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use. The gain for each input source can be set independently by Equations (4) and (5).

$$C_{IN2} = \frac{1}{2\pi R_{IN2} f_{C2}} \qquad (6)$$

If summing a ring tone and phone signals, the phone signals should use the differential inputs while the ring tone should use the single-ended input. The phone gain is set at Gain1= 0.1V/V, and the ring-tone gain is set to Gain2= 2V/V, the resistor values would be

R_{IN1}= 3MΩ, and R_{IN2}= 150kΩ.

The high pass corner frequency of the single-ended input is set by C_{IN2}. If the desired corner frequency is less than 20Hz.

$$C_{IN2} > \frac{1}{2\pi 150k\Omega \times 20Hz} \qquad (7)$$

$$C_{IN2} > 53pF \qquad (8)$$

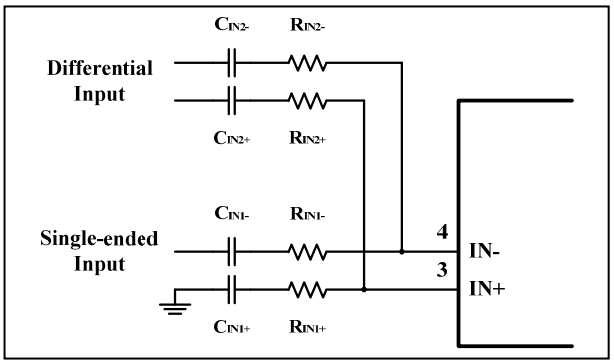


Figure 15 Application Circuit with Summing Differential Input and Single-Ended Input Signals

SUMMING TWO SINGLE-ENDED INPUT SIGNALS

The corner frequencies (f_{C1} and f_{C2}) for each input source can be set independently by Equations (9) and (10). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN- terminal (Figure 16). The gain for each input source can be set independently by Equations (4) and (5).

The single-ended inputs must be driven by low impedance sources.

$$C_{IN1} = \frac{1}{2\pi R_{IN1} f_{C1}} \qquad (9)$$

$$C_{IN2} = \frac{1}{2\pi R_{IN2} f_{C2}} \qquad (10)$$

$$C_P = C_{IN1} + C_{IN2} \qquad (11)$$

$$R_P = \frac{R_{IN1} \times R_{IN2}}{R_{IN1} + R_{IN2}} \qquad (12)$$

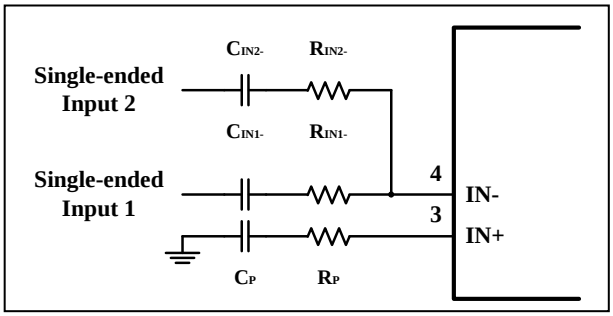


Figure 16 Application Circuit with Summing Two Single-Ended Inputs

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

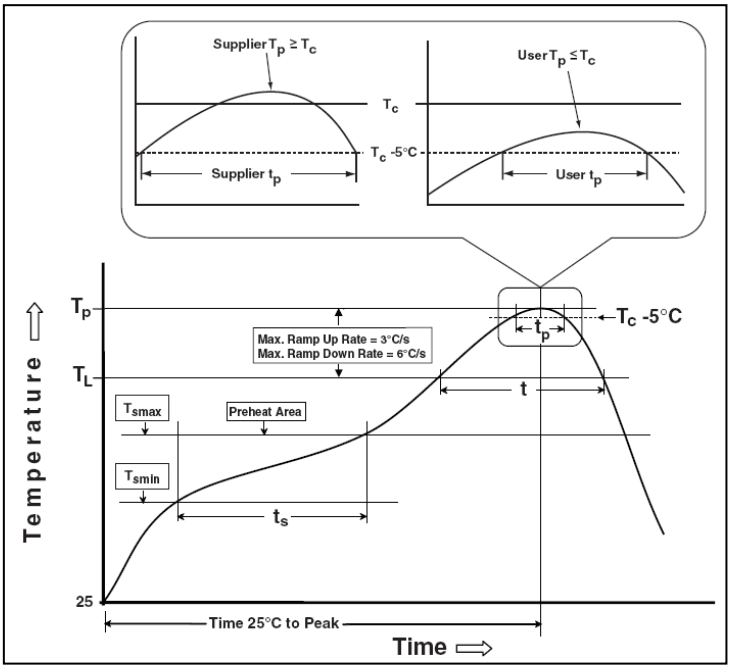
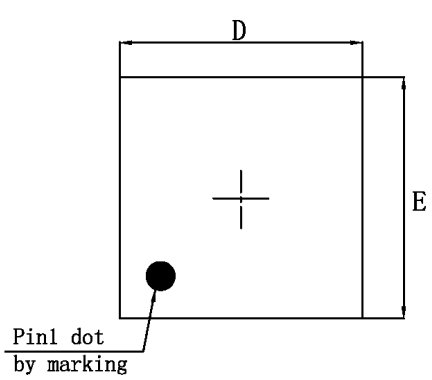


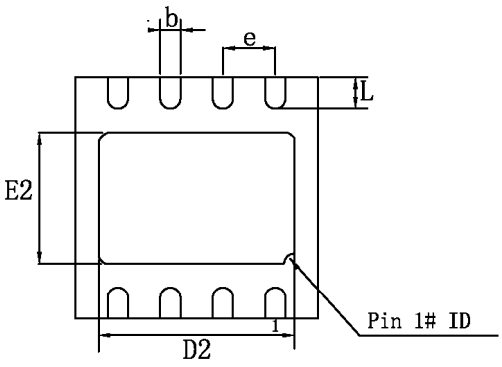
Figure 17 Classification Profile

PACKAGING INFORMATION

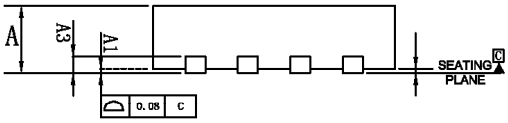
DFN-8



Top View



Bottom View

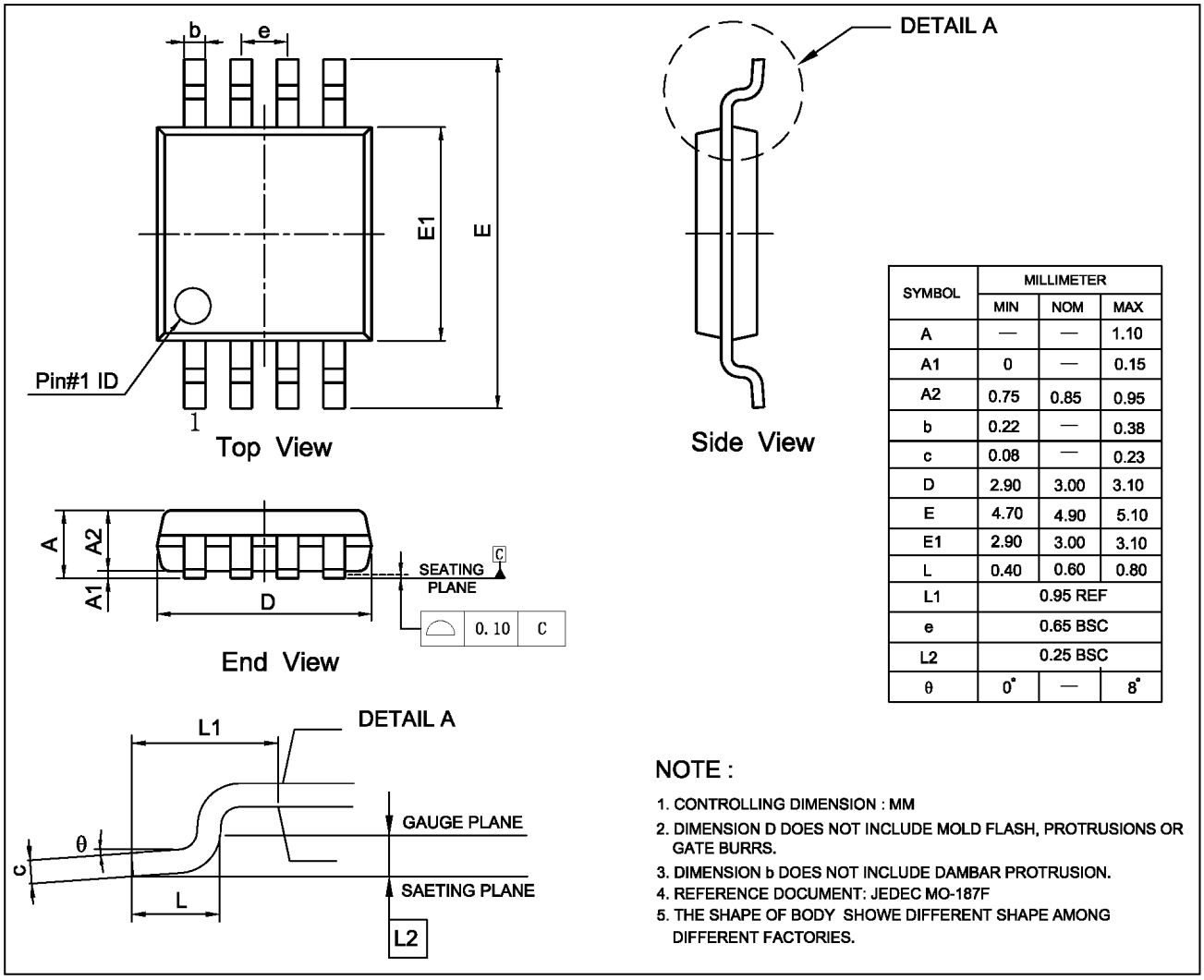


Side View

NOTES:
The thermal pad shows different shape among different factories.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E2	1.35	—	1.75
D2	2.15	—	2.55
b	0.17	—	0.35
L	0.30	0.40	0.575
e	0.65 BSC		

MSOP-8



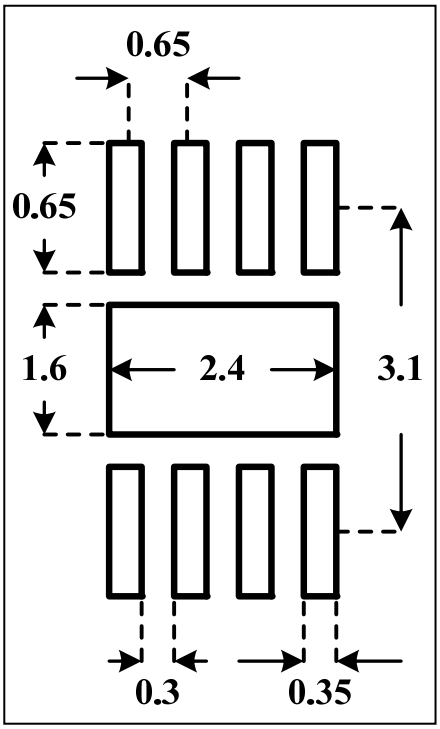
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.75	0.85	0.95
b	0.22	—	0.38
c	0.08	—	0.23
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
L	0.40	0.60	0.80
L1	0.95 REF		
e	0.65 BSC		
L2	0.25 BSC		
θ	0°	—	8°

NOTE :

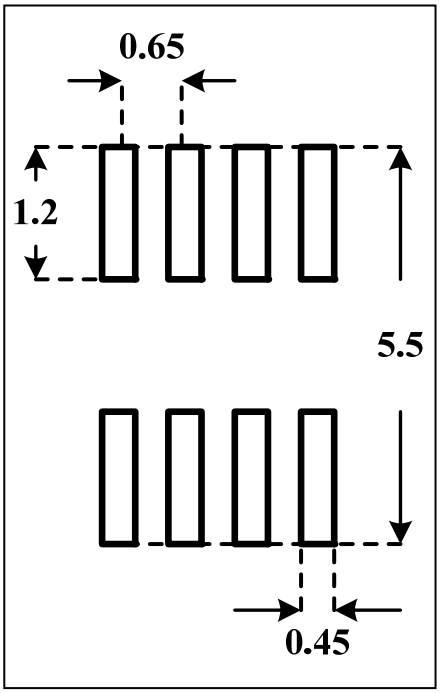
1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MO-187F
5. THE SHAPE OF BODY SHOWE DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN

DFN-8



MSOP-8



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2011.07.06
B	1. P.1 Add short-circuit and thermal protect 2. P.7-8 Update PSRR and efficiency figures 3. Add function block 4. POD should use GOODARK	2012.12.11
C	1. Add ESD(CDM) 2. Add SOP-8 package 2. Add land pattern	2015.08.31
D	1. Remove SOP-8 package information 2. Add θ_{JA}	2017.06.02

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