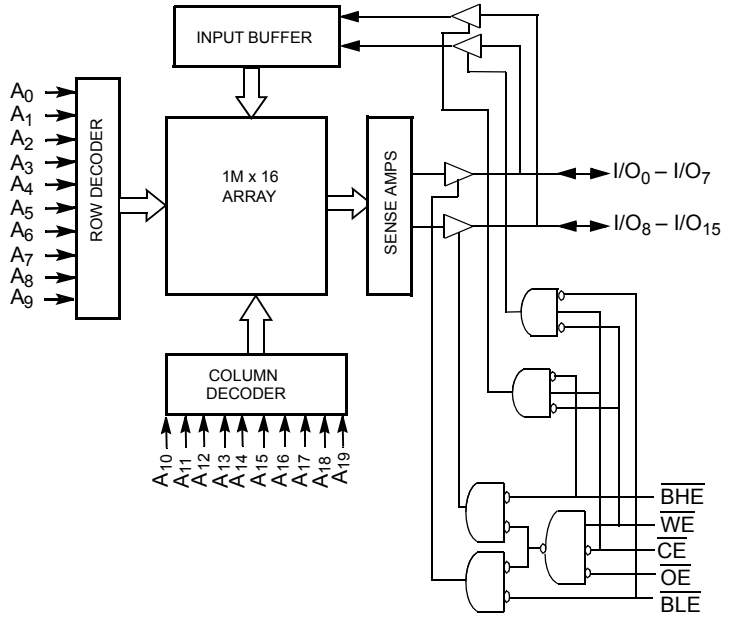
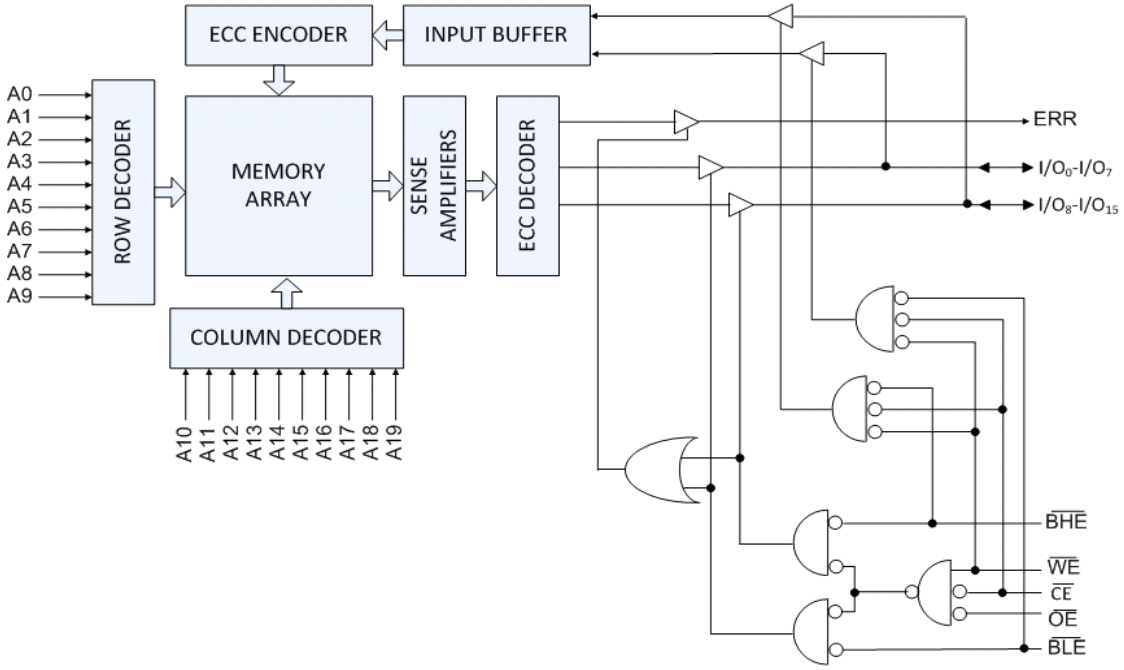
Logic Block Diagram – CY7C10612G



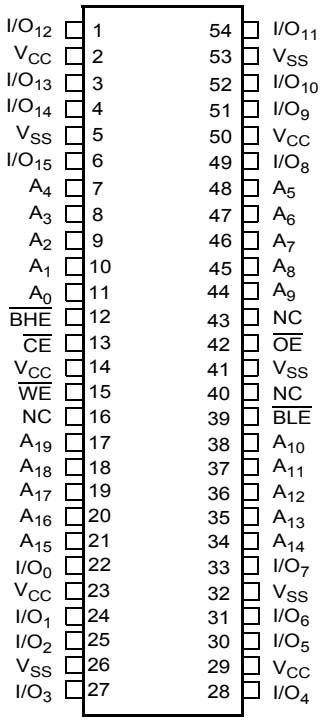
Logic Block Diagram – CY7C10612GE



Contents

Pin Configurations

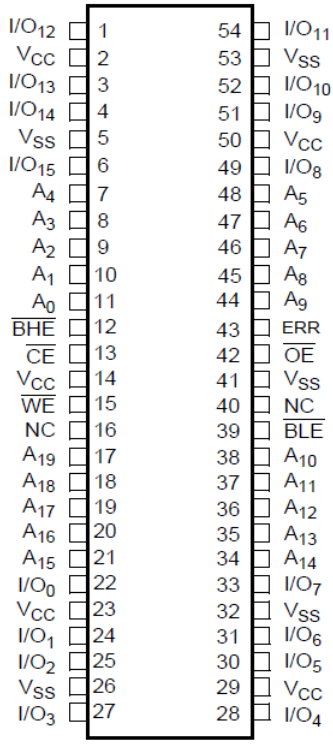
Figure 1. 54-pin TSOP II pinout (Top View) [1]
CY7C10612G



Note
1. NC pins are not connected on the die.

Pin Configurations (continued)

Figure 2. 54-pin TSOP II pinout with ERR (Top View) [2, 3]
CY7C10612GE



Note
2. NC pins are not connected on the die.
3. ERR is an Output pin. If not used, this pin should be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND[4] ..... –0.5 V to V_{CC} + 0.5 V

DC Voltage Applied to Outputs in High Z State[4] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage[4] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description		Test Conditions		10 ns			Unit
					Min	Typ [5]	Max	
V_{OH}	Output HIGH Voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	V
		2.7 V to 3.0 V	V_{CC} = Min, I_{OH} = –4.0 mA		2.4	–	–	
V_{OL}	Output LOW Voltage		V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	V
V_{IH}[4]	Input HIGH Voltage		–		2.0	–	V_{CC} + 0.3	V
V_{IL}[4]	Input LOW Voltage		–		–0.3	–	0.8	V
I_{IX}	Input Leakage Current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output Leakage Current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	µA
I_{CC}	Operating Supply Current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
				f = 66.7 MHz	–	70.0	80.0	mA
I_{SB1}	Automatic CE Power-down Current – TTL Inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{IH} [5], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	mA
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs		Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V [5], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0	30.0	mA

Notes

4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
5. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Capacitance

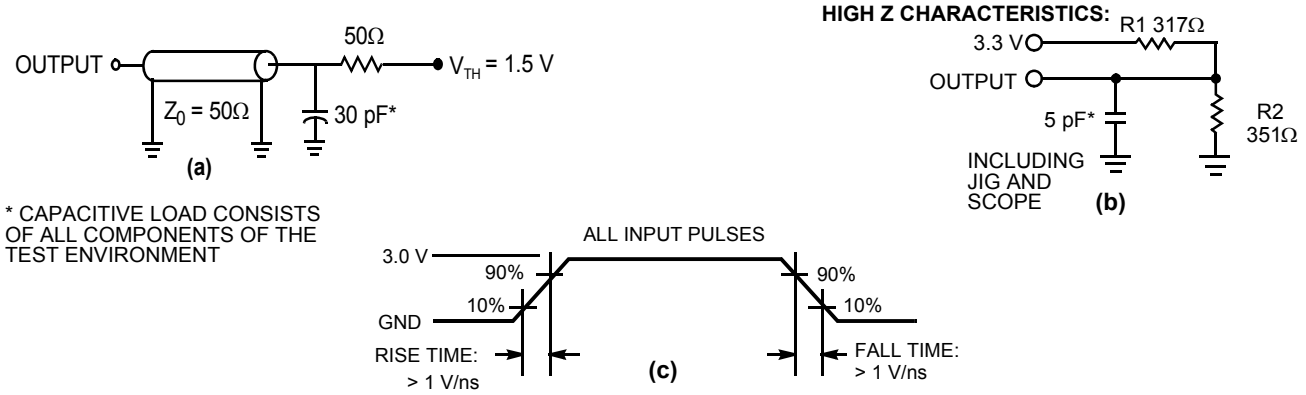
Parameter [6]	Description	Test Conditions	54-pin TSOP II	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	pF
C_{OUT}	I/O Capacitance			

Thermal Resistance

Parameter [6]	Description	Test Conditions	54-pin TSOP II	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	93.63	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		21.58	

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 100-µs wait time after V_{CC} stabilizes to its operational value.

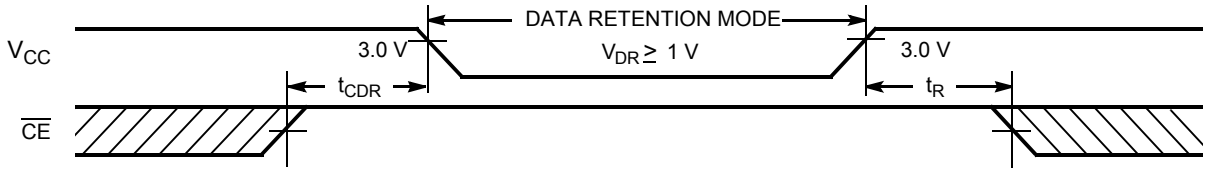
Data Retention Characteristics

Over the Operating Range –45 °C to 85 °C

Parameter	Description	Conditions	Min	Typ [8]	Max	Unit
V_{DR}	V_{CC} for Data Retention	–	1.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	30.0	mA
t_{CDR}[9]	Chip Deselect to Data Retention Time	–	0.0	–	–	ns
t_R[9, 10]	Operation Recovery Time	–	10.0	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
9. This parameter is guaranteed by design and is not tested.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

AC Switching Characteristics

Over the Operating Range

Parameter [11]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{POWER}	V_{CC} to the first access [12]	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data valid	–	10.0	ns
t_{OHA}	Data hold from address change	3.0	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5.0	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [13, 14, 15]	0.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [13, 14, 15]	–	5.0	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [13, 14, 15]	3.0	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [13, 14, 15]	–	5.0	ns
t_{PU}	$\overline{CE}$ LOW to power-up [16]	0.0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down [16]	–	10.0	ns
t_{DBE}	Byte enable to data valid	–	5.0	ns
t_{LZBE}	Byte enable to low Z	1.0	–	ns
t_{HZBE}	Byte disable to high Z	–	6.0	ns
Write Cycle [17, 18]				
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7.0	–	ns
t_{AW}	Address setup to write end	7.0	–	ns
t_{HA}	Address hold from write end	0.0	–	ns
t_{SA}	Address setup to write start	0.0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	ns
t_{SD}	Data setup to write end	5.0	–	ns
t_{HD}	Data hold from write end	0.0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [13, 14, 15]	3.0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [13, 14, 15]	–	5.0	ns
t_{BW}	Byte enable to end of write	7.0	–	ns

Notes

11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of Figure 3 on page 7, unless specified otherwise.
12. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
13. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} , t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 7. Transition is measured ±200 mV from steady state voltage.
14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
15. Tested initially and after any design or process changes that may affect these parameters.
16. These parameters are guaranteed by design and are not tested.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. Chip enable must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) for CY7C10612G [19, 20]

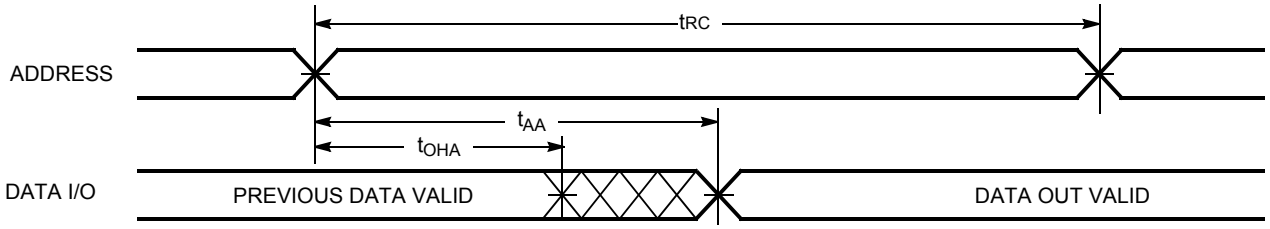
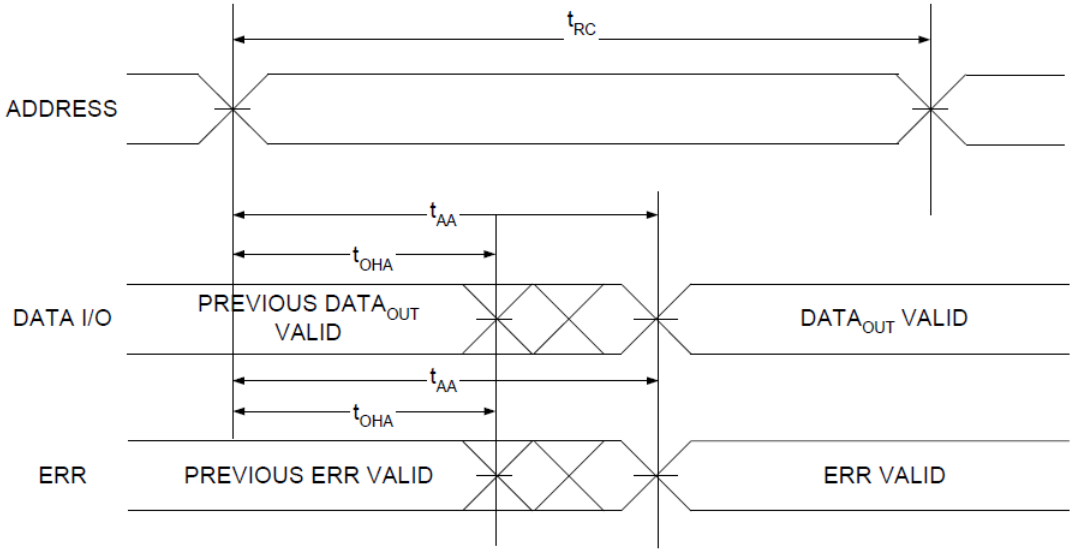


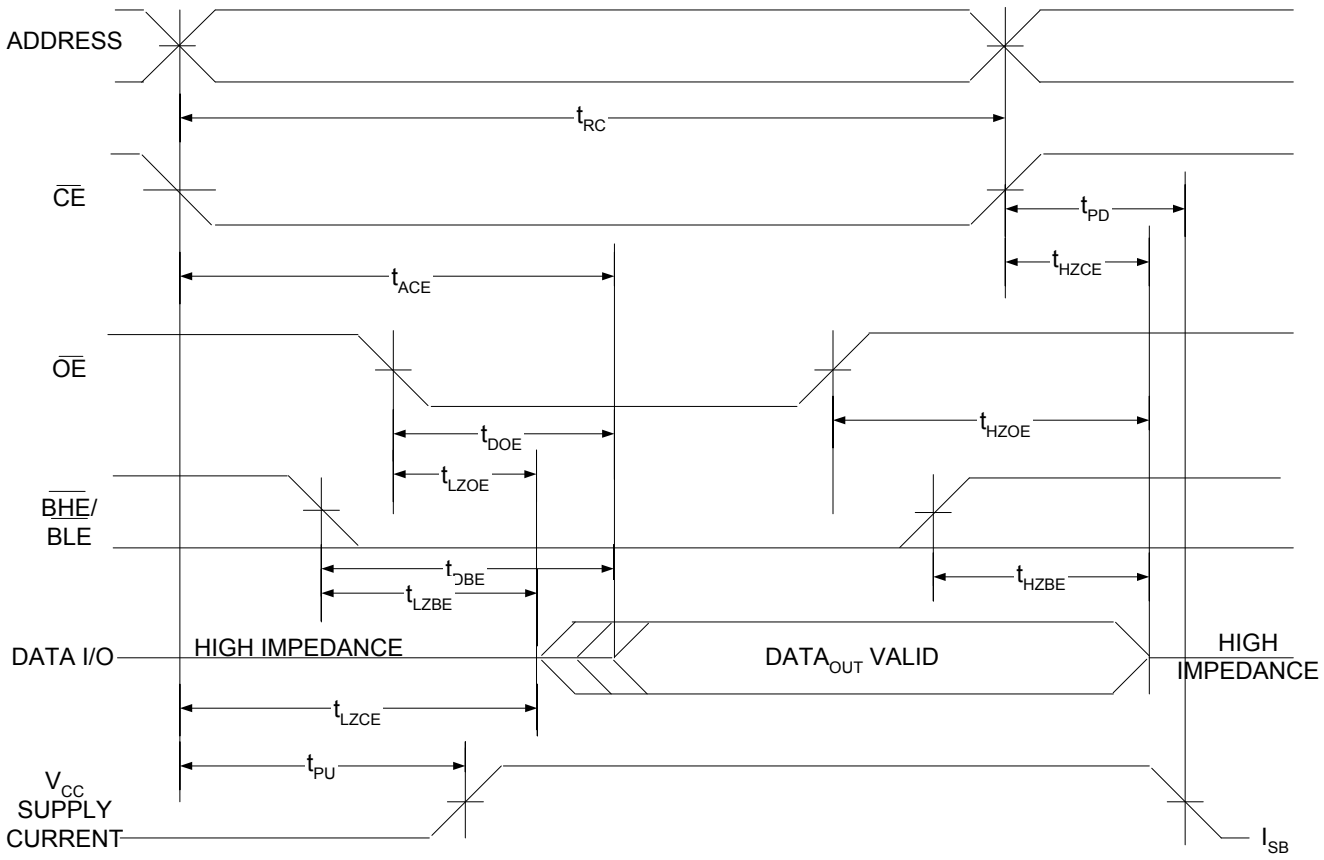
Figure 6. Read Cycle No. 1 (Address Transition Controlled) for CY7C10612GE [20, 21]



Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 (OE Controlled) [22, 23]



Notes
22. WE is HIGH for read cycle.
23. Address valid before or similar to CE transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{CE}$ Controlled) [24, 25, 26]

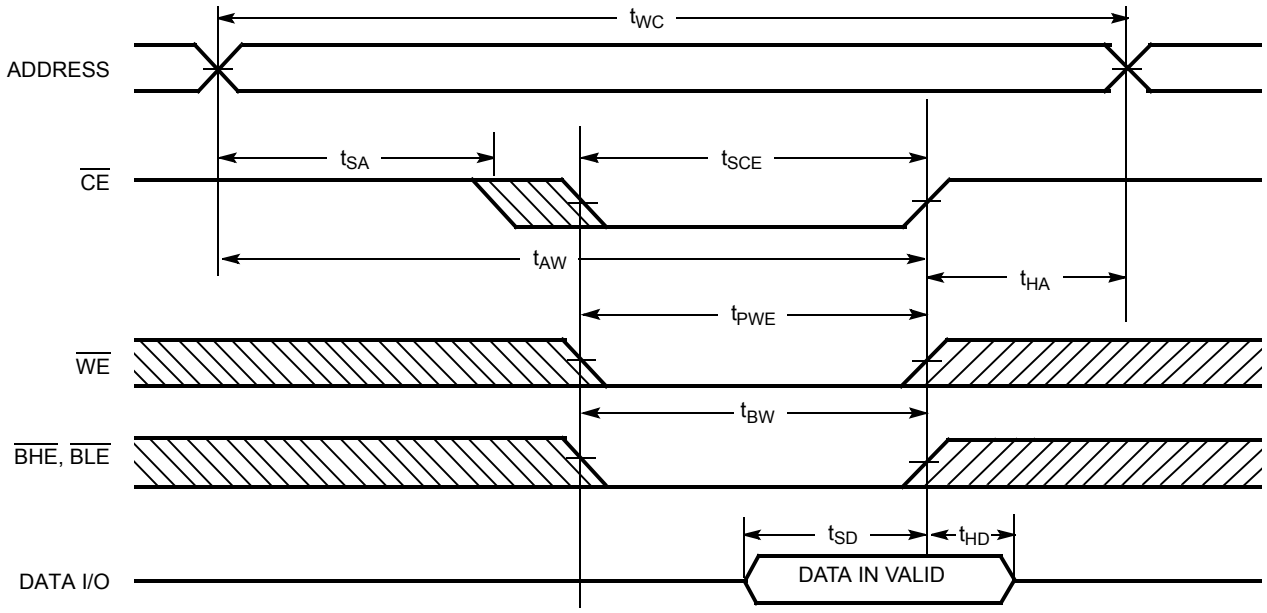
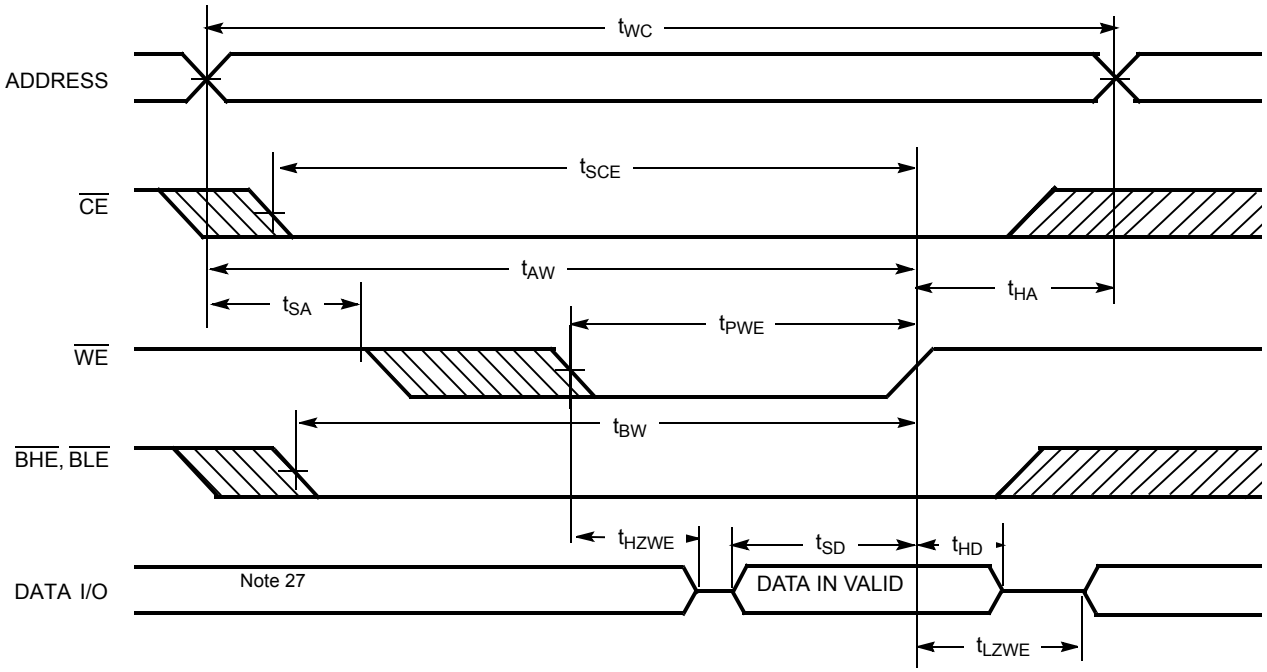


Figure 9. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [24, 25, 26]

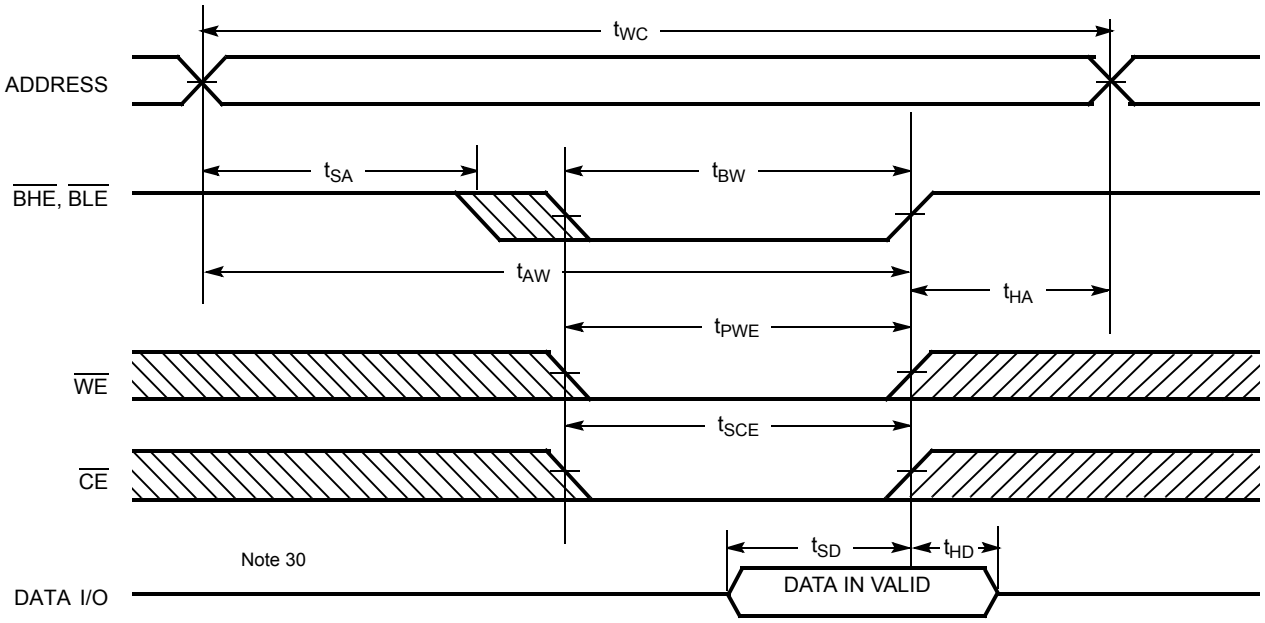


Notes

24. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.
27. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 (BLE or BHE Controlled) [28, 29]



Notes

28. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
30. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write all bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7C10612GE

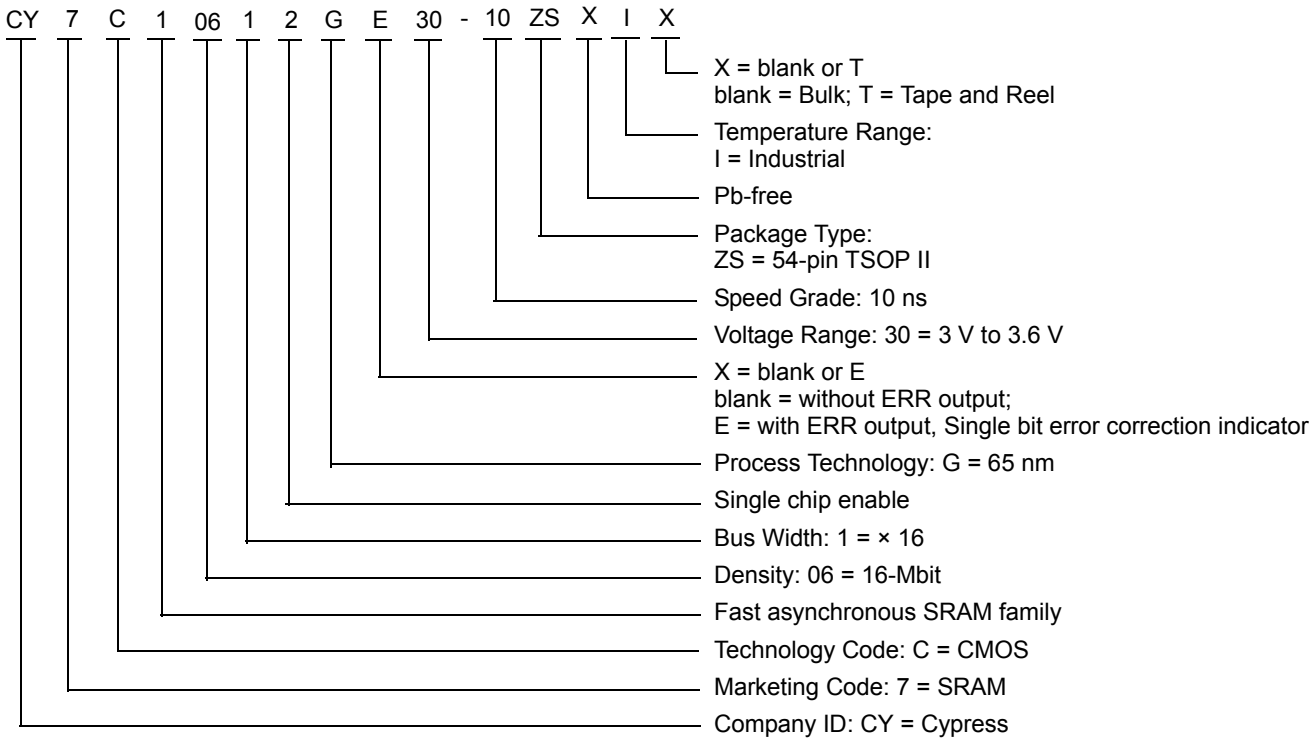
Output[31]	Mode
0	Read Operation, no error in the stored data.
1	Read Operation, single-bit error detected and corrected.
High-Z	Device deselected or Outputs disabled or Write Operation.

Note
31. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

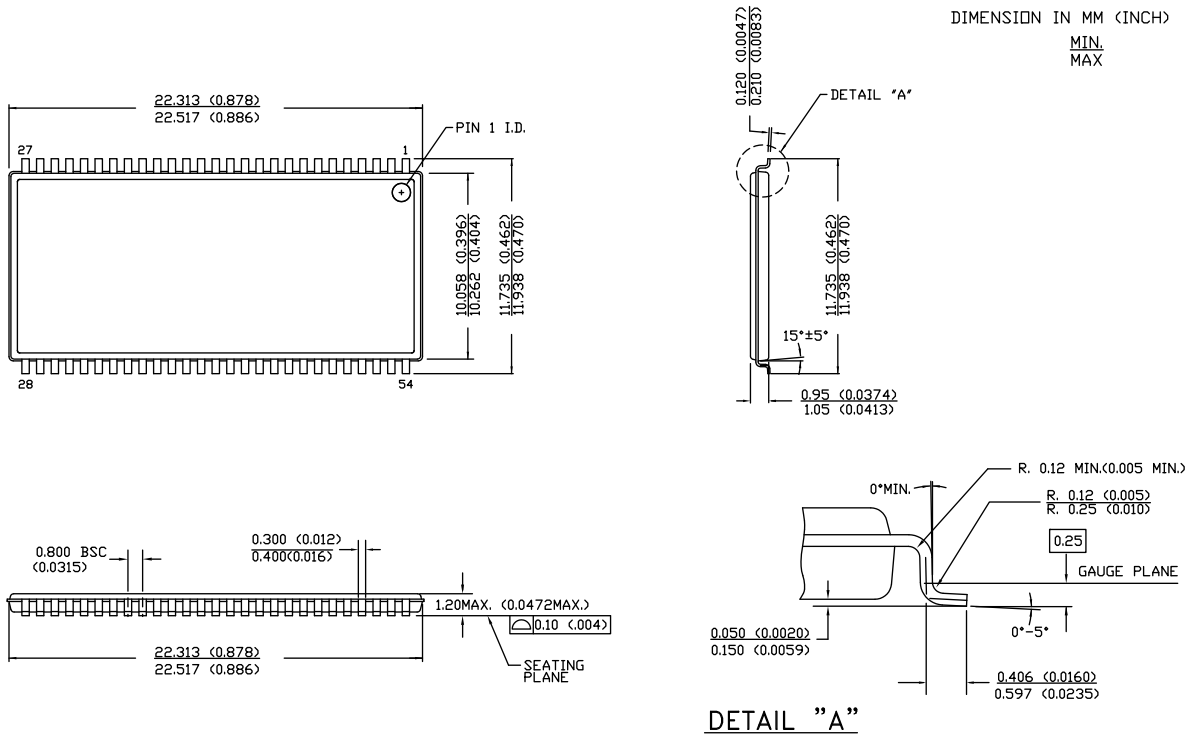
Speed (ns)	Ordering Code	Package Diagram	Package Type (Pb-free)	Operating Range
10	CY7C10612G30-10ZSXI	51-85160	54-pin TSOP II	Industrial
	CY7C10612G30-10ZSXIT		54-pin TSOP II, Tape and Reel	
	CY7C10612GE30-10ZSXI		54-pin TSOP II, with ERR Pin	
	CY7C10612GE30-10ZSXIT		54-pin TSOP II, with ERR Pin, Tape and Reel	

Ordering Code Definitions



Package Diagrams

Figure 11. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C10612G/CY7C10612GE, 16-Mbit (1M × 16) Static RAM Document Number: 001-88702				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	4865557	NILE	07/31/2015	Changed status from Preliminary to Final.
*E	5437839	NILE	09/15/2016	Updated Maximum Ratings: Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Removed all values corresponding to V_{OH} parameter. Included Operating Ranges “2.2 V to 2.7 V” and “2.7 V to 3.0 V” and all values corresponding to V_{OH} parameter. Updated Ordering Information: Updated part numbers. Updated Ordering Code Definitions. Updated to new template. Completing Sunset Review.
*F	6011828	AESATMP8	01/03/2018	Updated logo and Copyright.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor:

CY7C10612G30-10ZSXI CY7C10612G30-10ZSXIT