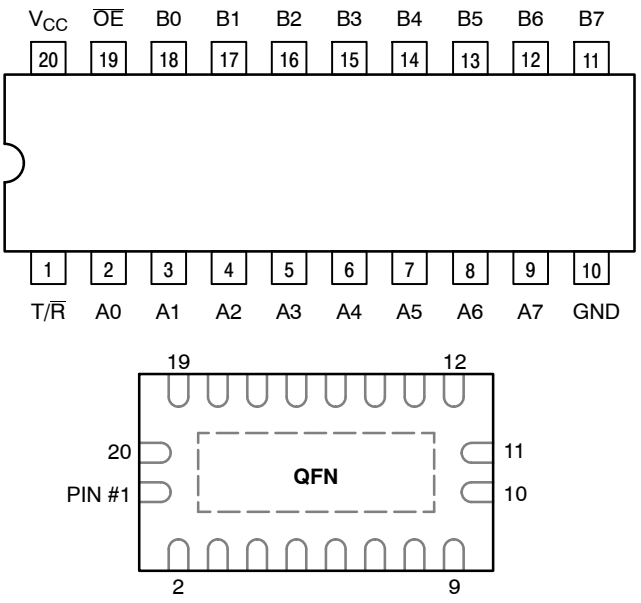



**Figure 1. Pinout** (Top View)

**PIN NAMES**

| PINS | FUNCTION |
|---|---|
| $\overline{OE}$ | Output Enable Input |
| T/$\overline{R}$ | Transmit/Receive Input |
| A0–A7 | Side A 3–State Inputs or 3–State Outputs |
| B0–B7 | Side B 3–State Inputs or 3–StateOutputs |

**TRUTH TABLE**

| INPUTS | | OPERATING MODE Non–Inverting |
|---|---|---|
| $\overline{OE}$ | T/$\overline{R}$ | |
| L | L | B Data to A Bus |
| L | H | A Data to B Bus |
| H | X | Z |

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions are Acceptable
For $I_{CC}$ reasons, Do Not Float Inputs

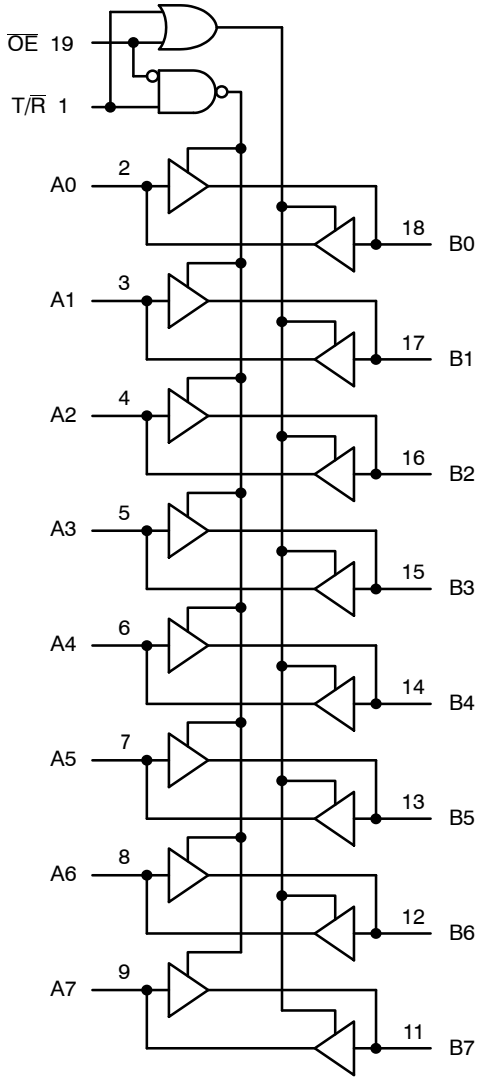



**Figure 2. Logic Diagram**

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Condition | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | DC Input Voltage | $-0.5 \le V_I \le +7.0$ | | V |
| $V_O$ | DC Output Voltage | $-0.5 \le V_O \le +7.0$ | Output in 3−State | V |
| | | $-0.5 \le V_O \le V_{CC} + 0.5$ | Output in HIGH or LOW State (Note 1) | V |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I <$ GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O <$ GND | mA |
| | | +50 | $V_O > V_{CC}$ | mA |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current Per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current Per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | | °C |
| MSL | Moisture Sensitivity | | Level 1 | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $I_O$ absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating<br>Data Retention Only | 2.0<br>1.5 | 2.5, 3.3<br>2.5, 3.3 | 5.5<br>5.5 | V |
| $V_I$ | Input Voltage | | 0 | | 5.5 | V |
| $V_O$ | Output Voltage | (HIGH or LOW State)<br>(3−State) | 0<br>0 | | $V_{CC}$<br>5.5 | V |
| $I_{OH}$ | HIGH Level Output Current | $V_{CC}$ = 3.0 V − 3.6 V<br>$V_{CC}$ = 2.7 V − 3.0 V<br>$V_{CC}$ = 2.3 V − 2.7 V | | | − 24<br>− 12<br>− 8 | mA |
| $I_{OL}$ | LOW Level Output Current | $V_{CC}$ = 3.0 V − 3.6 V<br>$V_{CC}$ = 2.7 V − 3.0 V<br>$V_{CC}$ = 2.3 V − 2.7 V | | | + 24<br>+ 12<br>+ 8 | mA |
| $T_A$ | Operating Free−Air Temperature | | −55 | | +125 | °C |
| $\Delta t/\Delta V$ | Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC}$ = 3.0 V | | 0 | | 10 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = −55°C to +125°C | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage (Note 2) | 2.3 V ≤ $V_{CC}$ ≤ 2.7 V | 1.7 | | V |
| | | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage (Note 2) | 2.3 V ≤ $V_{CC}$ ≤ 2.7 V | | 0.7 | V |
| | | 2.7 V ≤ $V_{CC}$ ≤ 3.6 V | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.3 V ≤ $V_{CC}$ ≤ 3.6 V; $I_{OL}$ = 100 μA | $V_{CC}$ − 0.2 | | V |
| | | $V_{CC}$ = 2.3 V; $I_{OH}$ = −8 mA | 1.8 | | |
| | | $V_{CC}$ = 2.7 V; $I_{OH}$ = −12 mA | 2.2 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −18 mA | 2.4 | | |
| | | $V_{CC}$ = 3.0 V; $I_{OH}$ = −24 mA | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | 2.3 V ≤ $V_{CC}$ ≤ 3.6 V; $I_{OL}$ = 100 μA | | 0.2 | V |
| | | $V_{CC}$ = 2.3 V; $I_{OL}$= 8 mA | | 0.6 | |
| | | $V_{CC}$ = 2.7 V; $I_{OL}$= 12 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 16 mA | | 0.4 | |
| | | $V_{CC}$ = 3.0 V; $I_{OL}$ = 24 mA | | 0.55 | |
| $I_{OZ}$ | 3−State Output Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $V_{OUT}$ = 0 to 5.5 V | | ±5 | μA |
| $I_{OFF}$ | Power Off Leakage Current | $V_{CC}$ = 0, $V_{IN}$ = 5.5 V or $V_{OUT}$ = 5.5 V | | 10 | μA |
| $I_{IN}$ | Input Leakage Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = 5.5 V or GND | | ±5 | μA |
| $I_{CC}$ | Quiescent Supply Current | $V_{CC}$ = 3.6 V, $V_{IN}$ = 5.5 V or GND | | 10 | μA |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | 2.3 ≤ $V_{CC}$ ≤ 3.6 V; $V_{IH}$ = $V_{CC}$ − 0.6 V | | 500 | μA |

2. These values of $V_I$ are used to test DC electrical characteristics only.

## AC CHARACTERISTICS $t_R = t_F$ = 2.5 ns; $R_L$ = 500 Ω

| Symbol | Parameter | Waveform | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = −55°C to +125°C | | | | | | | | |
| | | | $V_{CC}$ = 3.3 V ± 0.3V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 2.5 V ± 0.2V | | $V_{CC}$ = 5.0 V | | |
| | | | $C_L$ = 50 pF | | $C_L$ = 50 pF | | $C_L$ = 30 pF | | $C_L$ = 50 pF | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>Input to Output | 1 | 1.5<br>1.5 | 7.0<br>7.0 | 1.5<br>1.5 | 8.0<br>8.0 | 1.5<br>1.5 | 8.4<br>8.4 | 1.5<br>1.5 | 5.0<br>5.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>to High and Low Level | 2 | 1.5<br>1.5 | 8.5<br>8.5 | 1.5<br>1.5 | 9.5<br>9.5 | 1.5<br>1.5 | 10.5<br>10.5 | 1.5<br>1.5 | 7.0<br>7.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time From<br>High and Low Level | 2 | 1.5<br>1.5 | 7.5<br>7.5 | 1.5<br>1.5 | 8.5<br>8.5 | 1.5<br>1.5 | 9.0<br>9.0 | 1.5<br>1.5 | 6.0<br>6.0 | ns |
| $t_{OSHL}$<br>$t_{OSLH}$ | Output−to−Output Skew<br>(Note 3) | | | 1.0<br>1.0 | | 1.0<br>1.0 | | 1.0<br>1.0 | | 1.0<br>1.0 | ns |

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW ($t_{OSHL}$) or LOW−to−HIGH ($t_{OSLH}$); parameter guaranteed by design.

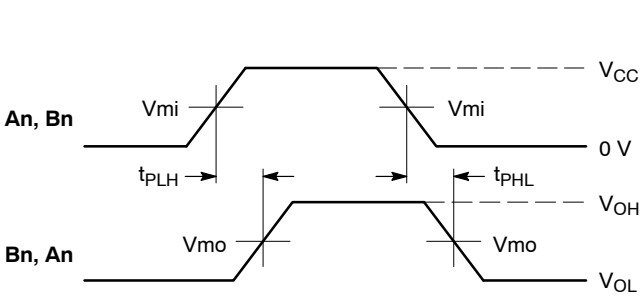
## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Characteristic | Condition | $T_A$ = +25°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 4) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | 0.8<br>0.6 | | V<br>V |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 4) | $V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $V_{IH}$ = 3.3 V, $V_{IL}$ = 0 V<br>$V_{CC}$ = 2.5 V, $C_L$ = 30 pF, $V_{IH}$ = 2.5 V, $V_{IL}$ = 0 V | | −0.8<br>−0.6 | | V<br>V |

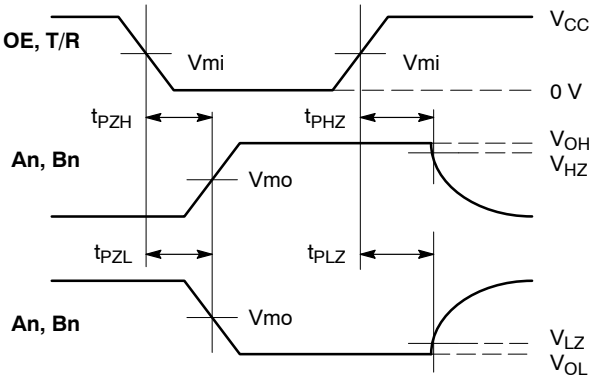
4. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Condition | Typical | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | 10 MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$ | 25 | pF |



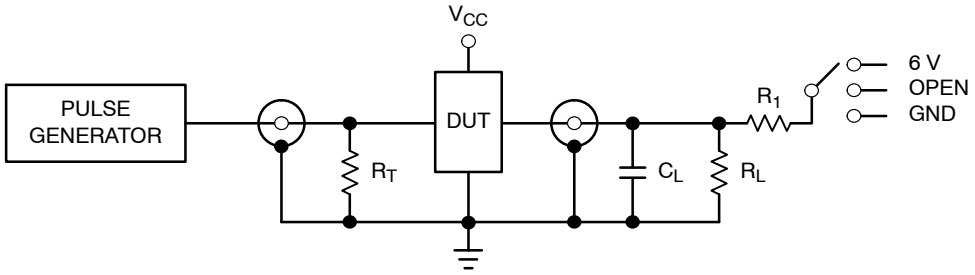

**WAVEFORM 1 – PROPAGATION DELAYS**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns




**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; $t_W$ = 500 ns

**Figure 3. AC Waveforms**

| Symbol | $V_{CC}$ | | | |
|---|---|---|---|---|
| | 3.3 V ± 0.3 V | 2.7 V | 2.5 V ± 0.2 V | 5.0 V |
| Vmi | 1.5 V | 1.5 V | $V_{CC}$/2 | $V_{CC}$/2 |
| Vmo | 1.5 V | 1.5 V | $V_{CC}$/2 | $V_{CC}$/2 |
| $V_{HZ}$ | $V_{OL}$ + 0.3 V | $V_{OL}$ + 0.3 V | $V_{OL}$ + 0.15 V | $V_{OL}$ + 0.15 V |
| $V_{LZ}$ | $V_{OH}$ − 0.3 V | $V_{OH}$ − 0.3 V | $V_{OH}$ − 0.15 V | $V_{OH}$ − 0.15 V |




| TEST | SWITCH |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6 V at $V_{CC}$ = 3.3 ±0.3 V<br>6 V at $V_{CC}$ = 2.5 ±0.2 V |
| Open Collector/Drain $t_{PLH}$ and $t_{PHL}$ | 6 V |
| $t_{PZH}$, $t_{PHZ}$ | GND |

$C_L$ = 50 pF at $V_{CC}$ = 3.3 ±0.3 V or equivalent (includes jig and probe capacitance)
$C_L$ = 30 pF at $V_{CC}$ = 2.5 ±0.2 V or equivalent (includes jig and probe capacitance)
$R_L$ = $R_1$ = 500 Ω or equivalent
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50 Ω)

**Figure 4. Test Circuit**

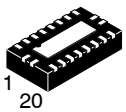
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74LCX245DWR2G | SOIC−20<br>(Pb−Free) | 1000 Tape & Reel |
| MC74LCX245DWG | SOIC−20<br>(Pb−Free) | 38 Units / Rail |
| MC74LCX245DTG | TSSOP−20<br>(Pb−Free) | 75 Units / Rail |
| MC74LCX245DTR2G | TSSOP−20<br>(Pb−Free) | 2500 Tape & Reel |
| NLV74LCX245DTR2G* | TSSOP−20<br>(Pb−Free) | 2500 Tape & Reel |
| MC74LCX245MNTWG | QFN20<br>(Pb−Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

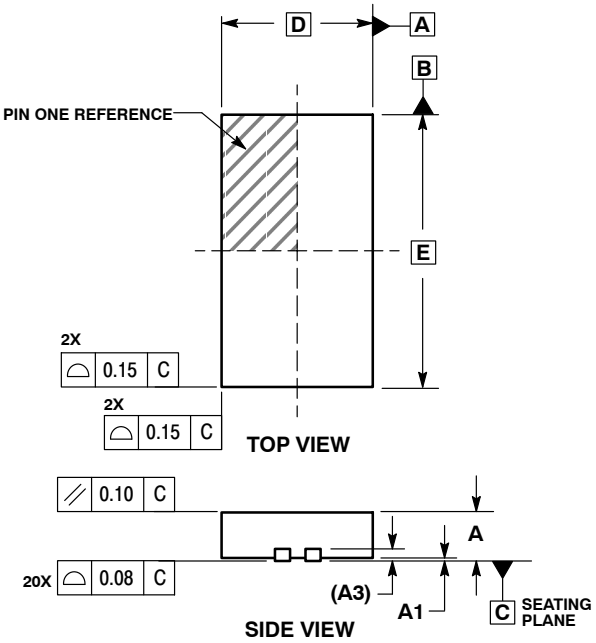
ON Semiconductor®




**SCALE 2:1**

**QFN20, 2.5x4.5 MM**
CASE 485AA−01
ISSUE B

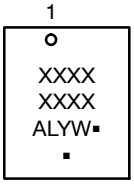
DATE 30 APR 2010




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.50 BSC | |
| D2 | 0.85 | 1.15 |
| E | 4.50 BSC | |
| E2 | 2.85 | 3.15 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.35 | 0.45 |

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

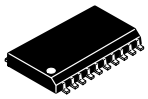
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON12653D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **QFN20. 2.5X4.5 MM** | **PAGE 1 OF 1** |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

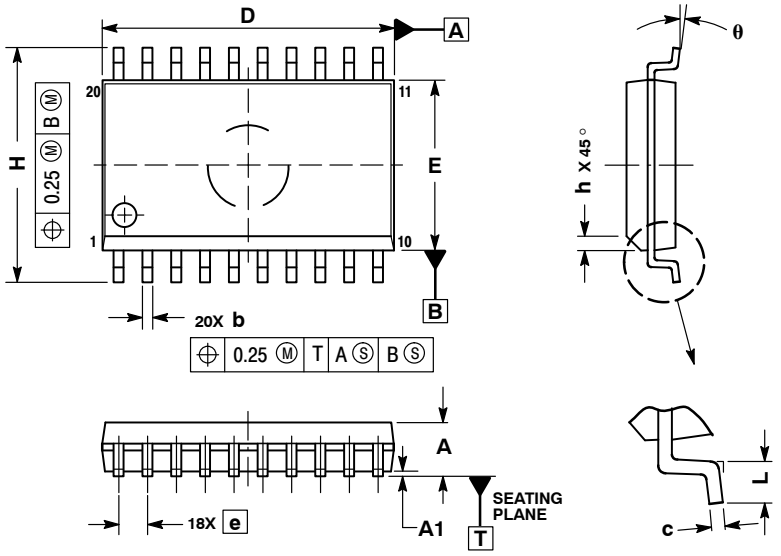
ON Semiconductor®



**SCALE 1:1**

**SOIC–20 WB**
CASE 751D–05
ISSUE H

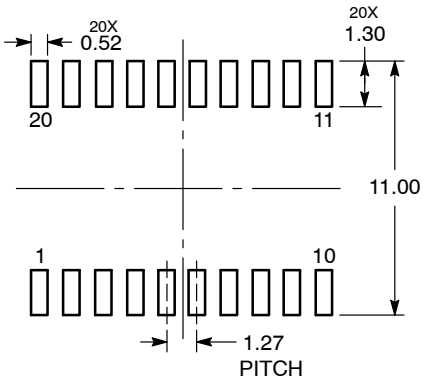
DATE 22 APR 2015




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

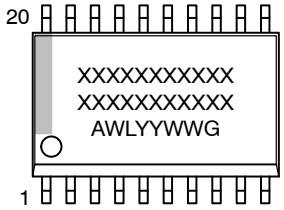
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

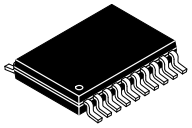
| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42343B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **SOIC–20 WB** | **PAGE 1 OF 1** |

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

**TSSOP−20 WB**
CASE 948E
ISSUE D

DATE 17 FEB 2016



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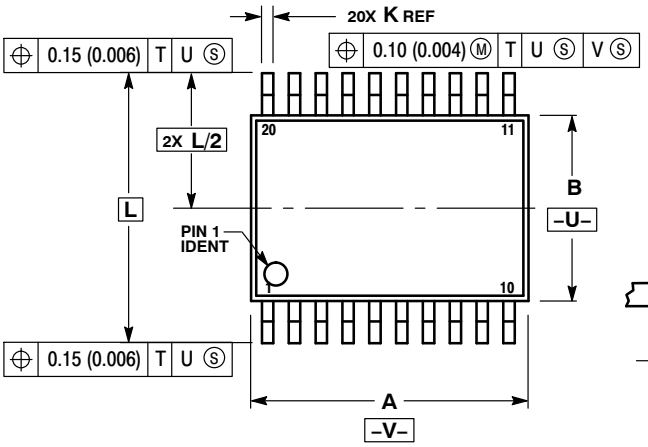
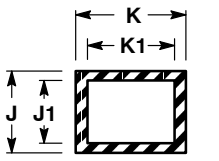
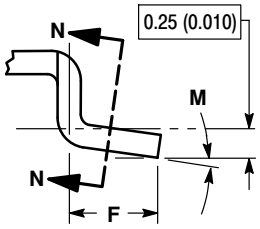
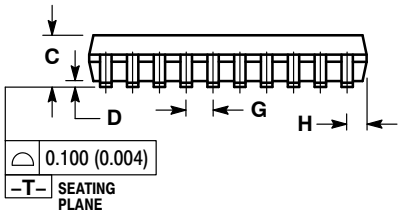


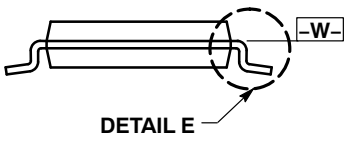




SECTION N−N




DETAIL E

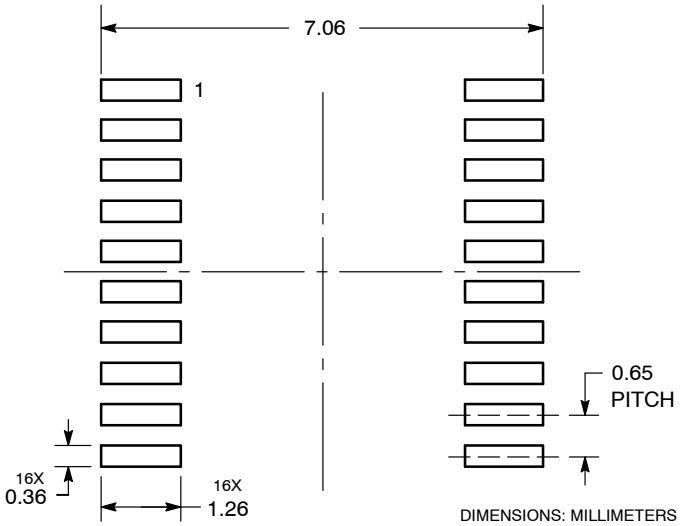



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

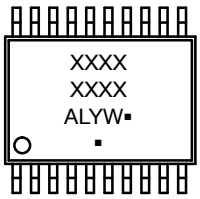
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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| DESCRIPTION: | TSSOP−20 WB | PAGE 1 OF 1 |

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