ABSOLUTE MAXIMUM RATINGS

BATT to GND .....-0.3V to 28V
BST to GND .....-0.3V to 30V
BST to LX .....-0.3V to 6V
LX to GND .....-0.6V to (BATT + 0.3V)
VL to GND .....-0.3V to 6V
CS, CSAV, CC, SYNC, REF, MINDAC, SS, OTP to GND .....-0.3V to (VL + 0.3V)
$\overline{SHDN}$, UP, DN to GND .....-0.3V to 6V
SMBSUS, SDA, SCL to GND .....-0.3V to 6V
BATT, LX Current 1A
SDA Current 50mA
VL Current 50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range
MAX1610CSE/MAX1611CSE .....0°C to +70°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C, BATT = 8.2V, MINDAC = 0V, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
BATT Input Voltage Range		4.75		26	V
BATT Quiescent Supply Current, Operate Mode	BATT = 25V		1.5	3	mA
BATT Quiescent Supply Current, Shutdown Mode			10	20	µA
VL Output Voltage, Operate Mode	4.75V < BATT < 26V	4.25	4.5	4.75	V
VL Output Voltage, Shutdown Mode		3.0	3.6	4.75	V
REF Output Voltage	No load	1.92	2.0	2.08	V
REF Load Regulation	I_{SOURCE} = 100µA		6	20	mV
SWITCHING REGULATOR					
BATT-to-LX Switch On-Resistance	BST - LX = 4.1V		0.7	1.0	Ω
LX Switch Off-Leakage Current				10	µA
Oscillator Frequency	SYNC = REF	250	290	330	kHz
	SYNC = GND	125	145	165	
Oscillator SYNC Pin Synchronization Range		240		350	kHz
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Input Current	SYNC = GND or VL	-1		1	µA
SYNC Input Low Voltage				0.5	V
SYNC Input High Voltage		4.0			V
Power-Switch Maximum Duty Cycle	SYNC = REF	89	91		%
SS Source Current	SS = GND	2.5	4.0	5.5	µA
SS Sink Current	SS = 0.5V	2			mA

ELECTRICAL CHARACTERISTICS (continued)

(T_A = 0°C to +70°C, BATT = 8.2V, MINDAC = 0V, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC AND ERROR AMPLIFIER						
DAC Resolution	Guaranteed monotonic		5			Bits
MINDAC Input Voltage Range			0		1	V
MINDAC Input Bias Current			-1		1	µA
MINDAC Digital PWM Threshold				3		V
CSAV Input Voltage Range			0		1.0	V
CSAV Regulation Point	D/A at full scale		232	247	260	mV
	D/A at 1LSB			12		
CSAV Input Bias Current			-5		5	µA
CSAV to CC Voltage-to-Current Converter Transconductance	CC = 2V, CSAV = 1V, D/A at 1LSB			85		µmho
CC Sink Current	CC = 2V, CSAV = 1V, D/A at 1LSB			80		µA
CC Source Current	CC = 2V, CSAV = 0V, D/A at full scale			20		µA
OPEN AND SHORTED TUBE PROTECTION						
OTP Voltage Trip Point	Referred to REF	OTP rising	-20		20	mV
OTP Input Bias Current	GND < OTP < VL		-1		1	µA
CS Overcurrent Cutoff Threshold				500		mV
MAX1610 LOGIC LEVELS						
$\overline{SHDN}$, UP, DN Input Low Voltage					0.8	V
$\overline{SHDN}$, UP, DN Input High Voltage			2.4			V
$\overline{SHDN}$, UP, DN Input Bias Current			-1		1	µA
MAX1611 LOGIC LEVELS						
SMBSUS, SDA, SCL Input Low Voltage					0.8	V
SMBSUS, SDA, SCL Input High Voltage			2.2			V
SMBSUS, SDA, SCL Input Bias Current			-1		1	µA
SDA Output Low Sink Current	V_{SDA} = 0.6V		6			mA

TIMING CHARACTERISTICS—MAX1610

(Figure 1, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UP, DN Pulse Width High	t_1		1			µs
UP, DN Pulse Width Low	t_2		1			µs
UP, DN Pulse Separation	t_3		1			µs
Counter Reset Time	t_4		1			µs

TIMING CHARACTERISTICS—MAX1611

(Figures 2 and 3, T_A = +25°C, unless otherwise noted.)

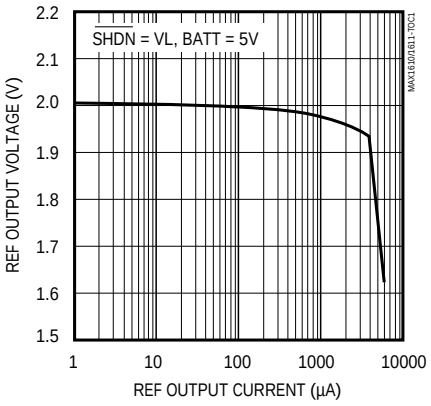
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial Clock High Period	t_{HIGH}		4			µs
SCL Serial Clock Low Period	t_{LOW}		4.7			µs
SCL, SCA Rise Time	t_R	(Note 1)			1	µs
SCL, SDA Fall Time	t_F	(Note 1)			0.3	µs
Start Condition Setup Time	$t_{SU:STA}$		4.7			µs
Start Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		500			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$	(Note 1)	0			ns
SCL Falling Edge to SDA Valid, Reading Out Data	t_{DV}				1	µs

Note 1: Guaranteed by design.

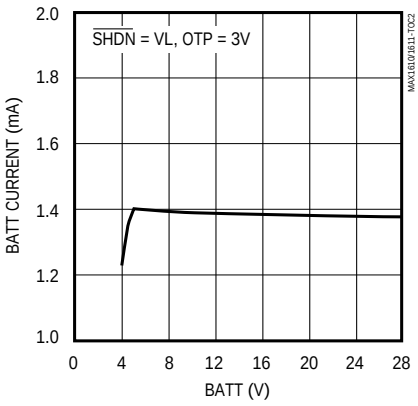
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

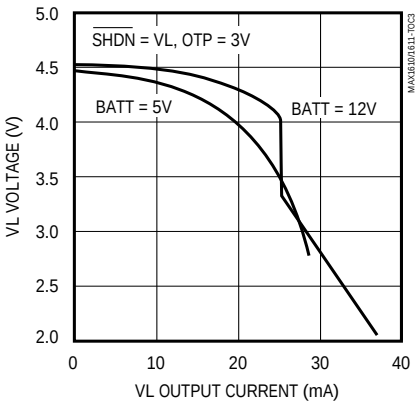
REF OUTPUT VOLTAGE vs. REF OUTPUT CURRENT



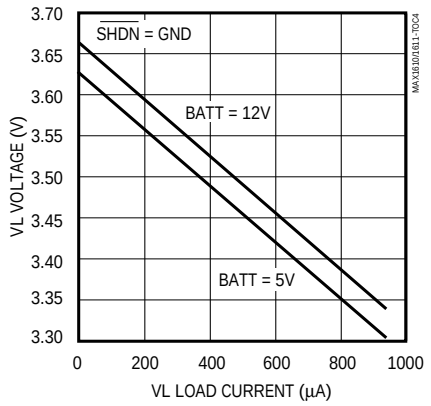
BATT SUPPLY CURRENT vs. BATT VOLTAGE (SHDN = VL)



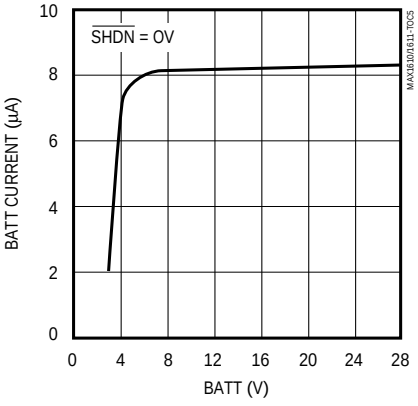
VL OUTPUT VOLTAGE vs. VL OUTPUT CURRENT



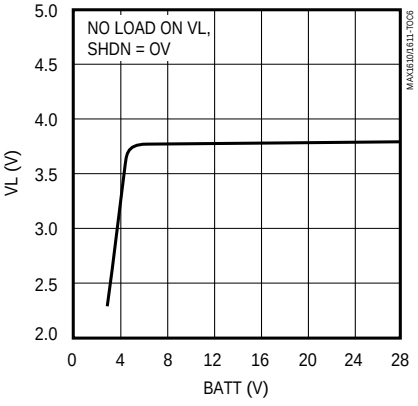
VL OUTPUT VOLTAGE vs. VL LOAD CURRENT



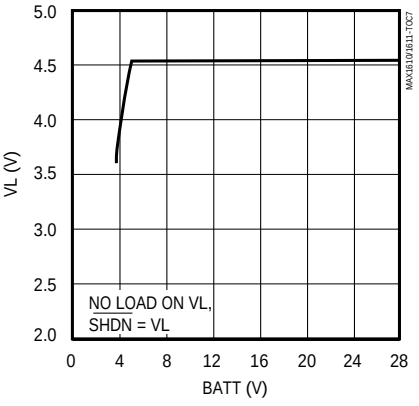
BATT SUPPLY CURRENT vs. BATT VOLTAGE (SHDN = OV)



VL OUTPUT VOLTAGE vs. BATT VOLTAGE (SHDN = OV)



VL OUTPUT VOLTAGE vs. BATT VOLTAGE (SHDN = VL)



Pin Description

PIN		NAME	FUNCTION
MAX1610	MAX1611		
1	—	UP	Logic-Level Input. A rising edge on UP increments the 5-bit counter for the 5-bit DAC. UP = DN = 1 presets the counter to mid-scale.
—	1	SDA	System Management Bus Serial Data Input and Open-Drain Output
2	—	DN	Logic-Level Input. A rising edge on DN decrements the 5-bit counter for the 5-bit DAC. UP = DN = 1 presets the counter to mid-scale.
—	2	SCL	System Management Bus Serial Clock Input
3	—	$\overline{SHDN}$	Logic-Level Shutdown Input Pin. Applying a logic low to $\overline{SHDN}$ places the chip in a low-supply-current shutdown mode.
—	3	SMBSUS	System Management Bus Suspend Mode Input. SMBSUS Selects one of two chip-configuration settings, which are preprogrammed serially.
4	4	SYNC	Oscillator Synchronization Input. Tying SYNC to REF sets the oscillator frequency to 290kHz. Tying SYNC to GND or VL lowers the oscillator frequency to 145kHz.
5	5	SS	Soft-Start Pin. A 4µA current source feeds the capacitor placed on SS. The voltage on this pin limits the peak current in the switch. When the lamp is turned off, SS pulls to GND.
6	6	CC	Output of the Voltage-to-Current Converter; Input to the PWM Comparator, which sets the current limit. A capacitor placed at CC sets the current-regulator-loop bandwidth.
7	7	CSAV	Input to the Voltage-to-Current Converter, which averages the voltage on CSAV using the capacitor on CC.
8	8	MINDAC	The voltage at MINDAC sets the DAC's minimum-scale output voltage. Tying MINDAC to VL enables the internal 280Hz current-chopping mode.
9	9	REF	2.0V Reference Output. Bypass with 0.1µF to GND.
10	10	OTP	Open-Tube Protection Comparator. As long as OTP exceeds the reference voltage, the N-channel BATT-to-LX switch is forced off.
11	11	CS	Low-Side Current-Sense Input. The current-mode regulator terminates the switch cycle when the voltage at CS exceeds REF - CC.
12	12	VL	Output of the Internal Linear Regulator. VL can be overdriven by a voltage greater than 4.75V to operate the chip from +5V ± 5%, and to conserve power. Bypass with 0.1µF to GND.
13	13	GND	System Ground
14	14	BST	Power Input to the High-Side Gate Driver, which switches the internal N-channel MOSFET on and off.
15	15	LX	Ground Connection for the Internal High-Side Gate Driver; source-connection point for the internal N-channel MOSFET
16	16	BATT	4.5V to 25V Battery-Voltage Input Point. Connects to the internal N-channel power MOSFET's drain, and to the input of the internal linear regulator that powers the chip.

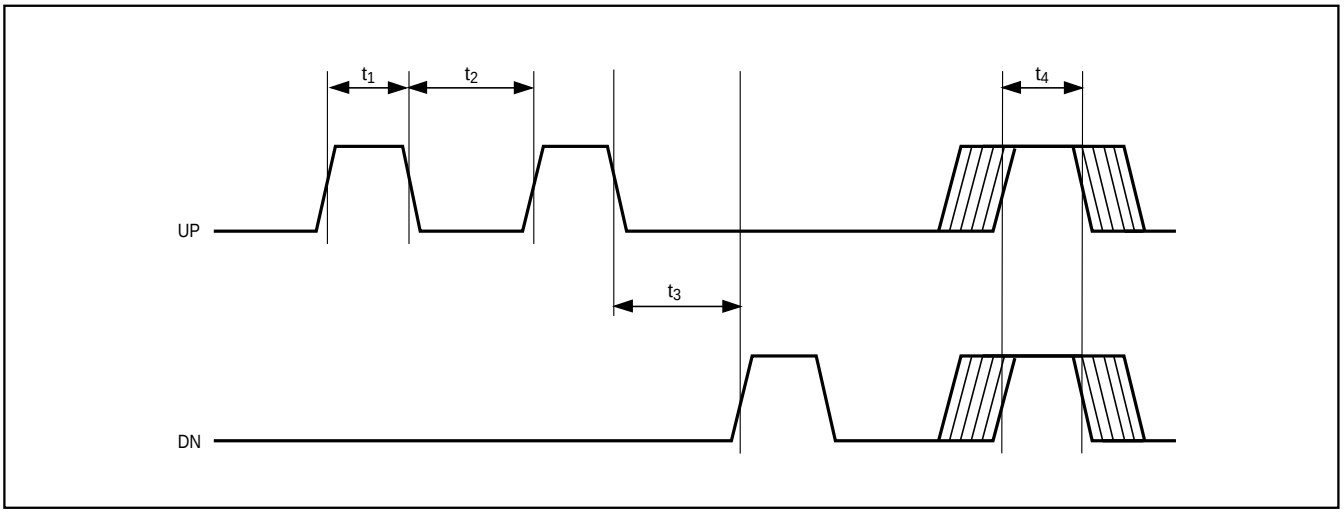


Figure 1. MAX1610 UP and DN Signal Timing

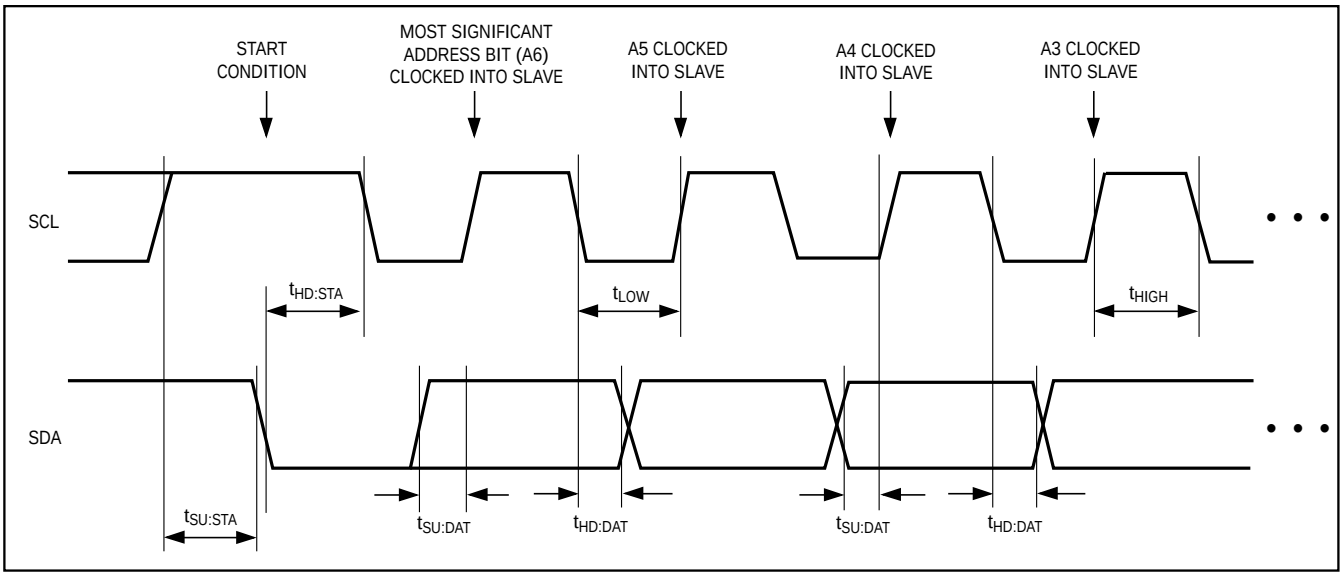


Figure 2. MAX1611 SMB Serial-Interface Timing—Address

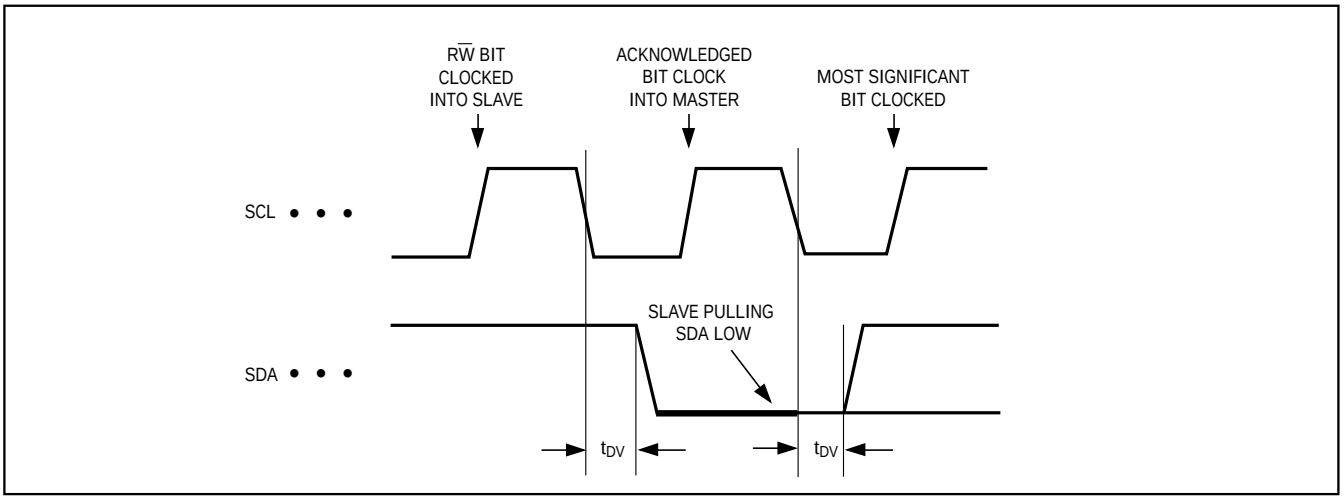


Figure 3. MAX1611 SMB Serial-Interface Timing—Acknowledge

Detailed Description

Getting Started

A cold-cathode fluorescent lamp (CCFL) has two terminals. For the CCFL to emit light, the two lamp terminals must be driven with a high-voltage (approximately 550V AC RMS) and high-frequency (approximately 45kHz) sine wave. The MAX1610/MAX1611 use a varying DC input voltage to create this high-voltage, high-frequency sine-wave drive. To select the correct component values for the MAX1610/MAX1611 circuit, several CCFL parameters and the minimum DC input voltage must be specified; these are listed in Table 1.

Table 3 shows the recommended component values to use with the circuit of Figure 4, depending on the particular CCFL parameters. The C2 values in Table 3 have been selected such that the normal operating voltage on the secondary of T1 is as close as possible to the CCFL strike voltage (where the strike voltage (V_S) is assumed to be approximately 1.8 times the CCFL operating voltage (V_L)).

Components T1, C1, R2, Q1, and Q2 form a Royer oscillator. A Royer oscillator is a resonant tank circuit that oscillates at a frequency dependent on C1, the primary magnetizing inductance of T1 (L_P), and the impedance seen by the T1 secondary. The MAX1610/MAX1611 regulate the current fed into the Royer oscillator by sensing the voltage on R1. For a given current through the Royer oscillator (I_{R1}), the power delivered to the CCFL depends on the Royer oscillator frequency. The R1 values in Table 3 have been selected to ensure that the power into the CCFL does not exceed its maximum rating, despite T1, C1, and C2 component-value variations. The Royer oscillator waveforms for the circuit of Figure 4 are shown in Figures 5 and 6.

Analog Circuitry

The MAX1610/MAX1611 maintain fixed CCFL brightness with varying input voltages on BATT by regulating the current fed into the Royer oscillator. This current is sensed via resistor R1 between CSAV and GND. An internal switch from BATT-to-LX pulse-width modulates at a fixed frequency to servo the CSAV pin to its regulation voltage. The CSAV regulation voltage can be adjusted via the digital interface to set CCFL brightness. The MAX1610 and MAX1611 differ only in the digital interface they use to adjust the internal 5-bit digital-to-analog converter (DAC) that sets the CSAV regulation voltage. The minimum-scale (min-scale) CSAV regulation voltage is resistor adjustable using the MINDAC pin, setting the minimum CCFL brightness. The D/A setting at MAX1610/MAX1611 power-up is preset to mid-scale (10000 binary) (Figure 7).

MINDAC Sets the Minimum Scale

The MINDAC pin sets the lowest CCFL brightness level. The voltage at MINDAC is divided by eight, and sets the minimum CSAV regulation voltage. For example, in the circuit of Figure 4, R5 (150kΩ) and R6 (51kΩ) form a resistor divider from REF, which sets MINDAC to 507mV (REF = 2.0V). This sets a minimum CSAV regulation voltage of 63mV with a full-scale CSAV regulation voltage of 247mV.

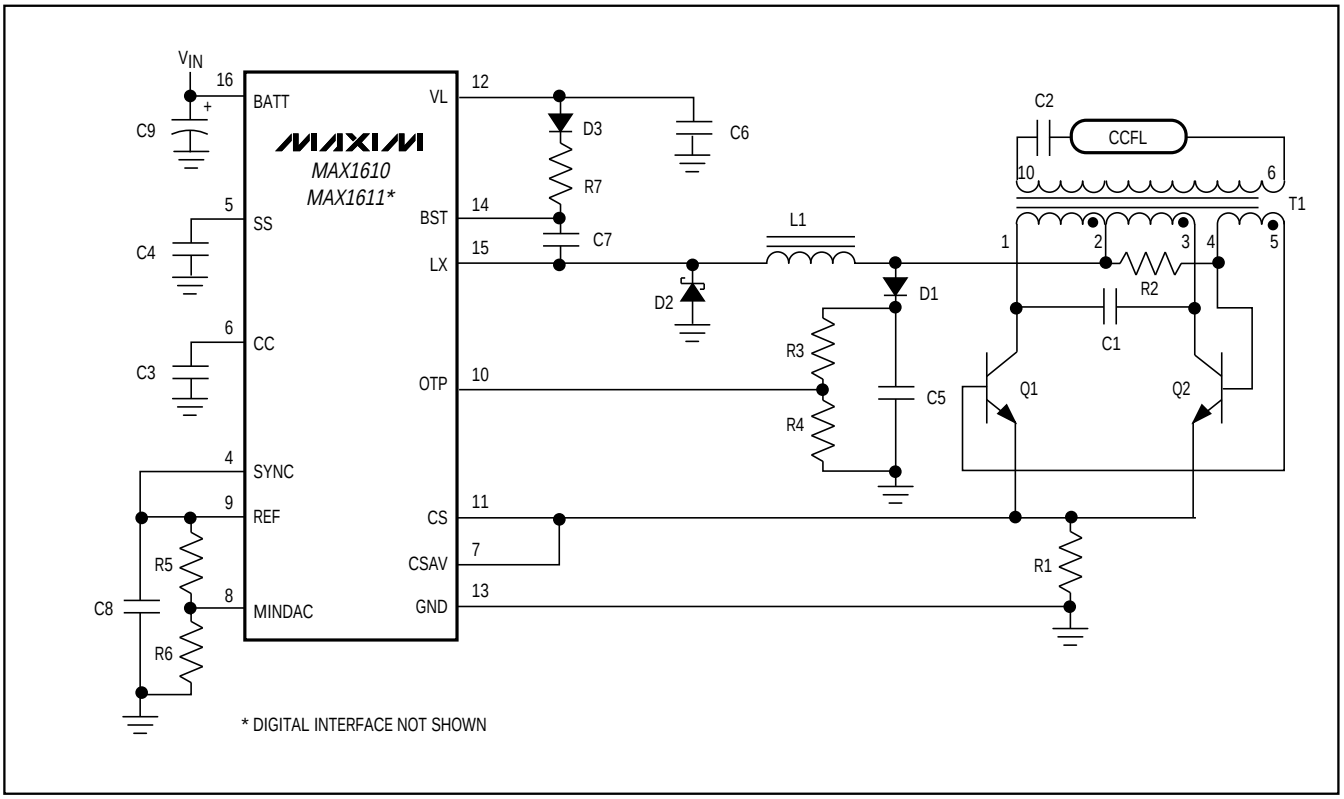


Figure 4. Typical Floating-Lamp Application Circuit

Table 1. Necessary CCFL Specifications

SPECIFICATION	UNITS	SYMBOL	DESCRIPTION
CCFL Minimum Strike Voltage (“Kick-Off Voltage”)	V_{RMS}	V_S	Although CCFLs typically operate at $550V_{RMS}$, a higher voltage is required initially to light up the tube.
CCFL Typical Operating Voltage (“Lamp Voltage”)	V_{RMS}	V_L	Once a CCFL has been struck, the voltage required to maintain light output falls to approximately $550V_{RMS}$. Small tubes may operate on as little as $250V_{RMS}$. The operating voltage of the CCFL stays relatively constant, even as the tube’s brightness is varied.
CCFL Maximum Operating Current (“Lamp Current”)	mA_{RMS}	I_L	The maximum root-mean-square AC current through a CCFL is almost always $5mA_{RMS}$. No DC current is allowed through any CCFL.
CCFL Maximum Frequency (“Lamp Frequency”)	kHz	f_L	The maximum AC-lamp-current frequency.
DC Power Source Minimum Input Voltage	V	V_{MIN}	The minimum DC input voltage to the MAX1610/MAX1611 circuit determines the turns ratio required for the DC-AC conversion transformer. Decreasing the minimum input voltage increases the size of the transformer required for a given output power.

Table 2. Typical Application Circuit Component Values

a) Resistors

SYMBOL	VALUE	TOLERANCE	POWER RATING
R1	(Note)	±1%	1/8W
R2	510Ω	±10%	1/8W
R3	51kΩ	±5%	1/16W
R4	8.2kΩ	±5%	1/16W
R5	150kΩ	±5%	1/16W
R6	51kΩ	±5%	1/16W
R7	20Ω	±10%	1/16W

b) Capacitors

SYMBOL	VALUE	TOLER-ANCE	WORKING VOLTAGE	NOTES
C1	0.1µF	±20%	±25V	δF ≤ 0.001 @ 1kHz
C2	(Note 1) (pF)	±10%	±3kV	High voltage
C3, C5	27nF	±20%	25V	
C4, C6, C7, C8	0.1µF	-20%	25V	Ceramic, larger values acceptable
C9	10µF	-50%	35V	Tantalum, low ESR

c) Other Components

SYMBOL	DESCRIPTION	GENERIC PART	SURFACE-MOUNT PART	MANUFACTURER
Q1, Q2	1A NPN switching transistor, $V_{CEO} \geq 50V$	2N2222A	FMMT619, SOT23	Zetex
D1, D3	50mA silicon diode, $V_{BR} \geq 40V$	1N4148	CMPD4448, SOT23	Central
D2	1A Schottky diode, $V_{BR} \geq 30V$	1N5818	EC10QS04	Nihon
L1	100µH, 1A inductor		CDR125-101	Sumida
T1	6W Royer oscillator transformer, turns ratio 67:1, secondary (pins 10 and 6) : primary (pins 1 and 3), primary magnetizing inductance (L_P) of 44µH ±20%		CTX110605	Coiltronics

Note: Component values depend on lamp characteristics. See Table 3 to select values.

Table 3. Selecting Circuit Values for Figure 4

V_L (V_{RMS})	I_L (mA_{RMS})	C2	R1	VCT (V_{MAX})	f_{ROY} (kHz)		
					MIN	TYP	MAX
250	3	22pF	1.21Ω	3.63V	50.3	58.6	71.8
250	5	43pF	0.715Ω	3.61V	43.3	49.7	60.3
300	3	18pF	1.18Ω	4.30V	52.1	61.0	75.1
300	5	36pF	0.681Ω	4.14V	45.6	52.8	64.7
450	5	20pF	0.732Ω	6.55V	51.1	59.7	73.3
500	5	18pF	0.715Ω	7.17V	52.1	61.0	75.1
550	5	18pF	0.665Ω	7.29V	52.5	61.8	76.7
600	5	15pF	0.698Ω	8.41V	53.6	63.1	78.1

Note: f_{ROY} = Royer oscillator damped resonant oscillation frequency. T1 primary magnetizing inductance (L_P) = 44µH ±20%.
VCT = average voltage from the T1 center tap to the emitters of Q1 and Q2 (ignoring Q1, Q2 $V_{CE,SAT}$).
C1 = 0.1µF ± 20%; C2 = ±10% tolerance; R1 = ±1% tolerance.

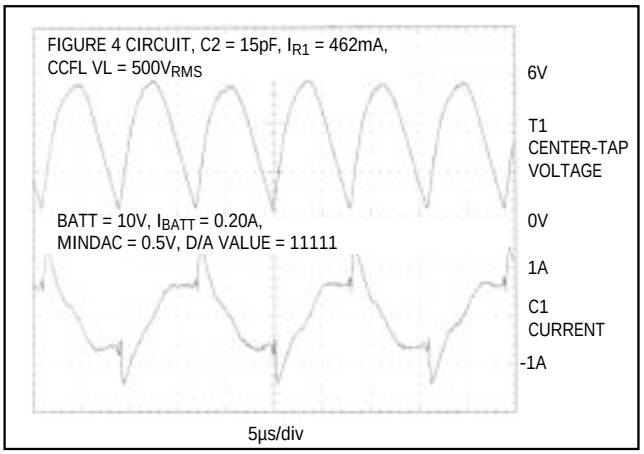


Figure 5. Royer Oscillator Typical Operating Waveforms for Circuit of Figure 4

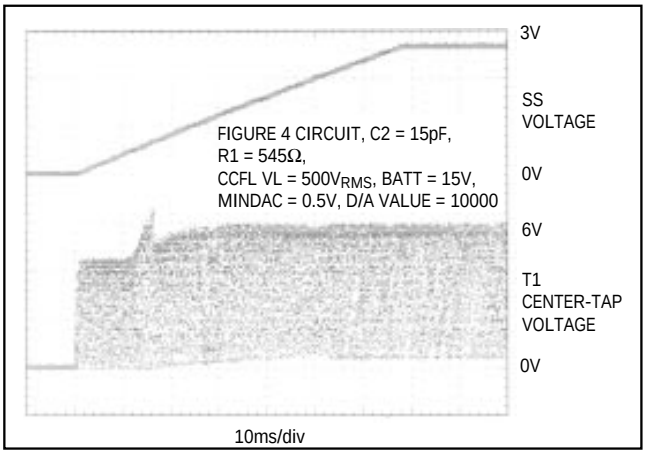


Figure 6. Start-Up Waveforms for Circuit of Figure 4

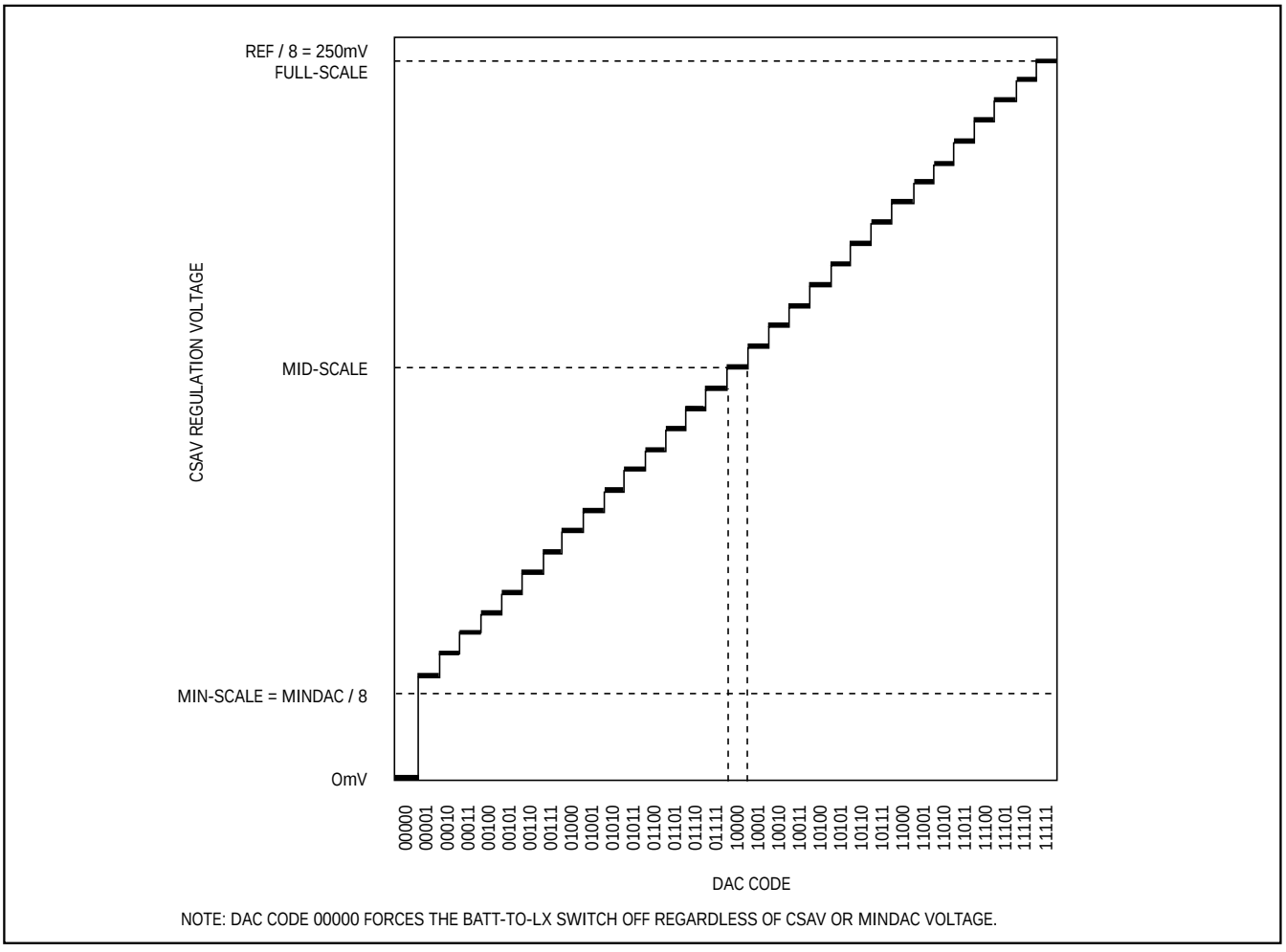


Figure 7. CSAV Regulation Voltage Range

Digitally Controlled CCFL Backlight Power Supplies

Open-Tube Protection (OTP)

Any real transformer used in a Royer oscillator will have a maximum-allowed secondary voltage. If the maximum-allowed secondary voltage is exceeded, the winding insulation can break down, leading to permanent transformer damage. The maximum-allowed secondary voltage can be exceeded either when the CCFL drive circuit is turned on without the CCFL being in place, or when the CCFL becomes disconnected during normal operation due to a mechanical failure. To protect against these fault conditions, use the OTP pin to sense the voltage on the transformer center tap (pin 2 of Figure 4). Whenever the voltage on OTP exceeds the REF reference voltage, the BATT-to-LX power switch is forced off.

For example, in Figure 4, the CTX110605 transformer has a maximum-allowed continuous secondary voltage of $1340V_{RMS}$. D1 and C5 detect the peak voltage on the center tap of T1. R3 and R4 determine the limit on the center tap peak voltage. The relationship between the voltage on the center tap of T1 and the secondary voltage is diagrammed in Figure 8. Neglecting the Q1/Q2 saturation voltage and the voltage on the R1 current-sense resistor yields Equation 1:

$$V_{CTPK} = \frac{V_{SEC}\sqrt{2}}{2N}$$

where V_{SEC} is the maximum root-mean-square voltage allowed on the secondary, N is the secondary-to-primary turns ratio, and V_{CTPK} is the peak voltage on the transformer center tap.

Block Diagram of the Analog Section

Figure 9 shows a functional diagram of the analog circuitry in the MAX1610/MAX1611. The chips have identical analog circuitry, and differ only in their digital interface.

Loop-Compensation Capacitor (CC)

The BATT-to-LX switch turns on at fixed frequency, and turns off when the current-sense voltage on the CS pin exceeds CC - REF. As the CC pin voltage rises, the CS current limit rises as well. A transconductance amplifier compares the voltage on CSAV to the desired regulation voltage and outputs a current proportional to this error to the CC pin. A capacitor from CC to GND sets the bandwidth of this regulation loop, as shown in Equation 2:

$$BW = \frac{85}{2\pi C3}$$

where BW is the bandwidth of the CSAV regulation loop in kHz, and C3 is the capacitance from CC to GND in nF.

Soft Start (SS)

Soft start prevents the triggering of OTP upon power-up. Placing a capacitor from SS to GND soft starts the Royer oscillator by slowly raising the CS current-limit voltage. Internal circuitry pulls SS to GND during power-on reset, or whenever the lamp is turned off (DAC = 00000, shutdown mode, ON-1 = 0, or ON-0 = 0) (Figures 10 and 11). When SS is not pulled to GND, an internal 4µA current sources into the capacitor at the SS pin. This pin is internally diode clamped to REF so that it rises to a maximum voltage of about 2.7V. Regardless of the voltage on CC, the CS current-sense voltage is never allowed to exceed the voltage on SS divided by 5.

Frequency Selection and Synchronization

The SYNC pin performs two functions: it sets the BATT-to-LX switching frequency, and it allows the BATT-to-LX switching frequency to be synchronized to an external oscillator. SYNC tied to GND or VL sets a 145kHz switching frequency; SYNC tied to REF sets a 290kHz

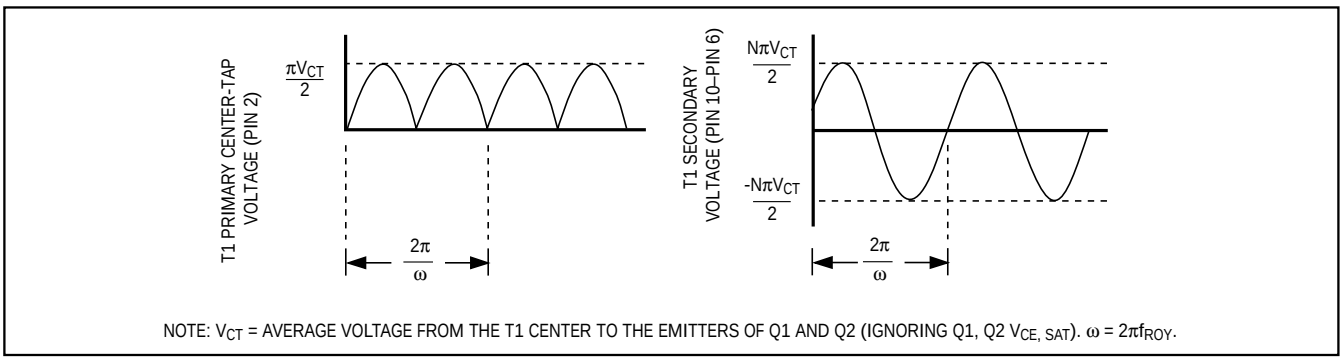


Figure 8. Transformer Primary/Secondary Voltage Relationship

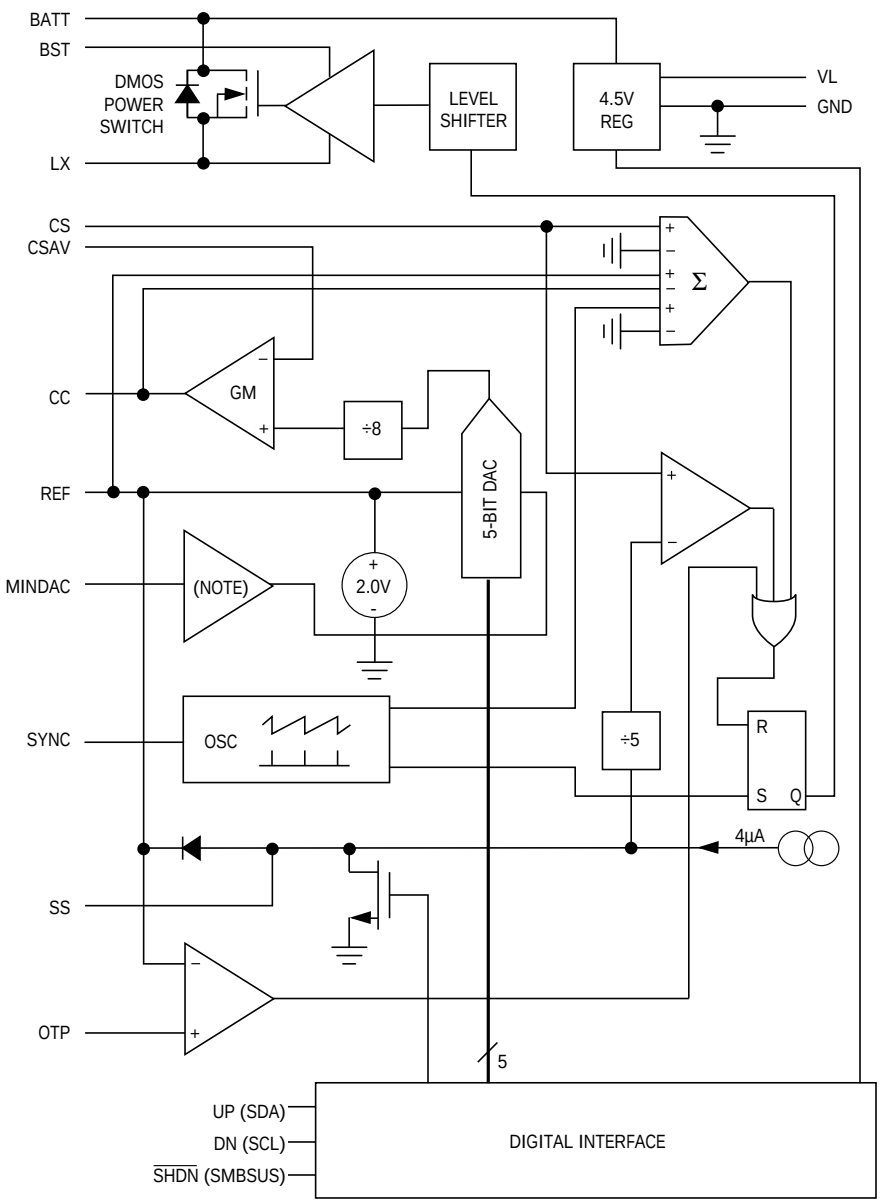


Figure 9. Functional Diagram

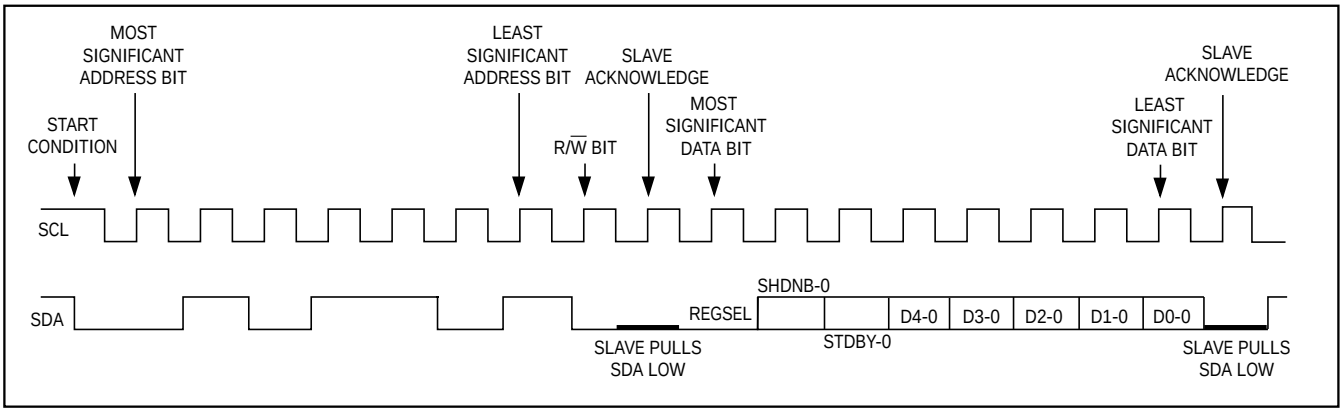


Figure 10. MAX1611 Serial-Interface Single-Byte Write Example (REGSEL = 0)

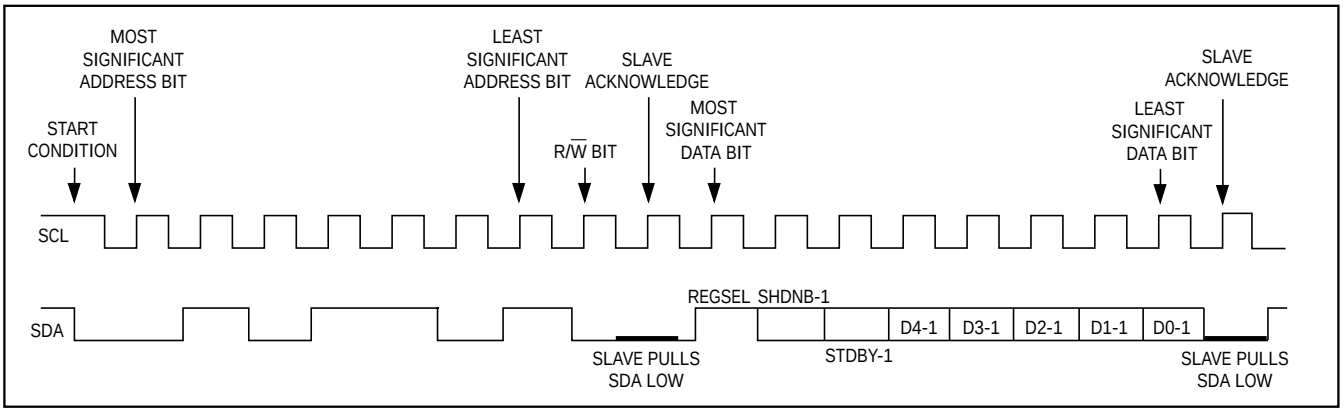


Figure 11. MAX1611 Serial-Interface Single-Byte Write Example (REGSEL = 1)

switching frequency. Any rising edge on SYNC restarts a BATT-to-LX switch cycle by forcing the switch on.

MAX1610 Digital Interface

The MAX1610 contains an internal 5-bit up/down counter that sets the value of the internal 5-bit DAC. At power-on, or when both the UP and DN pins are held high simultaneously, the 5-bit up/down counter is preset to 10000 binary, which corresponds to mid-scale. A rising edge on UP increments the 5-bit up/down counter. A rising edge on DN decrements the 5-bit up/down counter. The counter will not roll over on either underflow or overflow. For example, if the CCFL is at maximum intensity level, rising edges on UP will not change the output.

The $\overline{SHDN}$ pin provides a way to lower the MAX1610 supply current to 10µA without resetting the 5-bit up/down counter. With $\overline{SHDN}$ = 1, the MAX1610 operates normally with VL at 4.5V. When the BATT-to-LX power switch operates, an additional 3mA of current (other than the supply current) is consumed through the BST pin, requiring VL to source at least 4.5mA of current. With $\overline{SHDN}$ = 0, all analog circuitry turns off, except for a coarse regulator that can source up to 500µA from VL. The coarse regulator preserves the state of the internal logic and keeps the digital interface active during shutdown ($\overline{SHDN}$ = 0).

MAX1611 Digital Interface

A single byte of data written over the Intel System Management Bus (SMBus™) controls the MAX1611. Figures 10 and 11 show example single-byte writes. The MAX1611 contains two 7-bit latches for storing configuration data. Only one of the 7-bit latches is active at a time. The MAX1611 responds only to its own address, 0101101 binary. The SMBSUS pin selects which of the two sets of configuration data is used. Figure 12 shows a schematic diagram of the MAX1611's digital circuitry. Notice that the SMBSUS pin selects which one of the

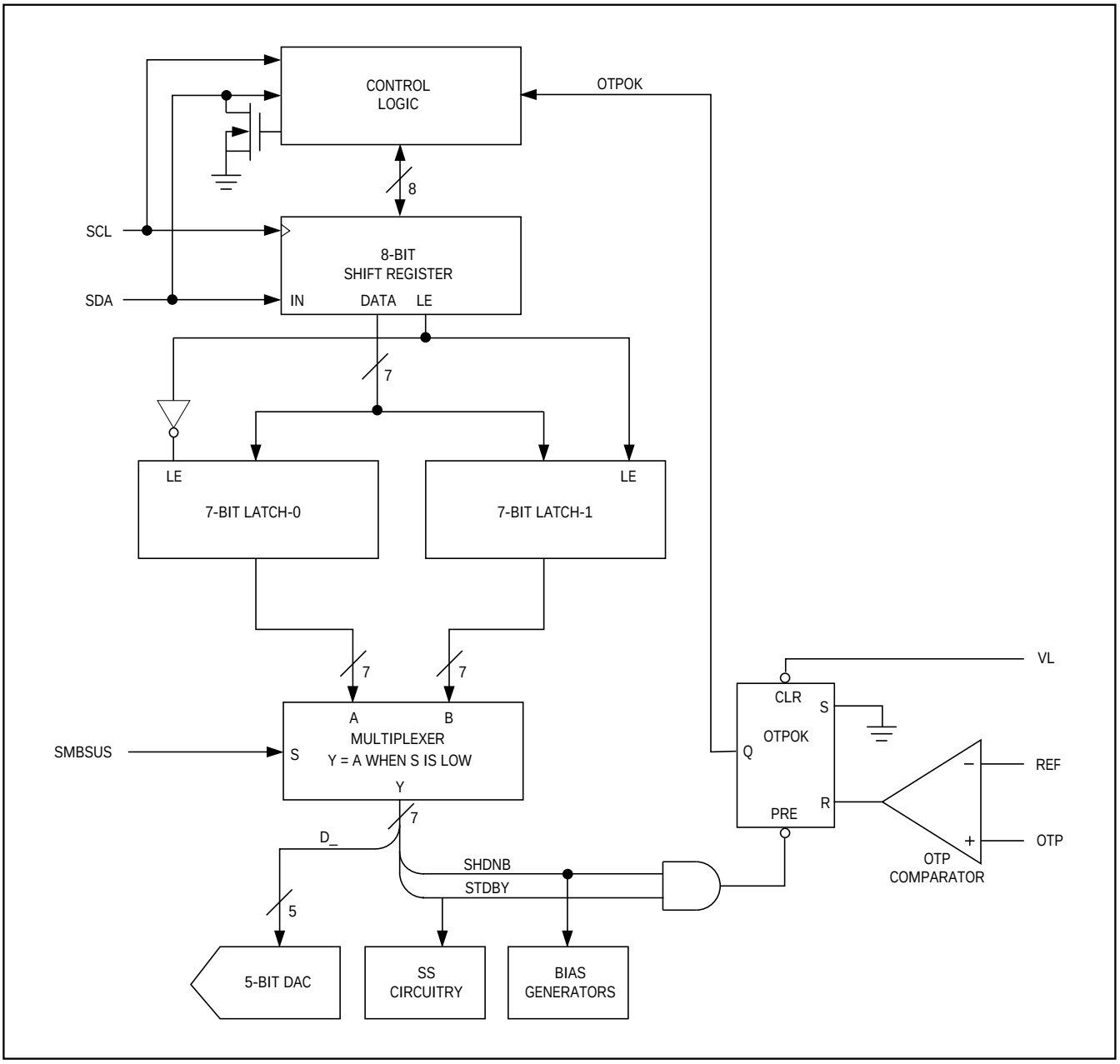


Figure 12. MAX1611 Serial-Interface Circuitry Block Diagram

Table 4. MAX1611 Configuration Byte with REGSEL = 0

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A zero in this bit writes the remaining seven bits into the 7-bit latch-0 (Figure 13).
6	SHDNB-0	0	Complete Shutdown. Pulling SMBSUS low with SHDNB-0 = 0 places the MAX1611 into a low-quiescent-current shutdown mode, with the reference off and the VL linear-regulator output switched to a low-current, coarse regulation mode. Pulling SMBSUS low with SHDNB-0 = 1 puts the MAX1611 into its normal operational mode, with the reference and internal VL linear regulator fully on. SHDNB-0 supersedes STDBY-0. As long as SHDNB-0 = 0 and SMBSUS = 0, it doesn't matter what STDBY-0 is; the MAX1611 still shuts down.
5	STDBY-0	0	Standby, disables CCFL supply only. As long as SMBSUS stays low and STDBY-0 = 0, the internal power switch is kept off and SS is held shorted to GND; neither the internal reference nor the linear regulator is affected. With STDBY = 1 and SMBSUS low, the MAX1611 operates normally.
4 3 2 1 0	D4-0 D3-0 D2-0 D1-0 D0-0	1 0 0 0 0	DAC Input Data. With the SMBSUS pin low, bits D4-0 through D0-0 set the DAC.

** Initial register state after power-up.*

Table 5. MAX1611 Configuration Byte with REGSEL = 1

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A one in this bit writes the remaining seven bits into the 7-bit latch-1 (Figure 13).
6	SHDNB-1	1	Complete Shutdown. Pulling SMBSUS high with SHDNB-1 = 0 places the MAX1611 into a low-quiescent-current shutdown mode, with the reference off and the VL linear regulator output switched to a low-current coarse regulation mode. Pulling SMBSUS high with SHDNB-1 = 1 puts the MAX1611 into its normal operational mode, with the reference and internal VL linear regulator fully on. SHDNB-1 supersedes STDBY-1. As long as SHDNB-1 = 0 and SMBSUS = 0, it doesn’t matter what STDBY-1 is; the MAX1611 still shuts down.
5	STDBY-1	1	Standby, disables CCFL supply only. As long as SMBSUS stays high and STDBY-1 = 0, the internal power switch is kept off and SS is held shorted to GND; neither the internal reference nor the linear regulator is affected. With STDBY-1 = 1 and SMBSUS high, the MAX1611 operates normally.
4 3 2 1 0	D4-1 D3-1 D2-1 D1-1 D0-1	1 0 0 0 0	DAC Input Data. With the SMBSUS pin high, bits D4-1 through D0-1 set the DAC.

** Initial register state after power-up.*

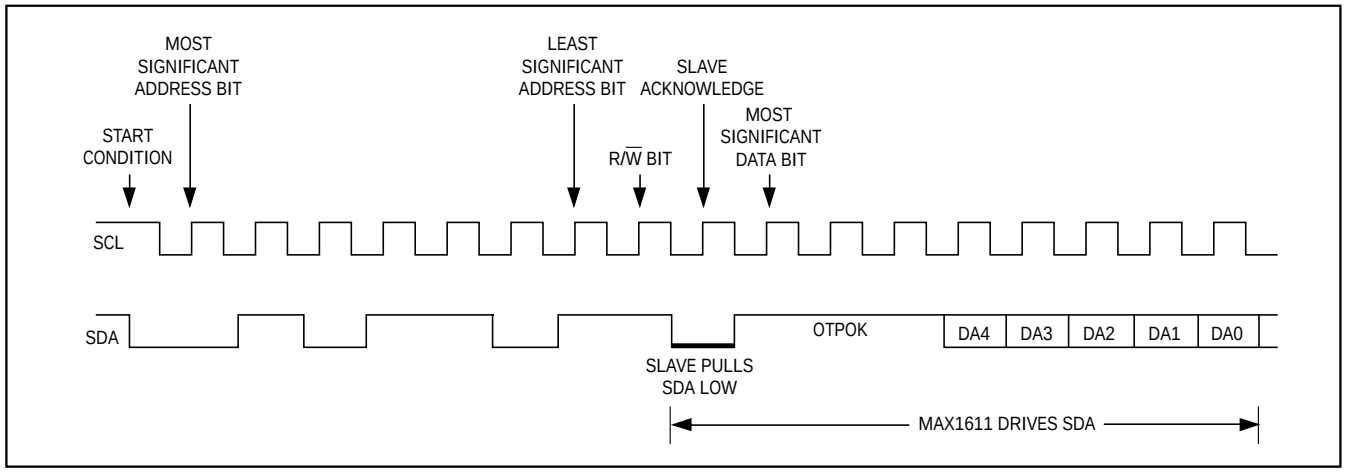


Figure 13. MAX1611 Serial-Interface Read Example

Table 6. MAX1611 Status Bits

BIT	NAME	POR STATE*	FUNCTION
7	OTPOK	1	Latched Open-Tube Detection. OTPOK = 0 indicates that open-tube detection has been triggered. As soon as the voltage on the OTP pin exceeds REF, the OTPOK bit is cleared. Reset the OTPOK pin by entering shutdown or standby.
6 5	— —	— —	Unused. These bits always return a logic one.
4 3 2 1 0	DA4 DA3 DA2 DA1 DA0		Displays the DAC setting selected by SMBSUS.

** Initial register state after power-up.*

two 7-bit registers is used. Tables 4 and 5 describe the data format for the configuration data.

Status information can be read from the MAX1611 using the SMBus read-byte protocol. Figure 13 shows an example status read. Table 6 describes the status information data format.

During shutdown (SMBSUS = 0 and SHDNB-0 = 0, or SMBSUS = 1 and SHDNB-1 = 0), the MAX1611 serial interface remains fully functional and can be used to set either the SHDNB-0 or SHDNB-1 bits in order to return the MAX1611 to its normal operational state.

Chopping the Lamp Current

Chopping the lamp current allows lower sustainable light levels without lamp flicker. Intensity is varied by controlling the on-time duty cycle. Tying MINDAC to VL activates a special mode, which allows the CCFL intensity to be varied by turning the lamp on and off at a frequency faster than the eye can detect. The SS pin pulls to GND during off time and rises to 2.7V during on time. During on time, the CSAV pin regulates to REF / 8 (250mV). During off time, the BATT-to-LX power switch is forced off and the CC compensation node goes high impedance. Omit R5, R6, and C4 of the circuit in Figure 4.

In this mode, leave SS floating and increase the CC capacitance to 0.1µF. Also, insert a 330Ω resistor in series with D1 (Figure 4) to prevent the open-lamp detection circuit from being tripped by the repeated striking of the lamp. The SS pin will oscillate at the switching frequency divided by 1024 (283Hz with SYNC = REF). The intensity can be varied with the duty cycle at the SS pin. The duty cycle is set by the DAC in 3% increments. Duty cycle will vary with intensity. Full-scale yields a 100% duty cycle. DAC codes 00001, 00010, and 00011 all yield the

Digitally Controlled CCFL Backlight Power Supplies

minimum 9% duty cycle. DAC code 00000 shuts off the lamp entirely (0% duty cycle). Figure 14 shows the chopped waveforms with the DAC set to mid-scale.

Applications Information

Directly Regulating the Lamp Current

The MAX1610/MAX1611 can directly regulate the CCFL current by tapping into the secondary of T1 (Figure 15). This allows more precise setting of the maximum lamp current (I_L). The disadvantage of this approach is that the secondary-to-ground voltage is twice that shown in Figure 4, increasing the likelihood of the thermometer effect, where one end of the lamp is brighter than the other. Figure 15 uses the same component values as Figure 4, except for R1, R40, D40, and D41. D40 and D41 are the same type of diode as D1. R1 should be 0.68Ω ±10% to set a peak current limit of about 735mA. Use a 107Ω ±1% resistor for R40 to set a lamp current of $5mA_{RMS}$. This circuit accepts a wide range of lamp types without component adjustments.

Component Suppliers

Table 7 lists three different sources for C1. C1 requires a low dissipation factor to prevent overheating as energy is cycled between C1 and the T1 magnetizing inductance in the Royer resonant tank. Table 8 lists suppliers for the high-voltage ballast capacitor, C2.

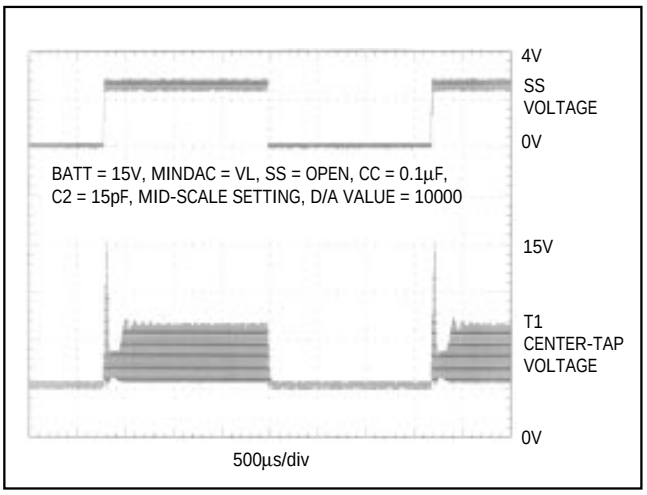


Figure 14. Chopped Waveforms

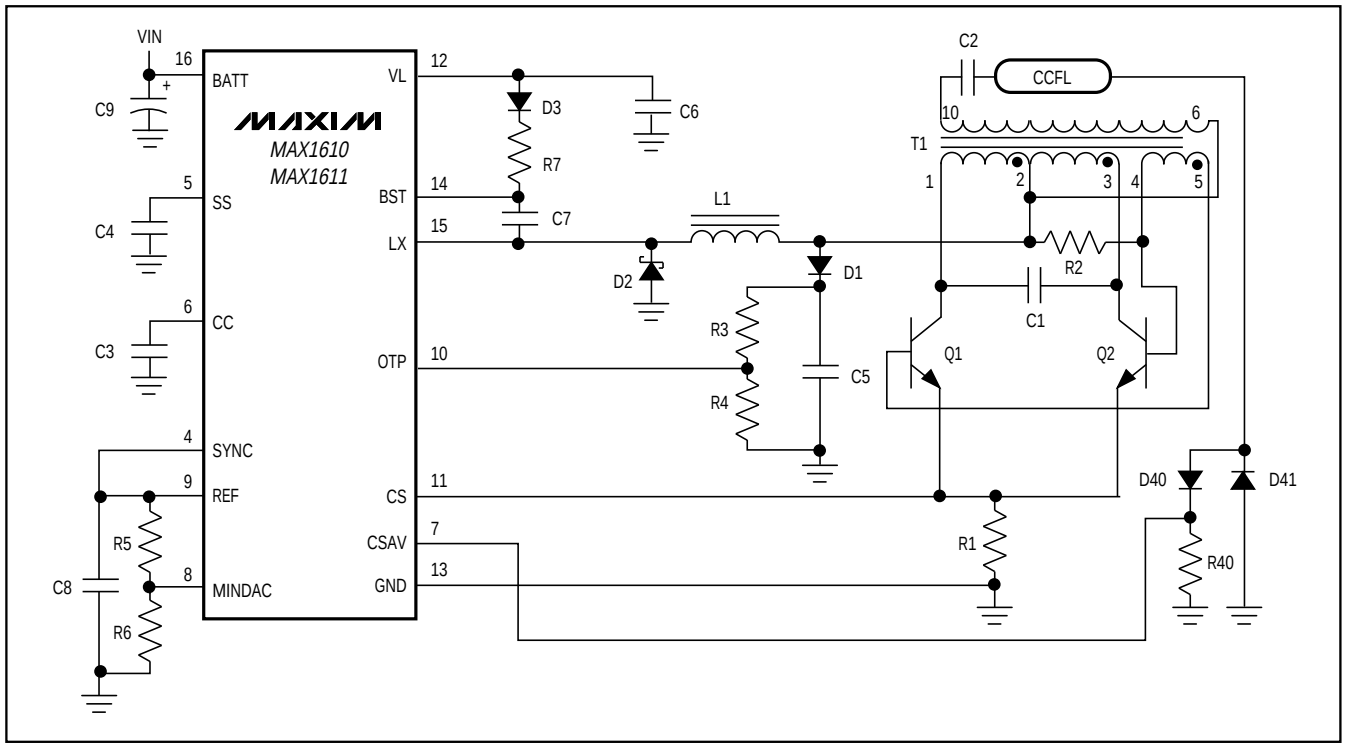


Figure 15. Directly Regulating the CCFL Current

Table 7. Capacitor C1 Supplier Information

PART	SUPPLIER	LOCATION	PHONE	FAX	NOTES/CONTACT
SMD7.3104	WIMA	Elmsford, NY	914-347-2474	914-347-7230	Dissipation factor (tan δ) at 1kHz and 20°C ≤ 0.008.
		Germany	(0621) 8785-0	(0621) 8710457158	
		Hong Kong	5-70-11-51	58-06-84-74	
CHEV0025J104	PACCOM Electronics	Redmond, WA	206-883-9200	206-881-6959	Dissipation factor (tan δ) at 1kHz ≤ 0.002.
4040N104M250	NOVACAP	Valencia, CA	805-295-5920	805-295-5928	Dissipation factor (tan δ) at 1kHz and 20°C ≤ 0.0015.

Table 8. Capacitor C2 Supplier Information

PART	SUPPLIER	LOCATION	PHONE	FAX
1808HA330KATMA	AVX/Kyocera	Olean, NY	716-372-6611	716-372-6316
		Vancouver, WA	206-696-2840	206-695-5836
		Germany	08131 9004-0	08131 9004-44
		Hong Kong	852-363-3303	852-765-8185
GHM1040SL330J3K	Murata	Smyrna, GA	404-436-1300	404-436-3030
		Germany	49-911-66870	49-911-6687193
		Taiwan	886-2-562-4218	886-2-536-6721
302C1812A330K	Metuchen Capacitors, Inc.	Old Bridge, NJ	908-679-3366	908-679-3222
302R29N330K	Johanson Dielectrics	Sylmar, CA	818-364-9800	818-364-6100

Chip Information

TRANSISTOR COUNT : 5457

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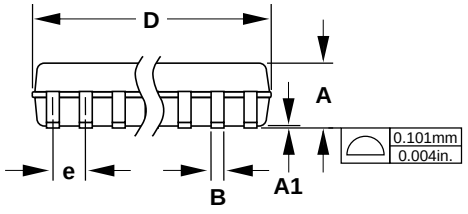
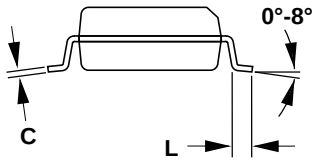
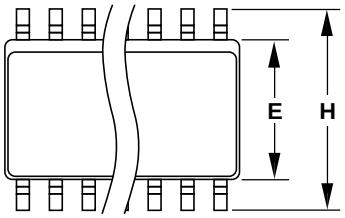
Package Information





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



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DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

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