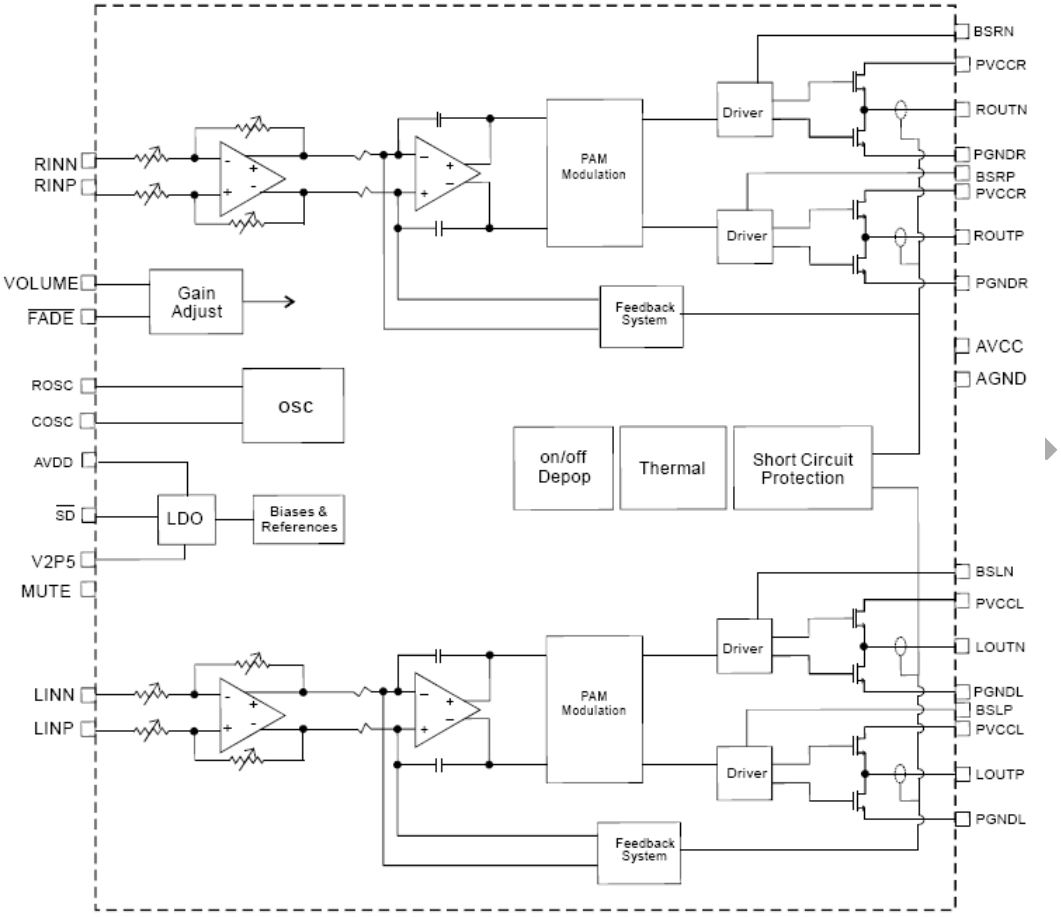
Pin Descriptions

Pin Number	Pin Name	Function
1	RINN	Negative differential audio input for right channel.
2	RINP	Positive differential audio input for right channel.
3	AVDD	5V Analog VDD
4	VREF	Analog reference for gain control section.
5	VOLUME	DC voltage that sets the gain of the amplifier.
6	REF GND	Ground for gain control circuitry. Connect to AGND. If using a DAC to control the volume, connect the DAC ground to this terminal.
7	AGND1	Analog GND
8	$\overline{\text{FADE}}$	Input for controlling volume ramp rate when cycling SD or during power-up. A logic low on this pin places the amplifier in fade mode. A logic high on this pin allows a quick transition to the desired volume setting.
9	LINP	Positive differential audio input for left channel.
10	LINN	Negative differential audio input for left channel.
11, 20	PGNDL	Power ground for left channel H-bridge.
12, 19	PVCCL	Power supply for left channel H-bridge, not connected to PVCCR or AVCC.
13, 14	LOUTN	Class-D 1/2-H-bridge negative output for left channel.
15	BSLN	Bootstrap I/O for left channel, negative high-side FET.
16	BSLP	Bootstrap I/O for left channel, positive high-side FET.
17, 18	LO UTP	Class-D 1/2-H-bridge positive output for left channel.
21	VCLAMPL	Internally generated voltage supply for left channel bootstrap capacitors.
22	CO SC	I/O for charge/discharging currents onto capacitor for ramp generator triangle wave biased at V2P5.
23	RO SC	Current setting resistor for ramp generator. Nominally equal to 1/8*VCC.
24, 28	AGND	Analog GND
25	MUTE	A logic high on this pin disables the outputs and a logic low enables the outputs.
26	AVCC	High-voltage analog power supply (7V to 15V)
27	V2P5	2.5V Reference for analog cells, as well as reference for unused audio input when using single-ended inputs.
29	$\overline{\text{SD}}$	Shutdown signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to VCC.
30	VCLAMPR	Internally generated voltage supply for right channel bootstrap capacitors.
31, 40	PGNDR	Power ground for right channel H-bridge.
32, 39	PVCCR	Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
33, 34	ROUTP	Class-D 1/2-H-bridge positive output for right channel.
35	BSRP	Bootstrap I/O for right channel, positive high-side FET.
36	BSRN	Bootstrap I/O for right channel, negative high-side FET.
37, 38	ROUTN	Class-D 1/2-H-bridge negative output for right channel.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage V_{DD}	-0.3 to +16.5	V
Input Voltage Range V_I:		
MUTE, V_{REF}, VOLUME, $\overline{FADE}$	0 to +6.0	V
$\overline{SD}$	-0.3 to V_{DD}	
RINN, RINP, LINN, LINP	-0.3 to +6.0	
Junction Temperature Range, T_J	-40 to +125	°C
Storage Temperature	-65 to +150	
Lead Temperature 1, 6mm (1/16 inch)	260, 5 sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage (V_{DD})	7 to 15	V
Maximum Volume Control Pins, Input Pins Voltage	0 to +5.0	
High Level Input Voltage:		
$\overline{SD}$	2.0 to V_{DD}	V
MUTE, $\overline{FADE}$	2.0 to 5.0	
Low Level Input Voltage:		
$\overline{SD}$	0 to +0.3	V
MUTE, $\overline{FADE}$	0 to +0.3	
Ambient Operating Temperature	-20 to +85	°C

Thermal Information

Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Ambient)	QFN6mm*6mm	θ_{JA}	18.1	°C/W
Thermal Resistance (Junction to Case)	QFN6mm*6mm	θ_{JC}	7.6	

The Exposed PAD must be soldered to a thermal land on the PCB.

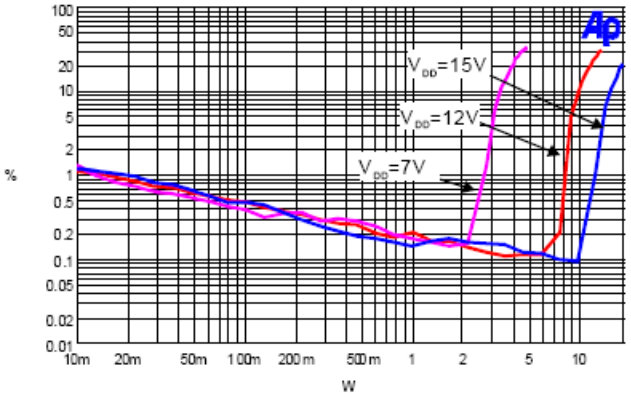
Electrical Characteristics (@T_A = +25°C, V_{DD} = 12V, R_L = 8Ω, unless otherwise specified.)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Supply Voltage	V_{DD}			7.0	12	15	V
Continuous Output Power	P_O	THD+N = 0.1%, f = 1kHz, R_L = 8Ω			5		W
		THD+N = 1.0%, f = 1kHz, R_L = 8Ω			8		
		THD+N = 10%, f = 1kHz, R_L = 8Ω, V_{DD} = 13V			10		
		THD+N = 0.1%, f = 1kHz, R_L = 4Ω (Note 3)			15		
Total Harmonic Distortion plus Noise	THD+N	P_O = 5W, f = 1kHz, R_L = 8Ω			0.1		%
Quiescent Current	I_{DD}	No Load			20	30	mA
Supply Quiescent Current in Shutdown Mode	I_{SD}	Shutdown = 0V			4	10	μA
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{CC} = 12V, I_O = 1A, T_J = +25°C	High Side		200		mΩ
			Low Side		200		
			Total		400		
Power Supply Ripple Rejection	PSRR	$1V_{PP}$ Ripple, f = 1kHz, Inputs AC-Coupled to Ground			-60		dB
Oscillator Frequency	f_{OSC}	R_{OSC} = 120kΩ, C_{OSC} = 220pF			250		kHz
Output Integrated Noise Floor	VN	20Hz to 22kHz, A-Weighting			-90		dB
Crosstalk	CS	P_O = 3W, R_L = 8Ω, f = 1kHz			-80		dB
Signal to Noise Ratio	SNR	Maximum output at THD+N < 0.5%, f = 1kHz			80		dB
Output Offset Voltage (measured differentially)	$\lvert V_{OS} \rvert$	INN and INP connected together			30		mV
2.5V Bias Voltage	V2P5	No Load			2.5		V
Internal Analog Supply Voltage	AV_{DD}	V_{DD} = 7V to 15V			5.0	5.5	V
Over Temperature Shutdown	OTS				150		°C
Thermal Hysteresis	OTH				40		°C

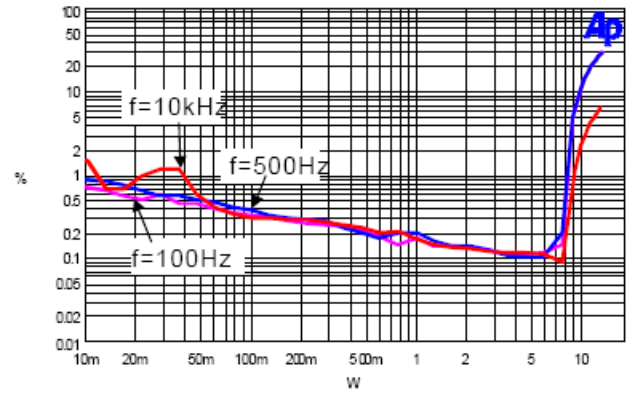
Note: 3. Heat sink is required for high power output.

Typical Performance Characteristics (@T_A = +25°C, V_{DD} = 12V, R_L = 8Ω, G_V = 24dB, unless otherwise specified.)

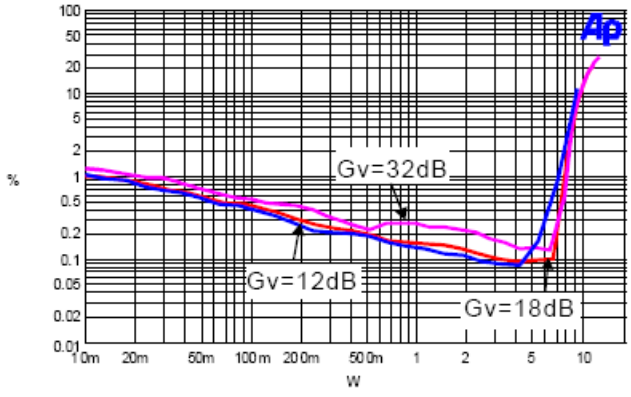
1. THD+N vs. Power



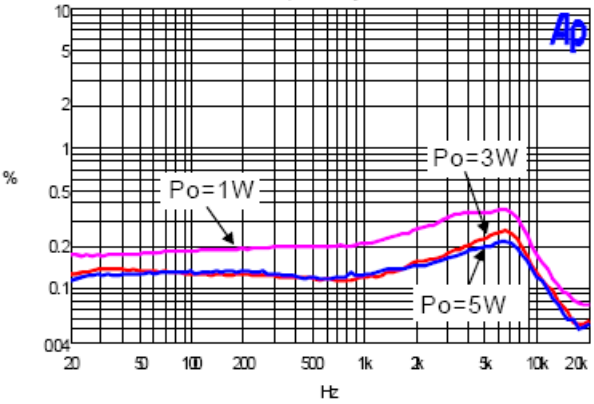
2. THD+N vs. Power



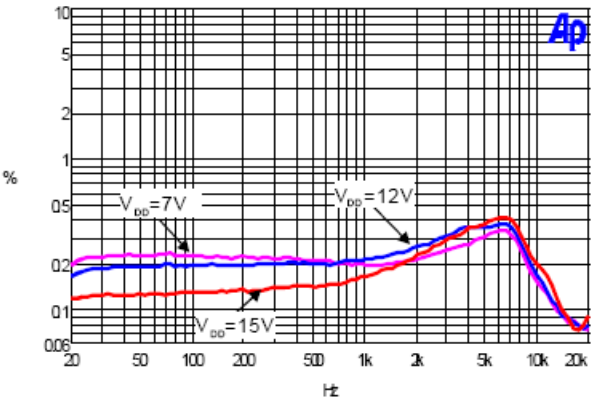
3. THD+N vs. Power



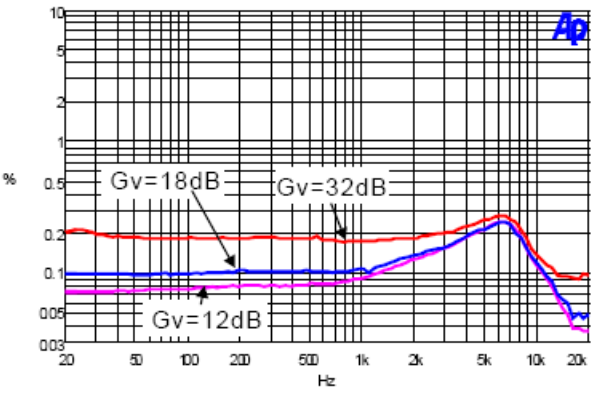
4. THD+N vs Frequency



5. THD+N vs Frequency (Po=1W)

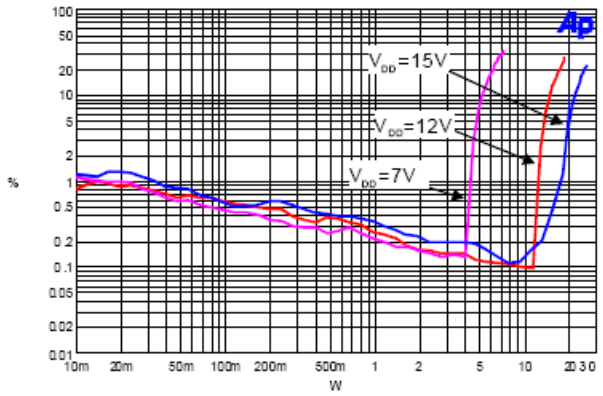


6. THD+N vs Frequency (Po=3W)

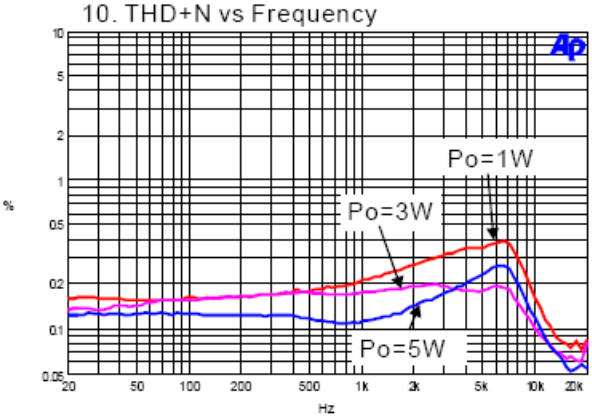


Typical Performance Characteristics (cont.) (@T_A = +25°C, V_{DD} = 12V, R_L = 4Ω, G_V = 24dB, unless otherwise specified.)

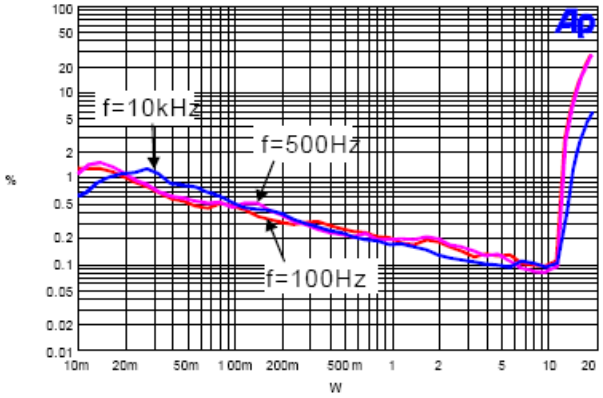
7. THD+N vs. Power



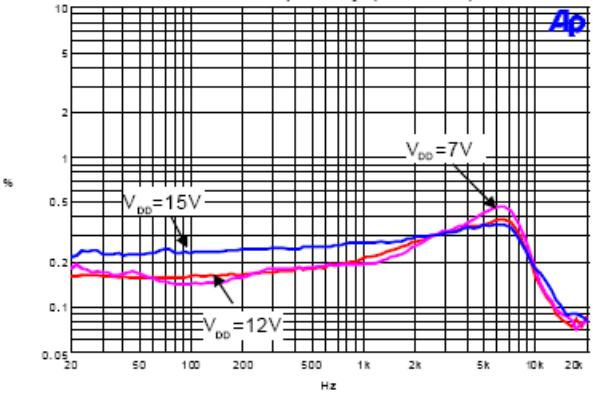
10. THD+N vs Frequency



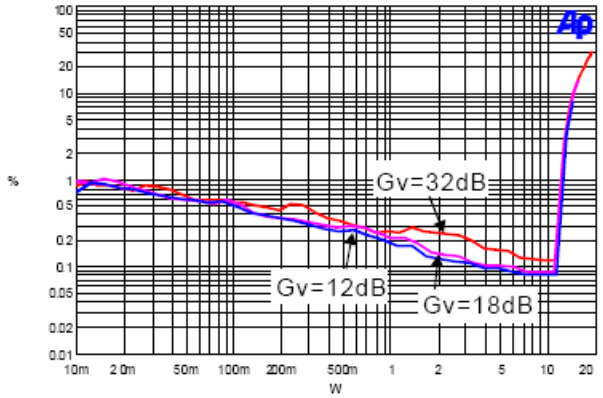
8. THD+N vs. Power



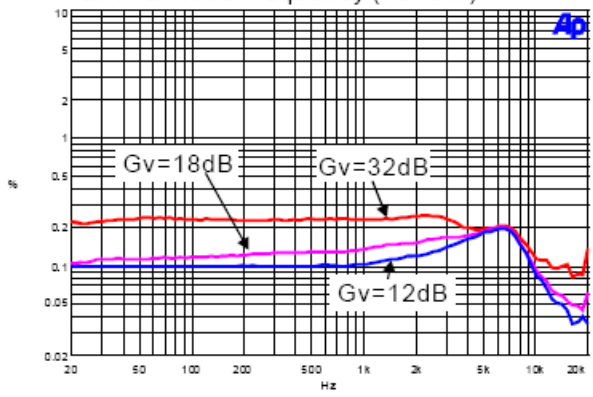
11. THD+N vs Frequency (Po=1W)



9. THD+N vs. Power

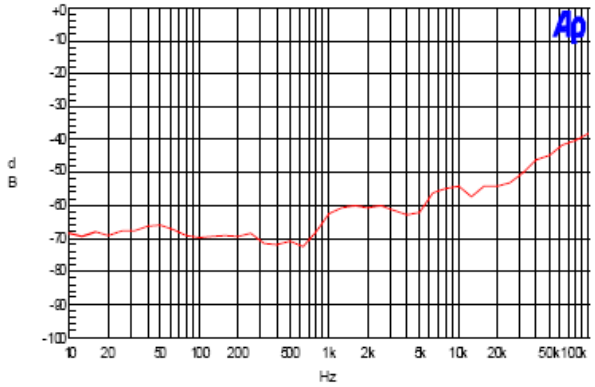


12. THD+N vs Frequency (Po=3W)

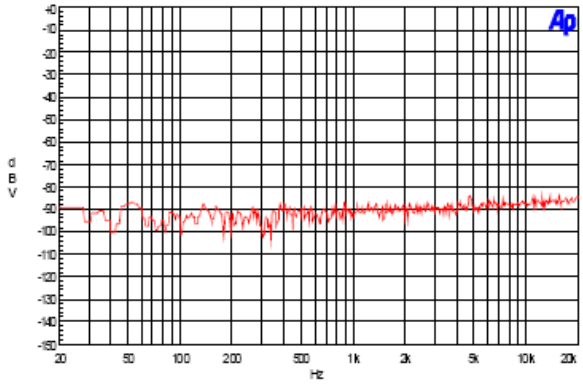


Typical Performance Characteristics (cont.) (@T_A = +25°C, V_{DD} = 12V, R_L = 8Ω, G_V = 24dB, unless otherwise specified.)

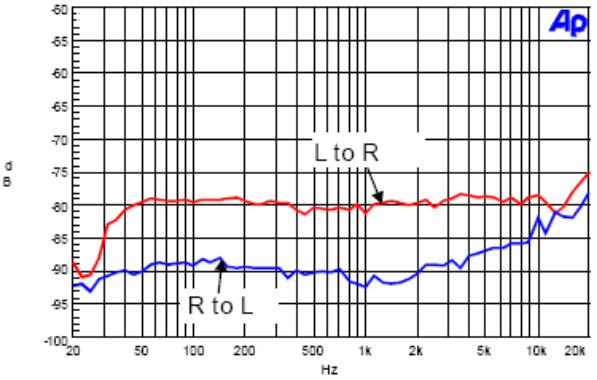
13. Power Supply Ripple Rejection



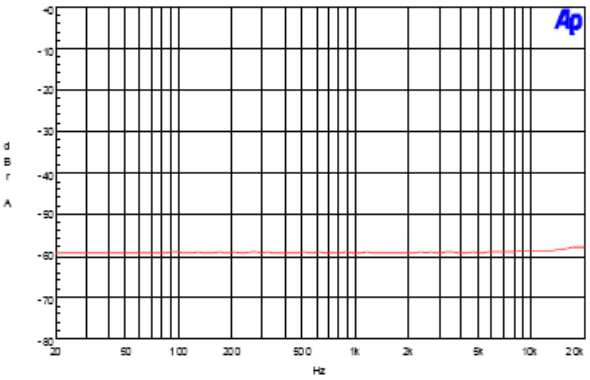
16. Noise Floor



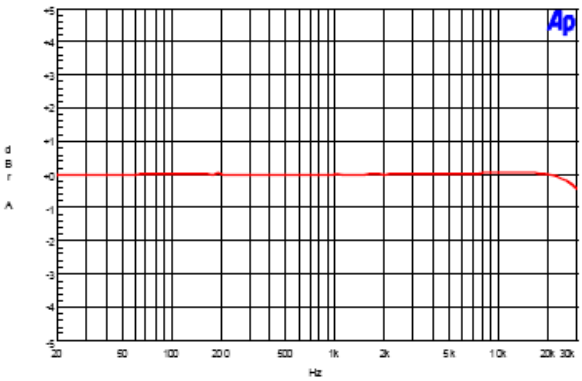
14. Crosstalk



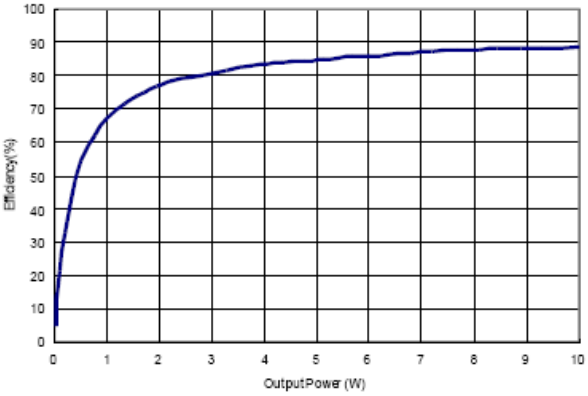
17. CMRR



15. Frequency Response (Vo=1.0Vrms)

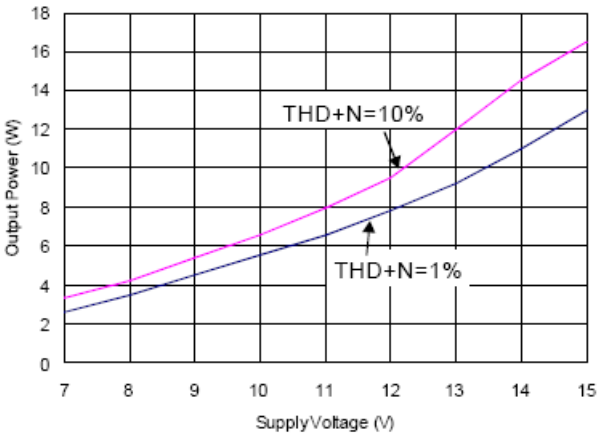


18. Efficiency vs Power

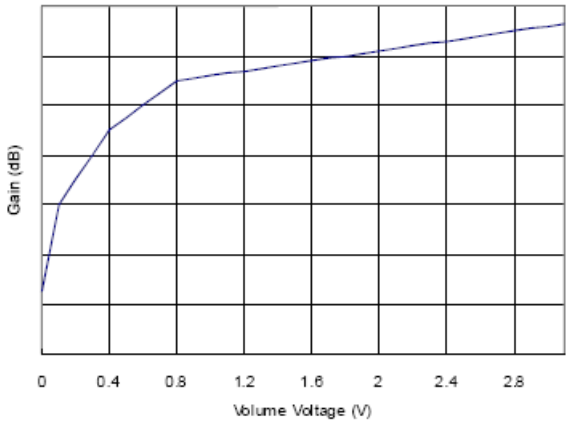


Typical Performance Characteristics (cont.) (@T_A = +25°C, V_{DD} = 12V, R_L = 8Ω, G_V = 24dB, unless otherwise specified.)

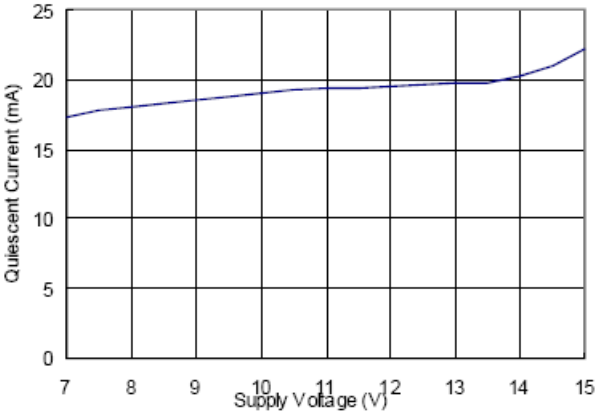
19. Output Power vs Supply Voltage



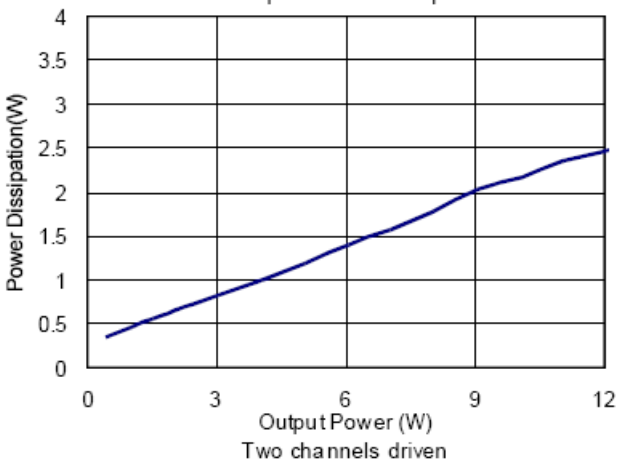
21.Gain vs DC voltage



20. Quesicent Current vs Supply Voltage



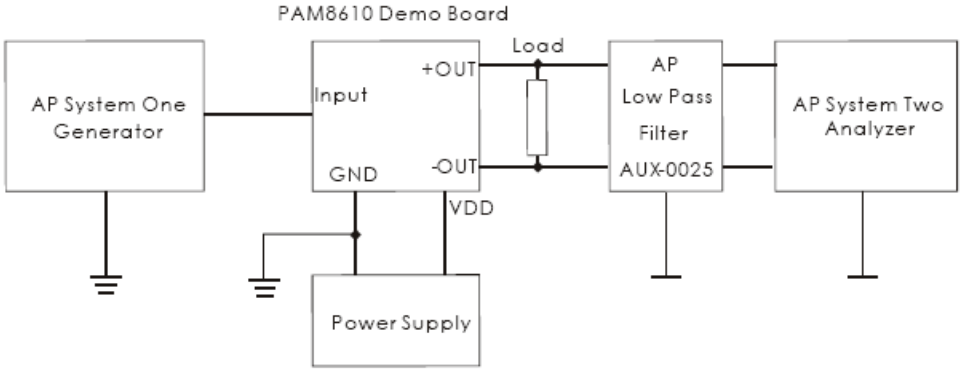
22.Power Dissipation vs. Output Power



Notes: PCB information for power dissipation measurement.
1. The PCB size is 74mm 68mm with 1.2mm thickness, two layers and Fr4.
2. 16 vias at the thermal land on the PCB with 0.5mm diameter.
3. The size of exposed copper is 10mm*10mm with 3oz thickness.

Application Information

Test Setup for Performance Testing



Notes: 4. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
5. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Power and Heat Dissipation

Choose speakers that are able to stand large output power from the PAM8610. Otherwise, speaker may suffer damage.

Heat dissipation is very important when the device works in full power operation. Two factors affect the heat dissipation, the efficiency of the device that determines the dissipation power, and the thermal resistance of the package that determines the heat dissipation capability.

In operation, some of power is dissipated to the resistors.

Power Dissipation: $P_{LOSS} = (P_O*(1-\eta/\eta)*2$

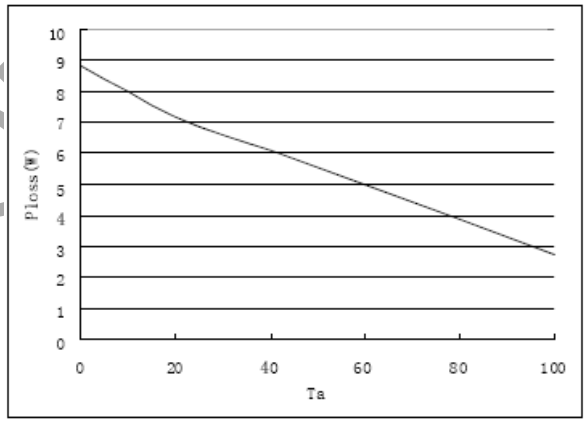
The PAM8610's efficiency is 90% with 10W ouput and 8Ω load. The dissipation power is 2.22W.

Thermal resistance of junction to ambient of the QFN package is 18.1°C/W and the junction temperature $T_J = P_{LOSS} * \theta_{JA}+T_A$, where T_A is ambient temperature. If the ambient temperature is +85°C, the QFN's junction temperature

$T_J = 2.22*18.1 + 85 = +125°C$

which is lower than +150°C rated junction temperature.

If the rated workable junction temperature is 150°C, the relat ionship between ambient temperature and permitted P_{LOSS} is shown in below diagram.



From the diagram, it can be found that when the device works at 10W/8Ω load the dissipation power is 1.1W per channel, 2.2W total, the permitted ambient temperature is over 100°C. This is proven by actual test. The PAM8610 can work in full output power under +85°C ambient temperature.

Application Information (cont.)

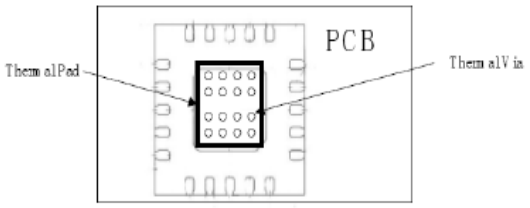
Heat Dissipation in PCB Design

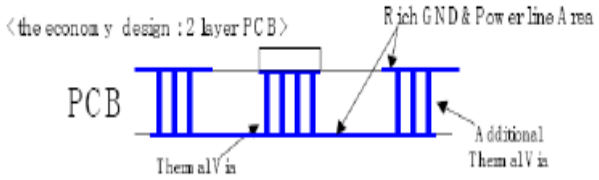
Generally, class-D amplifiers are high efficiency and need no heat sink. For high power ones that has high dissipation power, the heat sink may also not necessary if the PCB is carefully designed to achieve good heat by the PCB itself.

Dual-Side PCB

To achieve good heat, the PCB's copper plate should be thicker than 0.035mm and both sides of the PCB should be utilized for heat sink.

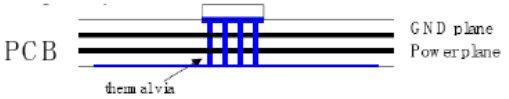
The thermal pad on the bottom of the device should be soldered to the plate of the PCB, and via holes, usually 9 to 16, should be drilled in the PCB area under the device and deposited copper on the vias should be thick enough so that the heat can be dissipated to the other side of the plate. There should be no insulation mask on the other side of the copper plate. It is better to drill more vias around the device if possible.





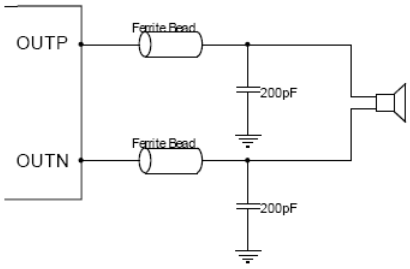
4-Layer PCB

If it is 4-layer PCB, the two middle layers of grounding and power can be employed for heat dissipation, isolating them into serval islands to avoid short between ground and power.



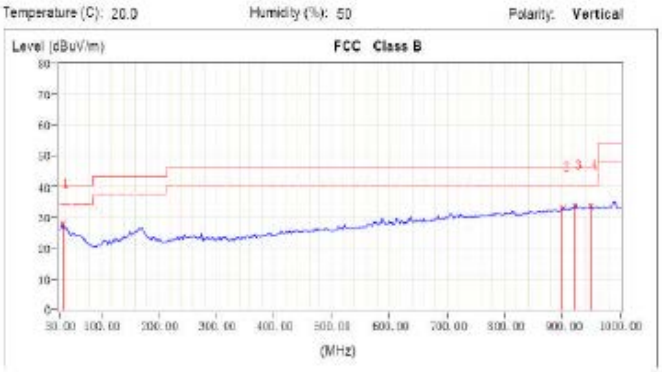
Consideration for EMI

Filters are not required if the traces from the amplifier to the speakers are short (<20cm). But most applications require a ferrite bead filter as shown in below figure. The ferrite bead filter reduces EMI of around 1MHz and higher to meet the FCC and CE's requirements. It is recommended to use a ferrite bead with very low impedances at low frequencies and high impedance at high frequencies (above 1MHz).

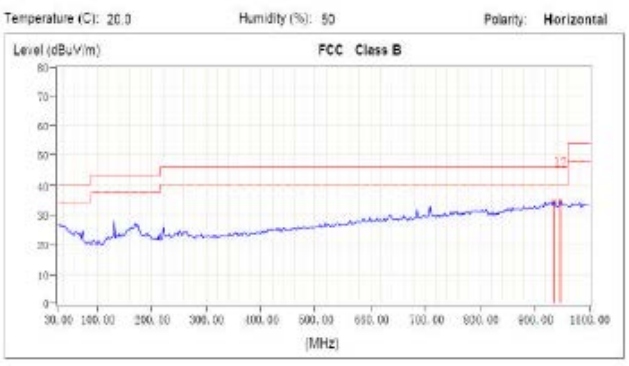


The EMI characteristics are as follows after employing the ferrite bead.

Vertical Polarization



Horizontal Polarization



Application Information (cont.)

Volume Control

A DC volume control section is integrated in PAM8610, controlling via V_{REF}, VOLUME and V_{REFGND} terminals. The voltage on VOLUME pin, without exceeding V_{REF}, determines internal amplifier gain as listed in Table 1.

If a resistor divider is used to fix gain of the amplifier, the V_{REF} terminal can be directly connected to AV_{DD} and the resistor divider connected across V_{REF} and REFGND. For fixed gain, the resistor divider values are to center the voltage given in the Table 1.

FADE Operation

The $\overline{\text{FADE}}$ terminal is a logic input that controls the operation of the volume control circuitry during transitions to and from the shutdown state and during power-up.

A logic low on this terminal will set the amplifier in fade mode. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the volume is smoothly ramped up from the mute state, -75dB, to the desired volume set by the voltage on the volume control terminal. Conversely, the volume is smoothly ramped down from the current state to the mute state when a logic low is applied to the $\overline{\text{SD}}$ terminal. A logic high on this pin disables the volume fade effect during transitions to and from the shutdown state and during power-up. During power-up or recovery from the shutdown state (a logic high is applied to the $\overline{\text{SD}}$ terminal), the transition from the mute state, -75dB, to the desired volume setting is less than 1ms. Conversely, the volume ramps down from current state to the mute state within 1ms when a logic low is applied to the $\overline{\text{SD}}$ terminal.

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8610. A logic high on this pin disables the outputs and low enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.

For power saving, the $\overline{\text{SD}}$ pin should be used to reduce the quiescent current to the absolute minimum level. The volume will fade, increasing or decreasing slowly, when leaving or entering the shutdown state if the $\overline{\text{FADE}}$ terminal is held low. If the $\overline{\text{FADE}}$ terminal is held high, the outputs will transit very quickly. Refer to the $\overline{\text{FADE}}$ operation section.

Shutdown Operation

The PAM8610 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{\text{SD}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SD}}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{\text{SD}}$ should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal 2.5V Bias Generator Capacitor Selection

The internal 2.5V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the Class-D outputs start switching. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the Class-D output switching-on other than that of the startup time. However, at least a 0.47µF capacitor is recommended for the V2P5 capacitor.

Another function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5V bias generator.

Power Supply Decoupling, C_S

The PAM8610 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-seriesresistance (ESR) ceramic capacitor, typically 1µF, is recommended, placing as close as possible to the device's V_{CC} lead. To filter lower-frequency noises, a large aluminum electrolytic capacitor of 10µF or greater is recommended, placing near the audio power amplifier. The 10µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

Application Information (cont.)

Selection of COSC and ROSC

The switching frequency is determined by the values of components connected to R_{OSC} (pin 23) and C_{OSC} (pin 22) and calculated as follows:

$$f_{OSC} = 2\pi / (R_{OSC} * C_{OSC})$$

The frequency may varies from 225kHz to 275kHz by adjusting the values of R_{OSC} and C_{OSC}. The recommended values are C_{OSC} = 220pF, R_{OSC} = 120kΩ for a switching frequency of 250kHz.

BSN and BSP Capacitors

The full H-bridge output stages use NMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. At least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from xOUTP to xBSP, and another 220nF capacitor from xOUTN to xBSN. It is recommended to use 1µF BST capacitor to replace 220nF (pin15, pin 16, pin 35 and pin 36) for lower than 100Hz applications.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors not exceeded, two internal regulators are used to clamp the gate voltage. Two 1µF capacitors must be connected from VCLAMPL and VCLAMPR to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used to power any other circuitry.

Internal Regulated 5-V Supply (AVDD)

The AVDD terminal is the output of an internally generated 5V supply, used for the oscillator, preamplifier, and volume control circuitry. It requires a 0.1µF to 1µF capacitor, placed very close to the pin to ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Differential Input

The differential input stage of the amplifier eliminates noises that appear on the two input lines of the channel. To use the PAM8610 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the PAM8610 with a single-ended source, acground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be acgrounded at the audio source other than at the device input for best noise performance.

Using Low-ESR Capacitors

Low- ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

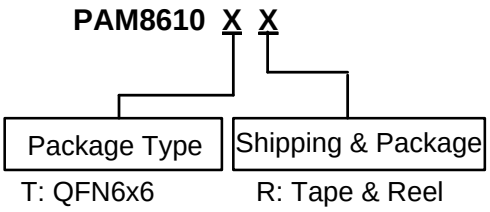
Short-Circuit Protection

The PAM8610 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts, output-to-GND shorts, or output-to-V_{CC} shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on $\overline{SD}$ the pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Thermal Protection

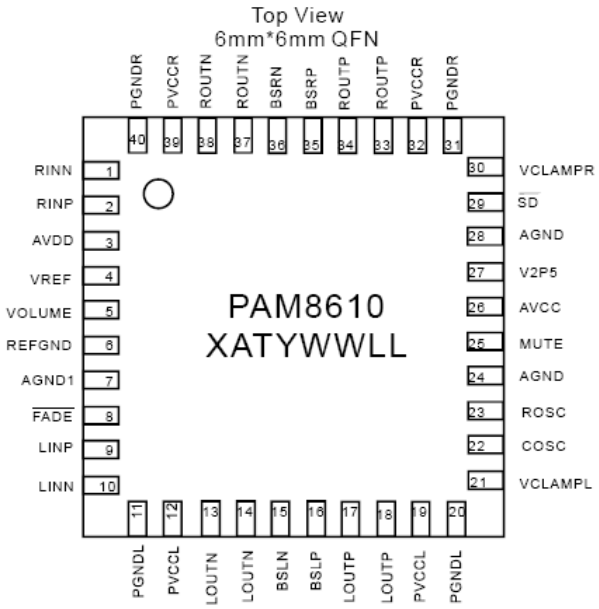
Thermal protection on the PAM8610 prevents damage to the device when the internal die temperature exceeds +150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 40°C. The device begins normal operation at this point without external system intervention.

Ordering Information



Part Number	Part Marking	Package Type	Standard Package
PAM8610TR	PAM8610 XATYWWLL	QFN6x6-40	2500 Units/Tape&Reel

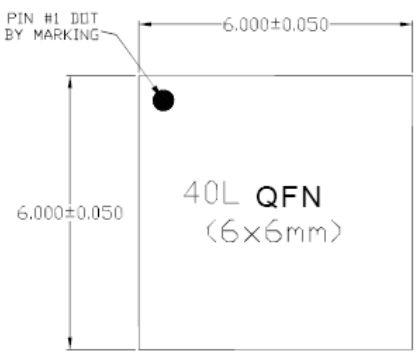
Marking Information



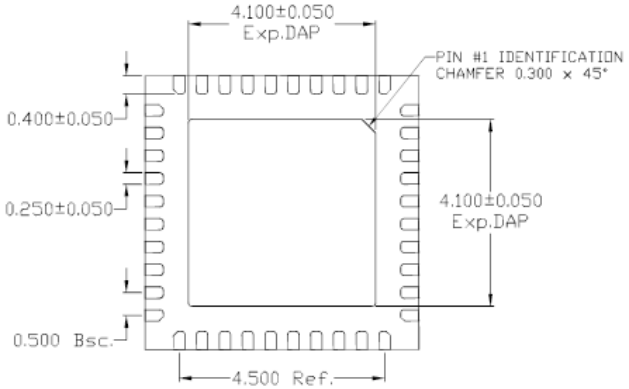
X: Internal Code
A: Internal Code
T: Internal Code
Y: Year
WW: Week
LL: Internal Code

Package Outline Dimensions (All dimensions in mm.)

QFN6x6-40



TOP VIEW



BOTTOM VIEW

NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700

SIDE VIEW

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