

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}).....	12V	16-Pin QSOP (derate 8.3mW/°C above +70°C).....	667mW
IN_A, IN_B, FB_.....($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)		16-Pin Narrow SO (derate 8.7mW/°C above +70°C)...	696mW
REF, EN, A/B.....($V_{EE} - 0.3V$) to ($V_{CC} + 0.3V$)		20-Pin TSSOP (derate 10.9mW/°C above +70°C).....	879mW
Current Into IN_A, IN_B, FB_.....	±20mA	20-Pin Wide SO (derate 10mW/°C above +70°C).....	800mW
Short-Circuit Duration (OUT_ to GND or V_{EE}).....	Continuous	Operating Temperature Range	-40°C to +85°C
Short-Circuit Duration (OUT_ to V_{CC}).....	(Note 1)	Junction Temperature	+150°C
Continuous Power Dissipation ($T_A = +70°C$)		Storage Temperature Range	-65°C to +150°C
14-Pin TSSOP (derate 9.1mW/°C above +70°C)	727mW	Lead Temperature (soldering, 10s)	+300°C
14-Pin Narrow SO (derate 8.3mW/°C above +70°C)	667mW		

Note 1: Do not short OUT_ to V_{CC} .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—Dual Supply

($V_{CC} = +5V$, $V_{EE} = -5V$, $R_L = \infty$, $EN = +5V$, $V_{CM} = REF = OUT_ = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25°C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_S	Guaranteed by PSRR	±2.25		±5.5	V
Quiescent Supply Current	I_S	OUT = 0V	MAX4023/MAX4024	25	36	mA
			MAX4025/MAX4026	34	48	
Disable Supply Current		EN = 0V	MAX4023/MAX4024	3.6	6	mA
			MAX4025/MAX4026	4.4	6	
Input Voltage Range	V_{IN}	MAX4023/MAX4025, inferred from CMRR	V_{EE}		$V_{CC} - 2.8$	V
		MAX4024/MAX4026, inferred from A_{VCL}	$V_{EE} + 2.9$		$V_{CC} - 2.8$	
Input Offset Voltage	V_{OS}	MAX4023/MAX4025		±0.5	±15	mV
		MAX4024/MAX4026		±1	±18	
Input Offset Voltage Matching	ΔV_{OS}	MAX4023/MAX4025		±1		mV
		MAX4024/MAX4026		±1.5		
Input Offset Voltage Drift	TC_{VOS}	MAX4023/MAX4025		15		µV/°C
		MAX4024/MAX4026		23		
Input Bias Current	I_B			4	14	µA
Input Offset Current	I_{OS}	MAX4023/MAX4025		±0.1	±2	µA
Differential Input Resistance	R_{IND}	MAX4023/MAX4025, -10mV < V_{IND} < +10mV		50		kΩ
Input Resistance	R_{IN}	MAX4023/MAX4025, common mode		4.5		MΩ
		MAX4024/MAX4026, single ended		4.5		
Output Resistance	R_{OUT}	MAX4023/MAX4025	Open loop	18		Ω
			Closed loop, $A_{VCL} = +1$	0.025		
		MAX4024/MAX4026		0.15		

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MAX4023-MAX4026

DC ELECTRICAL CHARACTERISTICS—Dual Supply (continued)

($V_{CC} = +5V$, $V_{EE} = -5V$, $R_L = \infty$, $EN = +5V$, $V_{CM} = REF = OUT_- = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Disable Output Resistance	R_{OUT}	MAX4023/MAX4025, $EN = 0V$		75		k Ω
		MAX4024/MAX4026, $EN = 0V$		1		
Power-Supply Rejection Ratio	PSRR	$\pm 2.25V < V_S < \pm 5.5V$	50	64		dB
Common-Mode Rejection Ratio	CMRR	MAX4023/MAX4025, $V_{EE} < V_{CM} < V_{CC} - 2.8V$	50	68		dB
Open-Loop Gain	A_{VOL}	MAX4023/MAX4025, $R_L = 150\Omega$, $-4.3V < V_{OUT} < +4.3V$	70	85		dB
Voltage Gain	A_{VCL}	MAX4024/MAX4026, $R_L = 150\Omega$, $V_{EE} + 2.9V < V_{IN} < V_{CC} - 2.8V$	5.5	6.0	6.5	dB
Gain Matching	ΔA_{VCL}	MAX4024/MAX4026		1		%
Output Voltage Swing	V_{OUT}	MAX4023/MAX4025	$R_L = 150\Omega$	$V_{CC} - 0.7$	$V_{CC} - 0.5$	V
				$V_{EE} + 0.5$	$V_{EE} + 0.7$	
		$R_L = 75\Omega$	$V_{CC} - 1.2$	$V_{CC} - 0.8$		
			$V_{EE} + 0.8$	$V_{EE} + 1.2$		
		MAX4024/MAX4026	$R_L = 150\Omega$	$V_{CC} - 0.7$	$V_{CC} - 0.5$	
				$V_{EE} + 0.3$	$V_{EE} + 0.7$	
$R_L = 75\Omega$	$V_{CC} - 1.2$	$V_{CC} - 0.8$				
		$V_{EE} + 0.5$	$V_{EE} + 1.2$			
LOGIC INPUT CHARACTERISTICS						
Logic-Low Threshold	V_{IL}	EN, A/B			$V_{CC} - 3.85$	V
Logic-High Threshold	V_{IH}	EN, A/B			$V_{CC} - 3.3$	V
Logic-Low Input Current	I_{IL}	EN, A/B; EN or A/B = 0V		5	10	μA
Logic-High Input Current	I_{IH}	EN, A/B; EN or A/B = V_{CC}		2	8	μA

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DC ELECTRICAL CHARACTERISTICS—Single Supply

($V_{CC} = +5V$, $V_{EE} = 0V$, $R_L = \infty$, $EN = +5V$, $V_{CM} = REF = OUT = 0.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_S	Guaranteed by PSRR	4.5		11	V
Quiescent Supply Current	I_S	MAX4023/MAX4024, $OUT = 0V$		19	32	mA
		MAX4025/MAX4026, $OUT = 0V$		31	43	
Disable Supply Current		MAX4023/MAX4024, $EN = 0V$		3.3	6	mA
		MAX4025/MAX4026, $EN = 0V$		3.9	6	
Input Voltage Range	V_{IN}	MAX4023/MAX4025, inferred from CMRR	V_{EE}		$V_{CC} - 2.8$	V
		MAX4024/MAX4026, inferred from A_{VCL}	$V_{EE} + 0.28$		$V_{CC} - 2.8$	
Input Offset Voltage	V_{OS}	MAX4023/MAX4025		± 1	± 18	mV
		MAX4024/MAX4026		± 3	± 20	
Input Offset Voltage Matching	ΔV_{OS}	MAX4023/MAX4025		± 1		mV
		MAX4024/MAX4026		± 1.5		
Input Offset Voltage Drift	TC_{VOS}	MAX4023/MAX4025		9		$\mu V/^\circ C$
		MAX4024/MAX4026		13		
Input Bias Current	I_B			4.5	14	μA
Input Offset Current	I_{OS}	MAX4023/MAX4025		± 0.1	± 2	μA
Differential Input Resistance	R_{IND}	MAX4023/MAX4025, $-10mV < V_{IND} < +10mV$		50		$k\Omega$
Input Resistance	R_{IN}	MAX4023/MAX4025, common mode		4.5		$M\Omega$
		MAX4024/MAX4026, single ended		4.5		
Output Resistance	R_{OUT}	MAX4023/MAX4025	Open loop	18		Ω
			Closed loop, $A_{VCL} = +1$	0.025		
		MAX4024/MAX4026		0.15		
Disable Output Resistance	R_{OUT}	MAX4023/MAX4025, $EN = 0V$		75		$k\Omega$
		MAX4024/MAX4026, $EN = 0V$		1		
Power-Supply Rejection Ratio	PSRR	$\pm 4.5V < V_S < \pm 11V$	50	64		dB
Common-Mode Rejection Ratio	CMRR	MAX4023/MAX4025, $V_{EE} < V_{CM} < V_{CC} - 2.8V$	50	91		dB
Open-Loop Gain	A_{VOL}	MAX4023/MAX4025, $R_L = 150\Omega$, $0.3V < V_{OUT} < 4.3V$	70	85		dB
Voltage Gain	A_{VCL}	MAX4024/MAX4026, $R_L = 150\Omega$, $V_{EE} + 0.28V < V_{IN} < V_{CC} - 2.8V$	5.5	6.0	6.5	dB
Gain Matching	ΔA_{VCL}	MAX4024/MAX4026		1		%

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MAX4023-MAX4026

DC ELECTRICAL CHARACTERISTICS—Single Supply (continued)

($V_{CC} = +5V$, $V_{EE} = 0V$, $R_L = \infty$, $EN = +5V$, $V_{CM} = REF = OUT = 0.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OUT}	MAX4023/MAX4025	$R_L = 150\Omega$ to GND	$V_{CC} - 1.1$	$V_{CC} - 0.5$	V
				$V_{EE} + 0.03$	$V_{EE} + 0.175$	
			$R_L = 75\Omega$ to GND	$V_{CC} - 1.1$	$V_{CC} - 0.8$	
				$V_{EE} + 0.03$	$V_{EE} + 0.175$	
		MAX4024/MAX4026	$R_L = 150\Omega$ to GND	$V_{CC} - 1.1$	$V_{CC} - 0.5$	
				$V_{EE} + 0.03$	$V_{EE} + 0.09$	
	$R_L = 75\Omega$ to GND	$V_{CC} - 1.1$	$V_{CC} - 0.8$			
		$V_{EE} + 0.04$	$V_{EE} + 0.08$			
LOGIC INPUT CHARACTERISTICS						
Logic-Low Threshold	V_{IL}	EN, A/B			$V_{CC} - 3.85$	V
Logic-High Threshold	V_{IH}	EN, A/B	$V_{CC} - 3.3$			V
Logic-Low Input Current	I_{IL}	EN, A/B; EN or A/B = 0V		5	10	μA
Logic-High Input	I_{IH}	EN, A/B; EN or A/B = V_{CC}		2	8	μA

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AC ELECTRICAL CHARACTERISTICS—Dual Supply

($V_{CC} = +5V$, $V_{EE} = -5V$, $R_{IN} = 75\Omega$ to GND, $R_L = 150\Omega$ to GND, $EN = +5V$, $V_{CM} = 0V$, $REF = 0V$, $A_{VCL} = +1$ (MAX4023/MAX4025). Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW _{SS}	$V_{OUT} = 100mV_{P-P}$	MAX4023/MAX4025	260		MHz
			MAX4024/MAX4026	200		
Large-Signal -3dB Bandwidth	BW _{LS}	$V_{OUT} = 2V_{P-P}$	MAX4023/MAX4025	85		MHz
			MAX4024/MAX4026	110		
Small-Signal 0.1dB Gain-Flatness Bandwidth	BW _{0.1dBSS}	$V_{OUT} = 100mV_{P-P}$	MAX4023/MAX4025	30		MHz
			MAX4024/MAX4026	32		
Large-Signal 0.1dB Gain-Flatness Bandwidth	BW _{0.1dBLS}	$V_{OUT} = 2V_{P-P}$	MAX4023/MAX4025	22		MHz
			MAX4024/MAX4026	24		
Slew Rate	SR	$V_{OUT} = 2V_{P-P}$	MAX4023/MAX4025	300		V/ μ s
			MAX4024/MAX4026	363		
Settling Time to 0.1%	t _s	$V_{OUT} = 2V$ step	MAX4023/MAX4025	32		ns
			MAX4024/MAX4026	32		
Power-Supply Rejection Ratio	PSRR	f = 100kHz		60		dB
Output Impedance		f = 10MHz		1.5		Ω
Differential Gain Error	DG	NTSC, PAL, $A_{VCL} = +2$	MAX4023/MAX4025	0.012		%
			MAX4024/MAX4026	0.015		
Differential Phase Error	DP	NTSC, PAL, $A_{VCL} = +2$	MAX4023/MAX4025	0.05		Degrees
			MAX4024/MAX4026	0.077		
Group Delay	D/dT	f = 3.58MHz or 4.43MHz, $A_{VCL} = +2$	MAX4023/MAX4025	1.6		ns
			MAX4024/MAX4026	1.8		
Peak Signal to RMS Noise	SNR	$V_{OUT} = 2V_{P-P}$, 10MHz BW, $A_{VCL} = +2$	MAX4023/MAX4025	90		dB
			MAX4024/MAX4026	86		
Crosstalk		f = 10MHz		-61		dB
SWITCHING CHARACTERISTICS						
Channel Switching Time	t _{sw}	MAX4023/MAX4025		25		ns
		MAX4024/MAX4026		25		
Enable Time	t _{ON}	$V_{IN} = 0.5V$		60		ns
Disable Time	t _{OFF}	$V_{IN} = 0.5V$		0.45		μ s
Switching Transient		MAX4023/MAX4025		20		mV _{P-P}
		MAX4024/MAX4026		20		

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MAX4023-MAX4026

AC ELECTRICAL CHARACTERISTICS—Single Supply

($V_{CC} = +5V$, $V_{EE} = 0V$, $R_{IN} = 75\Omega$ to V_{CM} , $R_L = 150\Omega$ to GND, $EN = +5V$, $V_{CM} = 0.5V$, $REF = V_{CM}$, $Av_{CL} = +1$ (MAX4023/MAX4025). Typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

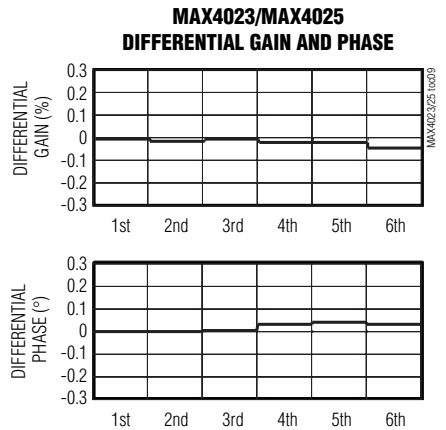
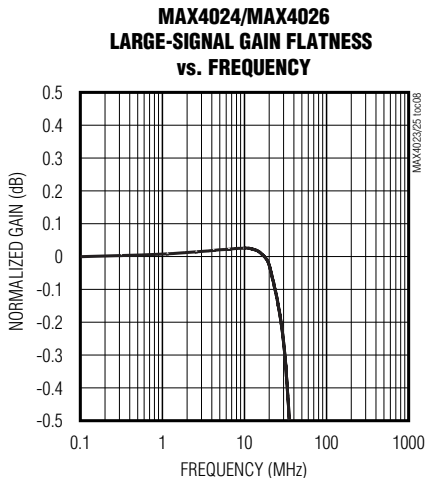
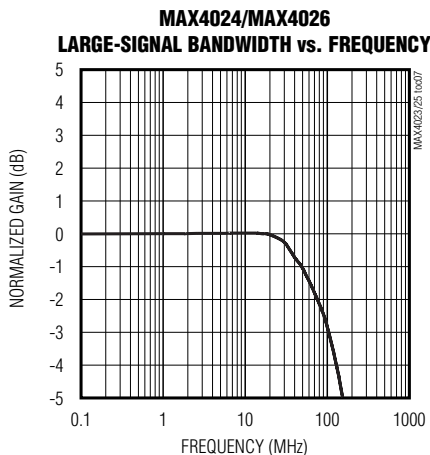
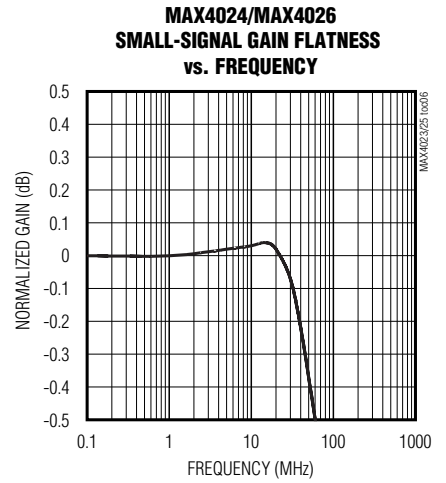
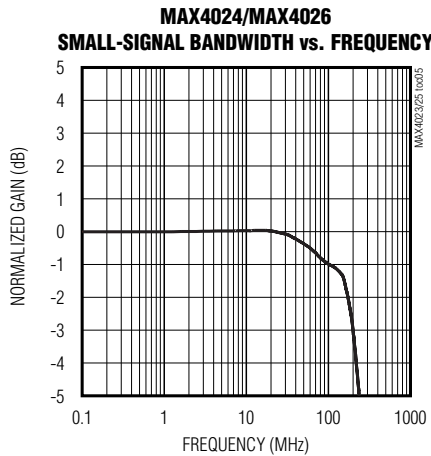
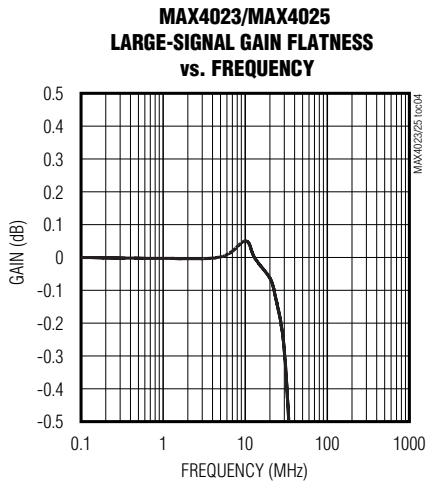
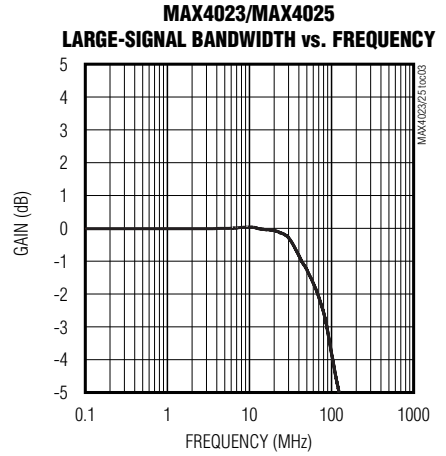
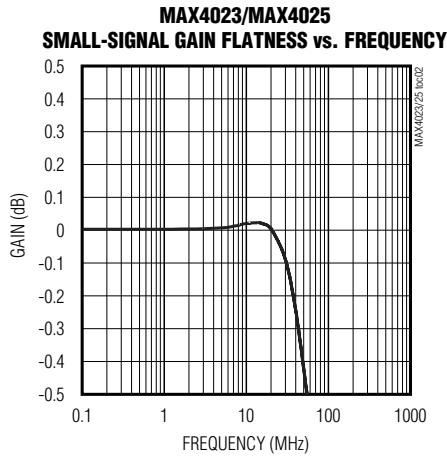
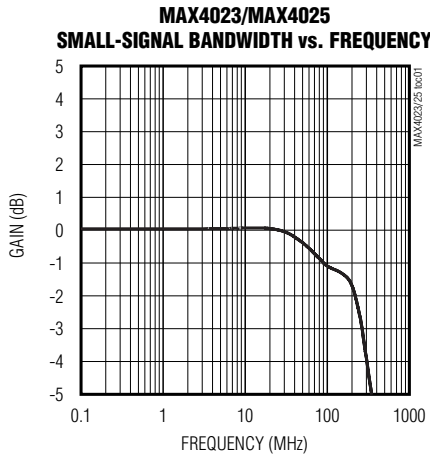
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW _{SS}	V _{OUT} = 100mV _{P-P}	MAX4023/MAX4025	260			MHz
			MAX4024/MAX4026	200			
Large-Signal -3dB Bandwidth	BW _{LS}	V _{OUT} = 2V _{P-P}	MAX4023/MAX4025	83			MHz
			MAX4024/MAX4026	110			
Small-Signal 0.1dB Gain-Flatness Bandwidth	BW _{0.1dBSS}	V _{OUT} = 100mV _{P-P}	MAX4023/MAX4025	40			MHz
			MAX4024/MAX4026	44			
Large-Signal 0.1dB Gain-Flatness Bandwidth	BW _{0.1dBLS}	V _{OUT} = 2V _{P-P}	MAX4023/MAX4025	22			MHz
			MAX4024/MAX4026	25			
Slew Rate	SR	V _{OUT} = 2V _{P-P}	MAX4023/MAX4025	300			V/ μ s
			MAX4024/MAX4026	363			
Settling Time to 0.1%	t _s	V _{OUT} = 2V step	MAX4023/MAX4025	32			ns
			MAX4024/MAX4026	32			
Power-Supply Rejection Ratio	PSRR	f = 100kHz		60			dB
Output Impedance		f = 10MHz		1.5			Ω
Differential Gain Error	DG	NTSC, PAL, Av _{CL} = +2	MAX4023/MAX4025	0.016			%
			MAX4024/MAX4026	0.02			
Differential Phase Error	DP	NTSC, PAL, Av _{CL} = +2	MAX4023/MAX4025	0.054			Degrees
			MAX4024/MAX4026	0.085			
Group Delay	D/dT	f = 3.58MHz or 4.43MHz, Av _{CL} = +2	MAX4023/MAX4025	1.6			ns
			MAX4024/MAX4026	1.9			
Peak Signal to RMS Noise	SNR	V _{OUT} = 2V _{P-P} , 10MHz BW, Av _{CL} = +2	MAX4023/MAX4025	90			dB
			MAX4024/MAX4026	86			
Crosstalk		f = 10MHz		-61			dB
SWITCHING CHARACTERISTICS							
Channel Switching Time	t _{sw}	MAX4023/MAX4025		25			ns
		MAX4024/MAX4026		25			
Enable Time	t _{ON}	V _{IN} = 0.5V		90			ns
Disable Time	t _{OFF}	V _{IN} = 0.5V		0.45			μ s
Switching Transient		MAX4023/MAX4025		10			mV _{P-P}
		MAX4024/MAX4026		10			

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Specifications over temperature are guaranteed by design.

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Typical Operating Characteristics—±5V Dual Supply

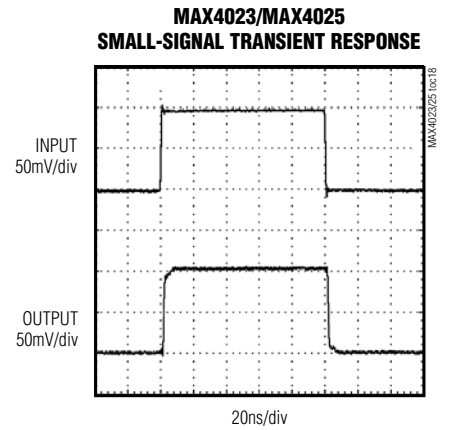
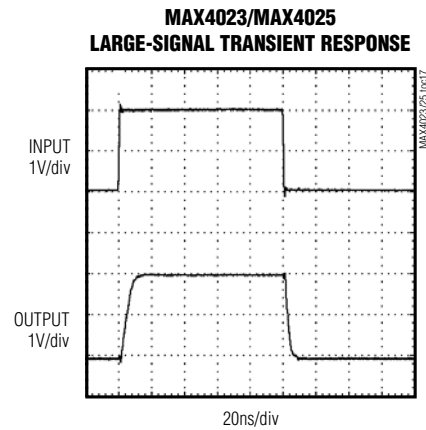
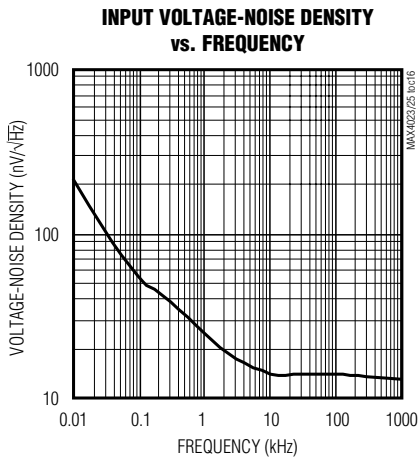
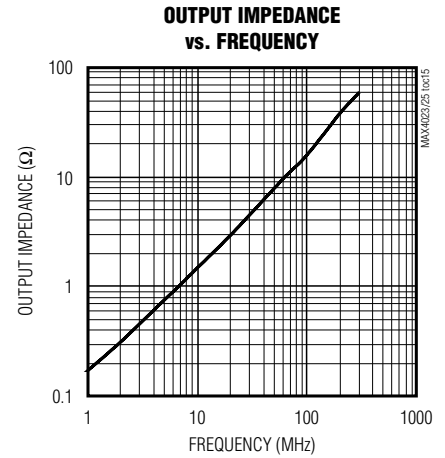
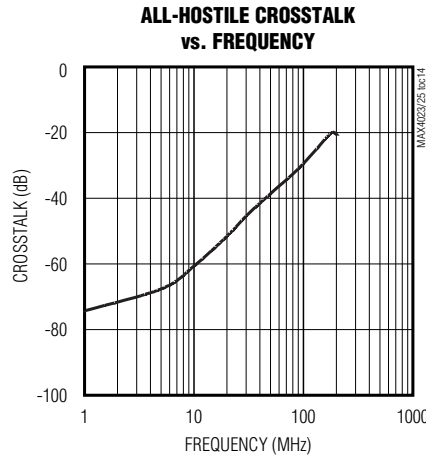
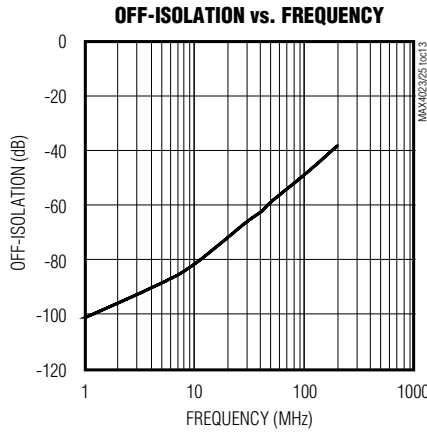
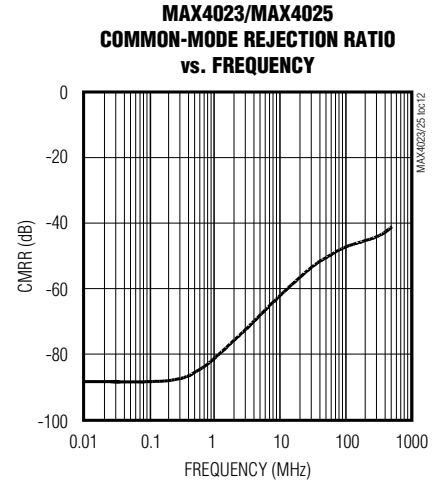
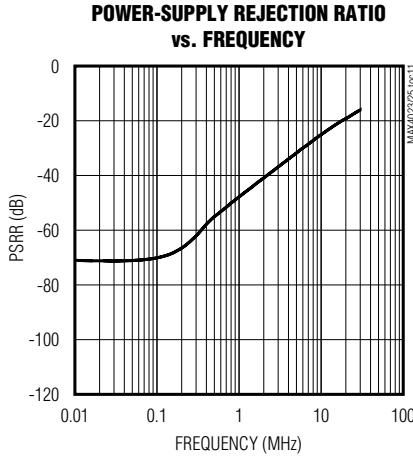
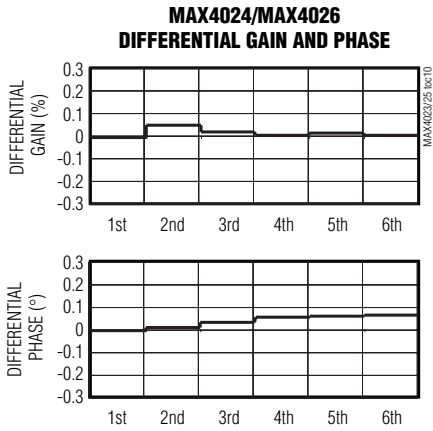
($V_{CC} = +5V$, $V_{EE} = -5V$, $V_{CM} = REF = 0V$, $EN = +5V$, $R_{IN} = 75\Omega$ to GND, $R_L = 150\Omega$ to GND, $A_{VCL} = +1V/V$ (MAX4023/MAX4025), $A_{VCL} = +2V/V$ (MAX4024/MAX4026), $T_A = +25^\circ C$, unless otherwise noted.)



Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Typical Operating Characteristics—±5V Dual Supply (continued)

($V_{CC} = +5V$, $V_{EE} = -5V$, $V_{CM} = REF = 0V$, $EN = +5V$, $R_{IN} = 75\Omega$ to GND, $R_L = 150\Omega$ to GND, $A_{VCL} = +1V/V$ (MAX4023/MAX4025), $A_{VCL} = +2V/V$ (MAX4024/MAX4026), $T_A = +25^\circ C$, unless otherwise noted.)



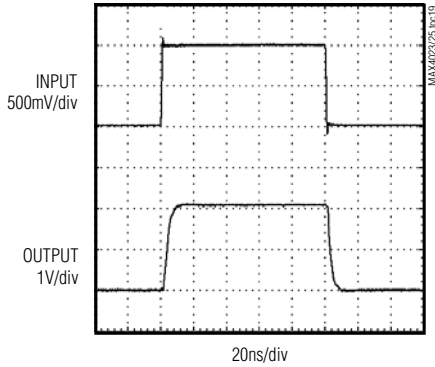
MAX4023-MAX4026

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

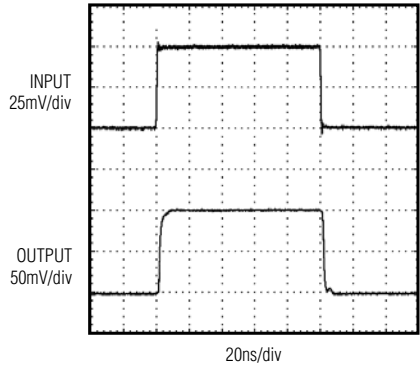
Typical Operating Characteristics—±5V Dual Supply (continued)

($V_{CC} = +5V$, $V_{EE} = -5V$, $V_{CM} = REF = 0V$, $EN = +5V$, $R_{IN} = 75\Omega$ to GND, $R_L = 150\Omega$ to GND, $A_{VCL} = +1V/V$ (MAX4023/MAX4025), $A_{VCL} = +2V/V$ (MAX4024/MAX4026), $T_A = +25^\circ C$, unless otherwise noted.)

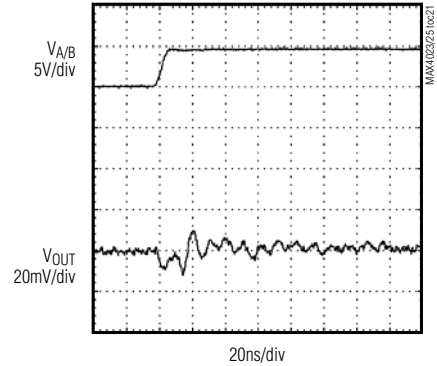
**MAX4024/MAX4026
LARGE-SIGNAL TRANSIENT RESPONSE**



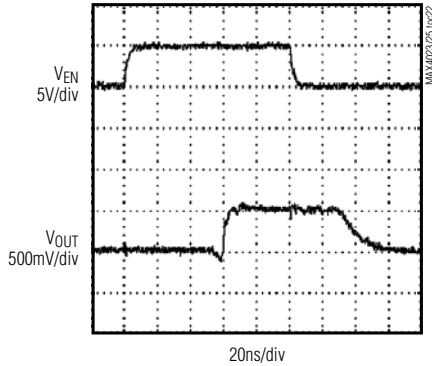
**MAX4024/MAX4026
SMALL-SIGNAL TRANSIENT RESPONSE**



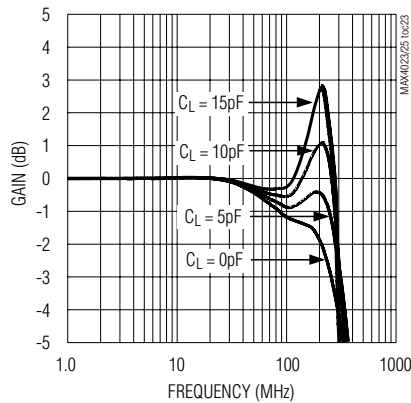
CHANNEL SWITCHING TRANSIENT



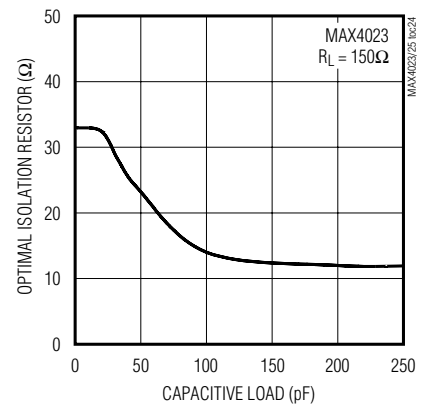
ENABLE RESPONSE TIME



**MAX4023/MAX4025
SMALL-SIGNAL BANDWIDTH
vs. FREQUENCY vs. C_L**



**OPTIMAL ISOLATION RESISTOR
vs. CAPACITIVE LOAD**

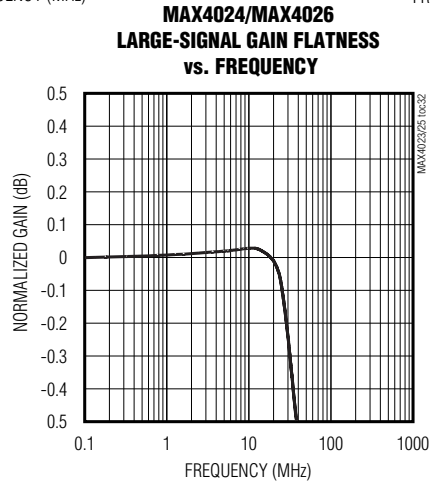
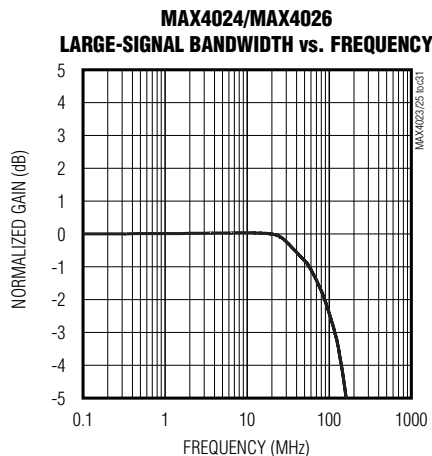
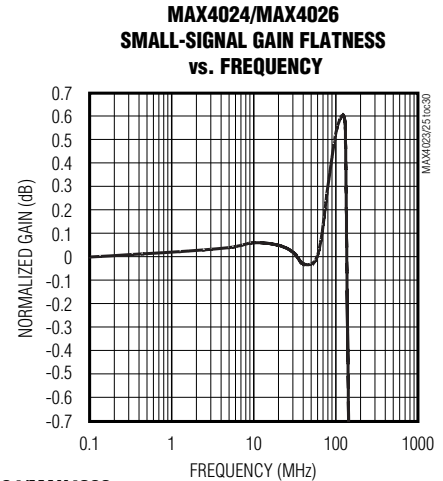
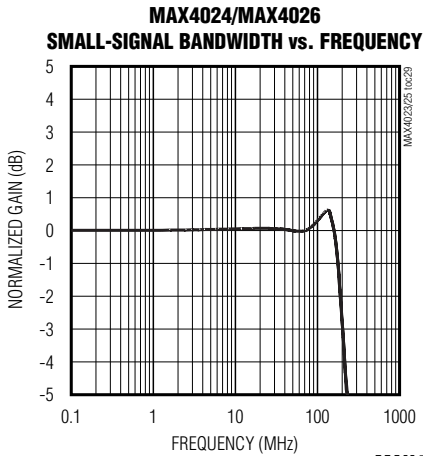
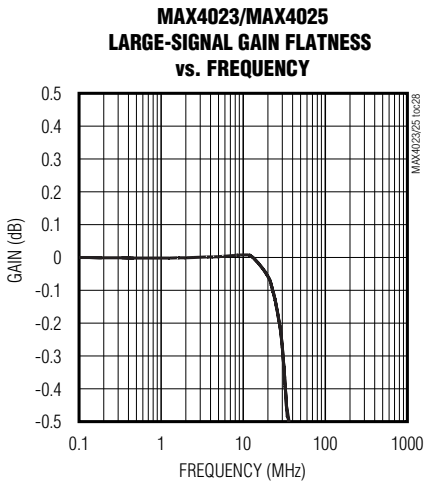
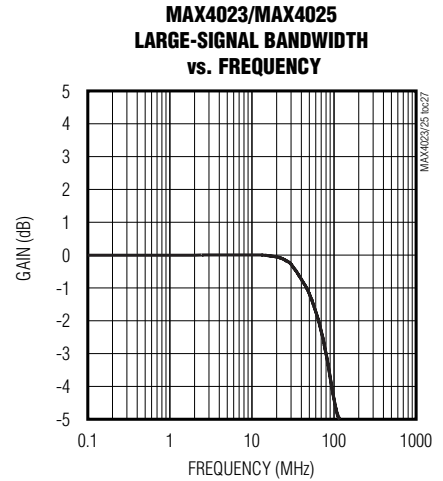
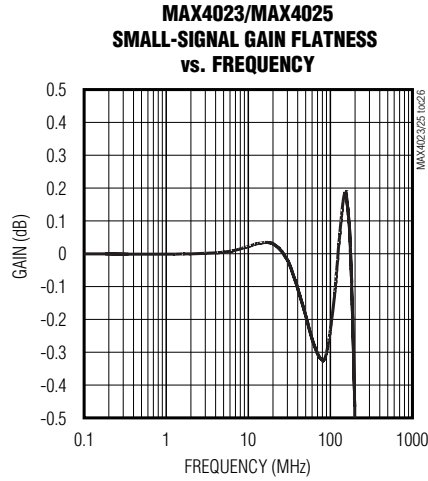
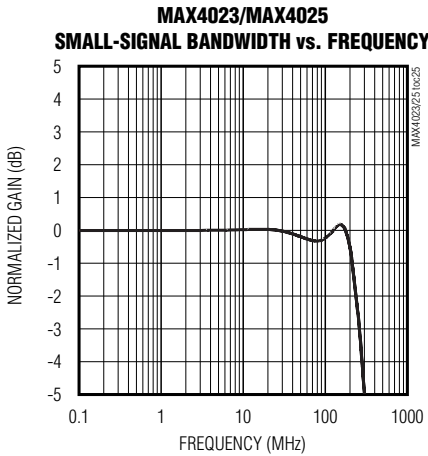


Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Typical Operating Characteristics—+5V Single Supply

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = 0.5V$, $V_{REF} = V_{CM}$, $EN = +5V$, $R_{IN} = 75\Omega$ to V_{CM} , $R_L = 150\Omega$ to GND, $A_{VCL} = +1V/V$ (MAX4023/MAX4025), $A_{VCL} = +2V/V$ (MAX4024/MAX4026), $T_A = +25^\circ C$, unless otherwise noted.)

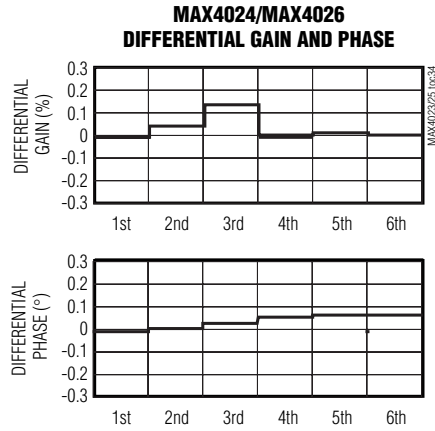
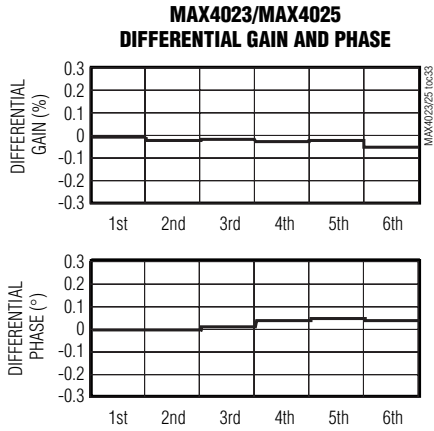
MAX4023-MAX4026



Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Typical Operating Characteristics—+5V Single Supply (continued)

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = 0.5V$, $V_{REF} = V_{CM}$, $EN = +5V$, $R_{IN} = 75\Omega$ to V_{CM} , $R_L = 150\Omega$ to GND, $A_{VCL} = +1V/V$ (MAX4023/MAX4025), $A_{VCL} = +2V/V$ (MAX4024/MAX4026), $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN				NAME	FUNCTION
MAX4023 SO/QSOP	MAX4024 SO/TSSOP	MAX4025 SO/TSSOP	MAX4026 SO/TSSOP		
1	1	1	1	IN1A	Amplifier Input 1A
2	2	2	2	IN2A	Amplifier Input 2A
3	3	3	3	IN3A	Amplifier Input 3A
4	4	5	5, 6	V_{EE}	Negative Power-Supply Voltage. Bypass V_{EE} to GND with a 0.1 μF capacitor. Connect V_{EE} to GND for single-supply operation.
5	13	6	17	A/B	Channel Select Input. Pull A/B high to select channel A. Drive A/B low to select channel B.
6	5	7	7	IN1B	Amplifier Input 1B
7	6	8	8	IN2B	Amplifier Input 2B
8	7	9	9	IN3B	Amplifier Input 3B
9	—	14	—	FB3	Amplifier Feedback Input for Amplifier 3
10	9	13	13	OUT3	Amplifier Output 3
11	10	18	18	OUT2	Amplifier Output 2
12	—	17	—	FB2	Amplifier Feedback Input for Amplifier 2
13	11	15	14	EN	Enable Input. Pull EN high for normal operation. Drive EN low to disable all outputs.

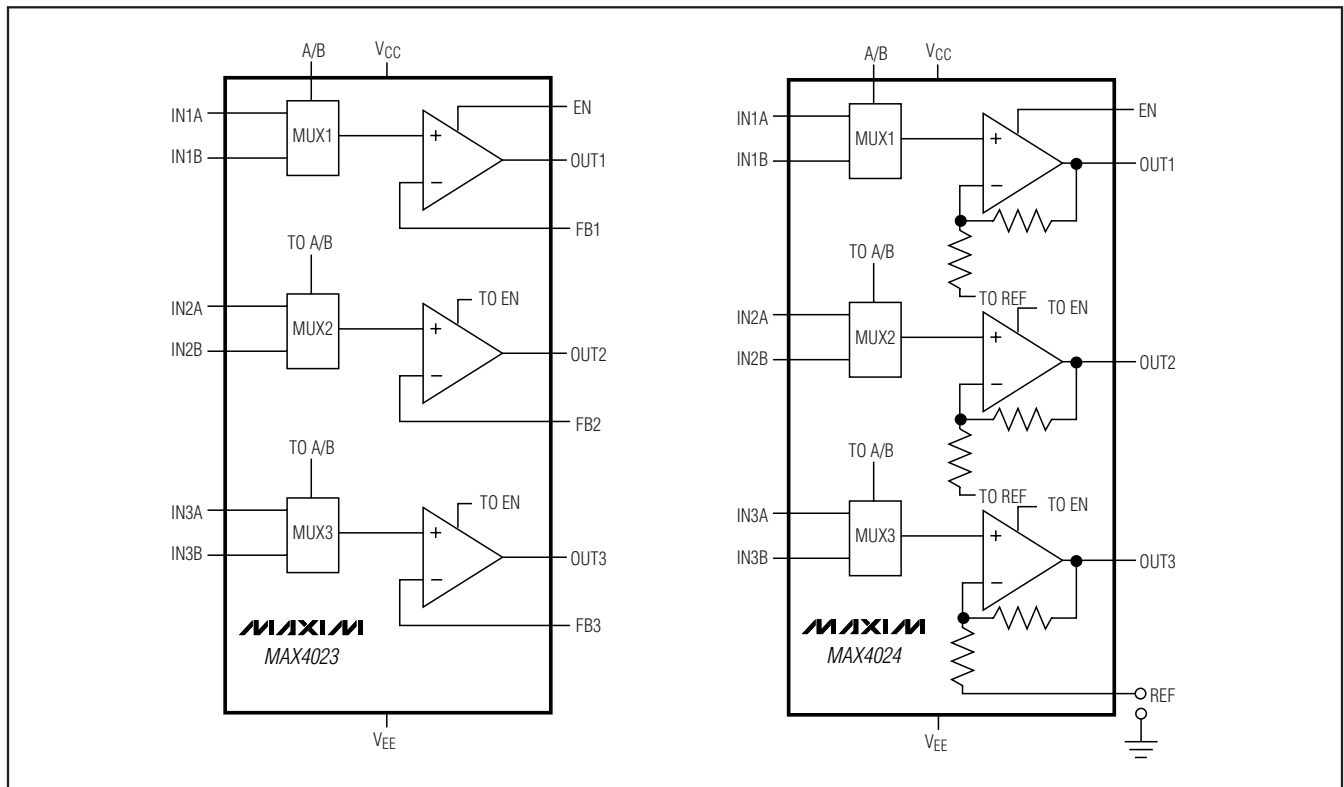
Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Pin Description (continued)

PIN				NAME	FUNCTION
MAX4023 SO/QSOP	MAX4024 SO/TSSOP	MAX4025 SO/TSSOP	MAX4026 SO/TSSOP		
14	12	16	15, 16	V _{CC}	Positive Power-Supply Voltage. Bypass V _{CC} to GND with a 0.1μF capacitor.
15	14	19	19	OUT1	Amplifier Output 1
16	—	20	—	FB1	Amplifier Feedback Input for Amplifier 1
—	8	—	11, 20	REF	Reference Pin for Internal Gain Resistor Network
—	—	4	4	IN4A	Amplifier Input 4A
—	—	10	10	IN4B	Amplifier Input 4B
—	—	11	—	FB4	Amplifier Feedback Input for Amplifier 4
—	—	12	12	OUT4	Amplifier Output 4

MAX4023-MAX4026

Functional Diagrams



Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Detailed Description

The MAX4024/MAX4026 combine three and four 2:1 multiplexers, respectively, with a fixed gain of 2 amplifier. The MAX4023/MAX4025 combine three and four 2:1 multiplexers, respectively, with an adjustable gain output amplifier optimized for a closed-loop gain of +1 or greater. These devices operate from a single-supply voltage of +4.5V to +11V or from dual supplies of $\pm 2.25\text{V}$ to $\pm 5.5\text{V}$. The outputs may be placed in a high-impedance state and the supply current minimized by forcing the EN pin low. The input multiplexers feature short 25ns channel-switching times and small 10mV_{P-P} switching transients. These devices feature voltage-feedback output amplifiers that achieve up to 363V/ μs slew rates and up to 220MHz -3dB bandwidths. They also feature excellent differential gain/phase performance.

The MAX4023–MAX4026 feature an A/B pin, which is an input pin for selecting either channel A or B. Drive A/B high to select channel A or drive A/B low to select channel B. Channel A is automatically selected if A/B is left unconnected.

Applications Information

Feedback and Gain Resistor Selection (MAX4023/MAX4025)

Select the MAX4023/MAX4025 gain-setting feedback R_F and R_G resistors to fit your application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros, and can decrease bandwidth or cause oscillations.

Stray capacitance at the FB pin produces peaking in the frequency-response curve. Keep the capacitance at FB as low as possible by using surface-mount resistors and by avoiding the use of a ground plane beneath or beside these resistors and the FB pin. Some capacitance is unavoidable. If necessary, its effects can be neutralized by adjusting R_F . Use 1% resistors to maintain gain accuracy.

Low-Power Shutdown Mode

All parts feature a low-power shutdown mode that is activated by driving the EN input low. Placing the amplifier in shutdown mode reduces the quiescent supply current to below 4mA and places the output into a high-impedance state, typically 75k Ω (MAX4023/MAX4025). Multiple devices may be paralleled to construct larger switch matrices by connecting the outputs of several devices together and disabling all but one of the paralleled amplifiers' outputs.

For MAX4023/MAX4025 application circuits operating with a closed-loop gain of +1 or greater, consider the external-feedback network impedance of all devices used in the mux application when calculating the total load on the output amplifier of the active device. The MAX4024/MAX4026 have a fixed gain of +2 that is internally set with two 500 Ω thin-film resistors. The impedance of the internal feedback resistors must be taken into account when operating multiple MAX4024/MAX4026s in large multiplexer applications.

For normal operation, drive EN high. Note that the MAX4023–MAX4026 have internal pullup circuitry on EN, so if left unconnected, it is automatically pulled up to VCC.

Layout and Power-Supply Bypassing

The MAX4023–MAX4026 have high bandwidths and consequently require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible, with one exception: The feedback (FB) should have as low a capacitance to ground as possible. Whether or not a constant-impedance board is used, it is best to observe the following guidelines when designing the board:

- 1) Do not use wire-wrapped boards or breadboards.
- 2) Do not use IC sockets; they increase parasitic capacitance and inductance.
- 3) Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
- 4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
- 5) Use surface-mount components. They generally have shorter bodies and lower parasitic reactance, yielding better high-frequency performance than through-hole components.

The bypass capacitors should include a 0.1 μF ceramic surface-mount capacitor between each supply pin and the ground plane, located as close to the package as possible. Optionally, place a 10 μF tantalum capacitor at the power-supply's point of entry to the PC board to ensure the integrity of incoming supplies. The power-supply traces should lead directly from the tantalum capacitor to the VCC and VEE pins. To minimize para-

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

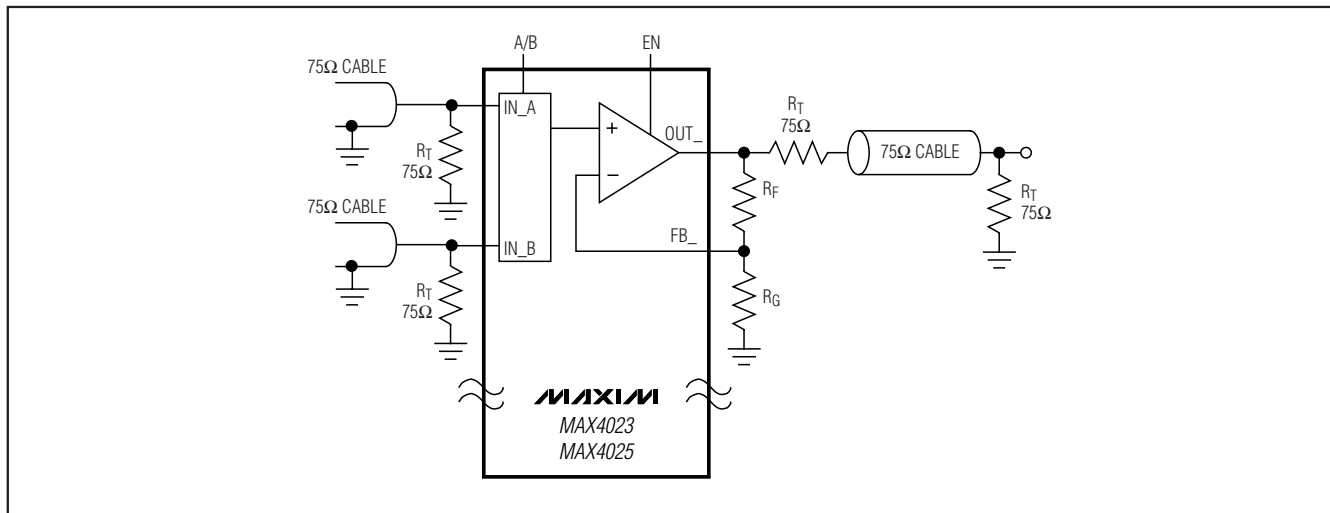


Figure 1. MAX4023/MAX4025 Noninverting Gain Configuration

sitic inductance, keep PC traces short and use surface-mount components.

If input termination resistors and output back-termination resistors are used, they should be surface-mount types, and should be placed as close to the IC pins as possible.

Video Line Driver

The MAX4024/MAX4026 are well suited to drive short coaxial transmission lines when the cable is terminated at both ends (as shown in Figure 2a) where the fixed gain of +2 compensates for the loss in the resistors. The MAX4023/MAX4025 have settable gain to equalize long cables. The MAX4023/MAX4025 allow adding functions that normally require additional op amps. For example, a cable driver can “boost” the high frequencies for long runs, making the part perform multiple functions. Figure 2b shows the “cable booster” using the MAX4023/MAX4025.

Driving Capacitive Loads

A correctly terminated transmission line is purely resistive and presents no capacitive load to the amplifier.

Reactive loads decrease phase margin and may produce excessive ringing and oscillation (see *Typical Operating Characteristics*).

Another concern when driving capacitive loads is the amplifier’s output impedance, which appears inductive at high frequencies. This inductance forms an L-C resonant circuit with the capacitive load, which causes peaking in the frequency response and degrades the amplifier’s phase margin.

Although the MAX4023-MAX4026 are optimized for AC performance and are not designed to drive highly capacitive loads, they are capable of driving up to 33pF without oscillations. However, some peaking may occur in the frequency domain (Figure 3). To drive larger capacitive loads or to reduce ringing, add an isolation resistor between the amplifier’s output and the load (Figure 4). The value of R_{ISO} depends on the circuit’s gain and the capacitive load (Figure 5). Also note that the isolation resistor forms a divider that decreases the voltage delivered to the load.

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

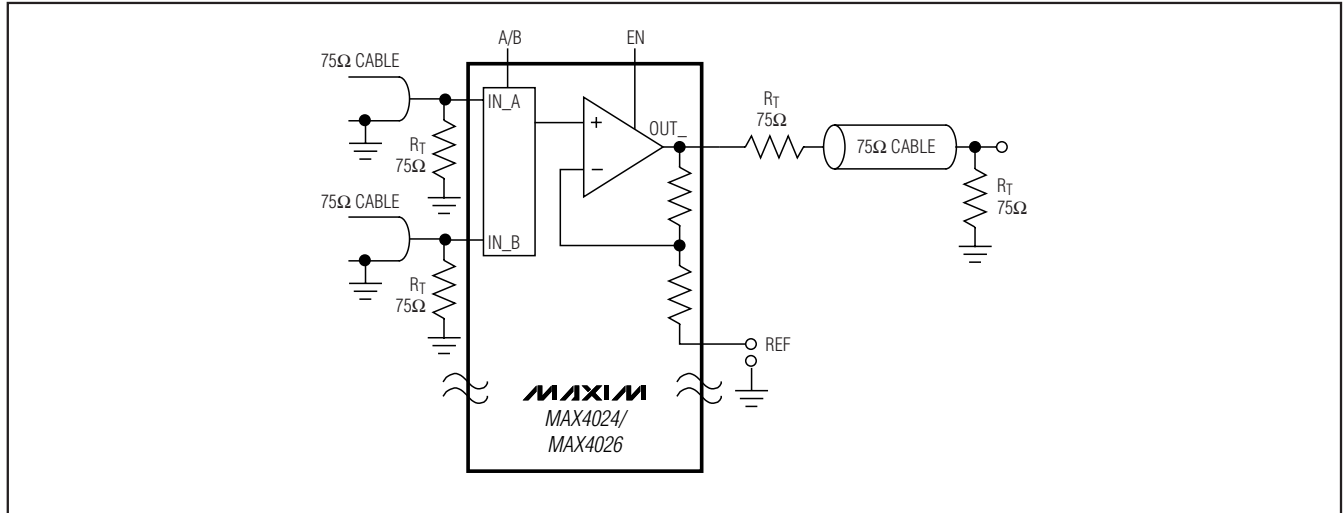


Figure 2a. Video Line Driver

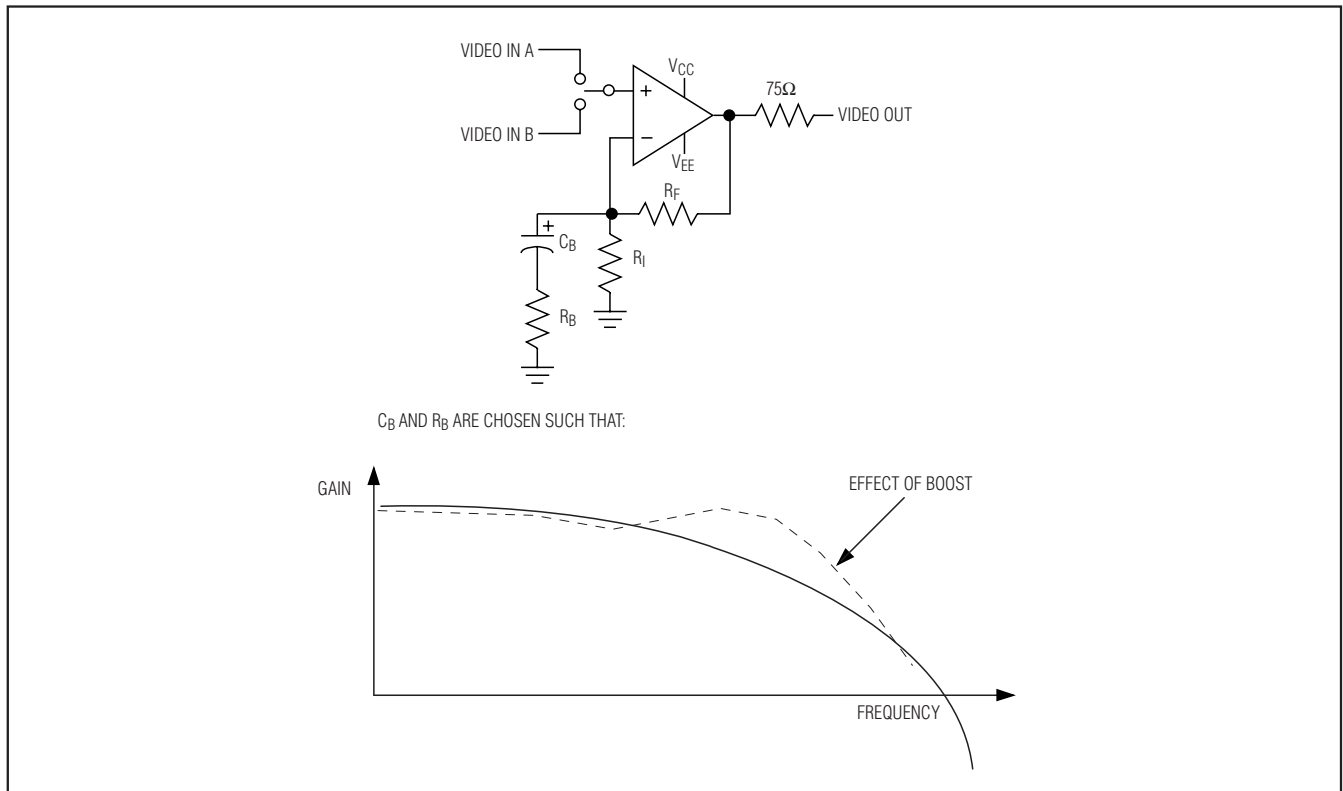


Figure 2b. Cable Booster Using the MAX4023/MAX4025

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

MAX4023-MAX4026

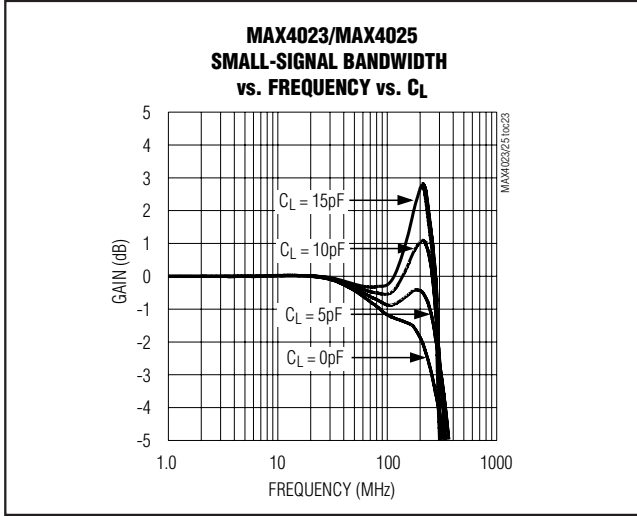


Figure 3. Small-Signal Bandwidth vs. Frequency with Capacitive Load and No Isolation Resistor

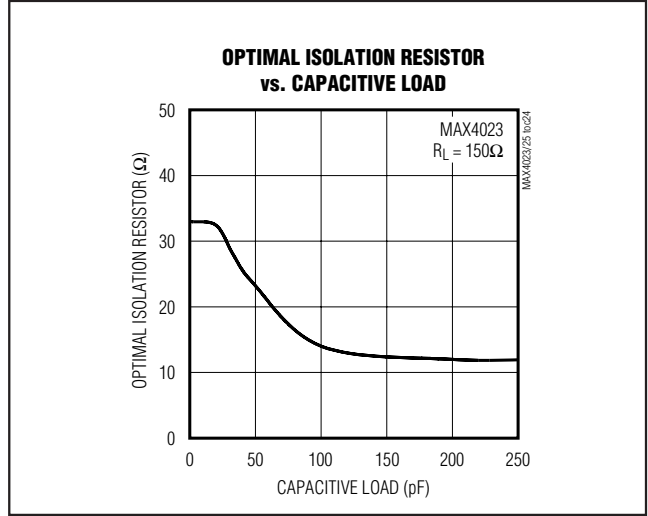


Figure 5. Optimal Isolation Resistance vs. Capacitive Load

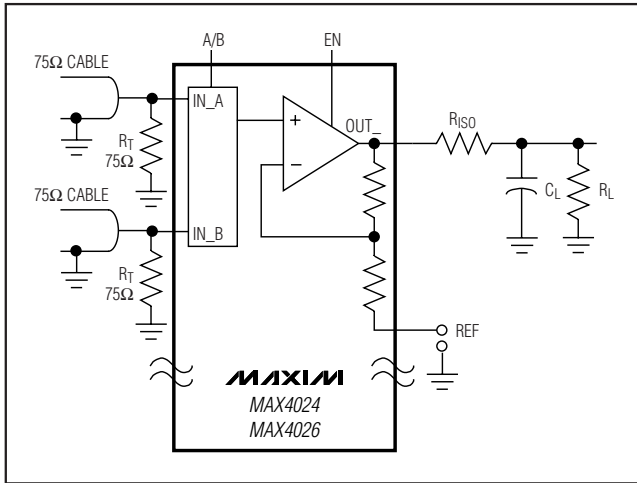


Figure 4. Using an Isolation Resistor (R_{ISO}) for a High-Capacitive Load

Selector Guide

PART	PIN-PACKAGE	NO. OF VIDEO MUX-AMPS	AMPLIFIER GAIN (V/V)
MAX4023	16 SO/QSOP	3	$\geq +1$
MAX4024	14 SO/TSSOP	3	+2
MAX4025	20 SO/TSSOP	4	$\geq +1$
MAX4026	20 SO/TSSOP	4	+2

Chip Information

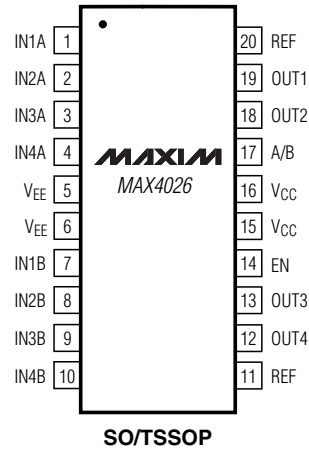
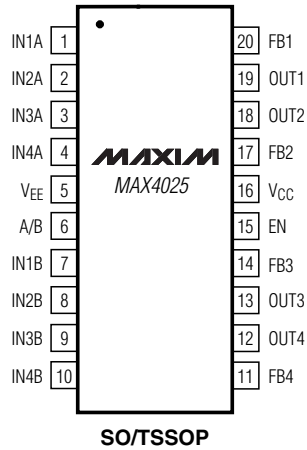
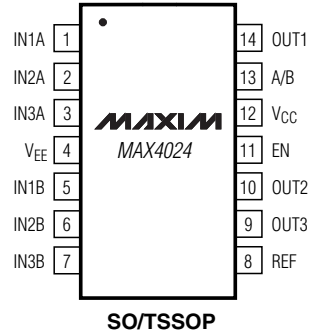
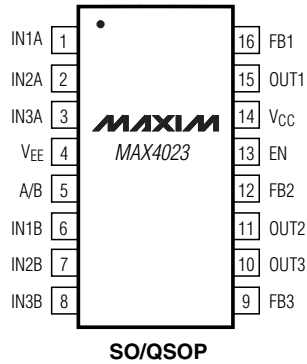
TRANSISTOR COUNT: 655

PROCESS: Bipolar

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Pin Configurations

TOP VIEW



Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
14, 20 TSSOP	U14-2, U20-2	21-0066
14, 16 SOIC	S14-1, S16-1	21-0041
16 QSOP	E16-1	21-0055
20 SOIC	W20-1	21-0042

MAX4023-MAX4026

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	.043	—
A ₁	0.05	0.15	.002	.006
A ₂	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b ₁	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c ₁	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N	PKG. CODES	VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	U14-1; U14-2	4.90	5.10	.193	.201
AB	16	U16-1; U16-2	4.90	5.10	.193	.201
AC	20	U20-2; U20M-2 U20-3	6.40	6.60	.252	.260
AD	24	U24-1	7.70	7.90	.303	.311
AE	28	U28-1; U28-2; U28-3	9.60	9.80	.378	.386

NOTES

- DIMENSIONS D AND E DO NOT INCLUDE FLASH
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
- CONTROLLING DIMENSION: MILLIMETER
- MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
- 'N' REFERS TO NUMBER OF LEADS
- LEAD COPLANARITY 0.10 MM MAX.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
- BENT LEAD 0.10 MM MAX.
- ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

TITLE:
PACKAGE OUTLINE,
TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO. 21-0066	REV. J	1/1
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Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Package Information (continued)

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

SOICN .EPS

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

NOTES:

- D&E DO NOT INCLUDE MOLD FLASH.
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
- LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
- CONTROLLING DIMENSION: MILLIMETERS.
- MEETS JEDEC MS012.
- N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, .150" SOIC

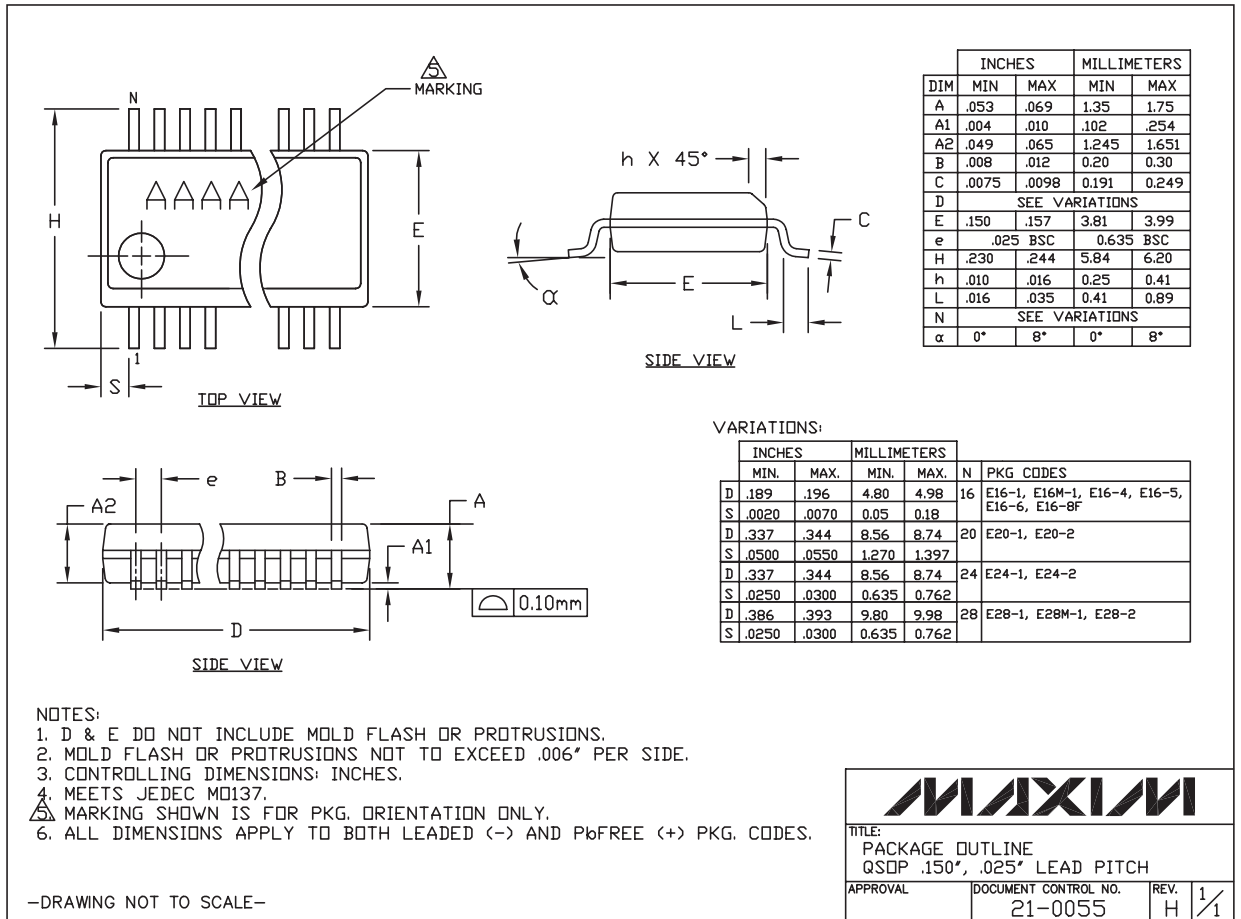
APPROVAL	DOCUMENT CONTROL NO. 21-0041	REV. B	1/1
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Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Package Information (continued)

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

MAX4023-MAX4026



QSOP EPSS

Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Package Information (continued)

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

SOICWEP5

TOP VIEW

FRONT VIEW

SIDE VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS013
	MIN	MAX	MIN	MAX		
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS013.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, .300" SOIC

APPROVAL	DOCUMENT CONTROL NO. 21-0042	REV. B 1/1
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Triple and Quad, 2:1 Video Multiplexer-Amplifiers with Fixed and Settable Gain

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/03	Initial release	—
1	11/09	Updated TOC16	9

MAX4023-MAX4026

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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[MAX4024EUD+](#) [MAX4024EUD+T](#) [MAX4025EUP+](#) [MAX4025EUP+T](#) [MAX4025EWP+](#) [MAX4025EWP+T](#)
[MAX4026EUP+](#) [MAX4026EUP+T](#) [MAX4026EWP+](#)