

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND	-0.3V, +6V
REF, OUT, FB to GND	-0.3V to (V <sub>DD</sub> + 0.3V)
Digital Inputs to GND	-0.3V to +6V
Continuous Current into Any Pin	±20mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
μMAX (derate 4.10mW/°C above +70°C)	330mW
CERDIP (derate 8.00mW/°C above +70°C)	640mW

### Operating Temperature Ranges

MAX5352_C_A/MAX5353_C_A	0°C to +70°C
MAX5352_E_A/MAX5353_E_A	-40°C to +85°C
MAX5352BMJA/MAX5353BMJA	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS: MAX5352

(V<sub>DD</sub> = +5V ±10%, REF = 2.5V, GND = 0V, R<sub>L</sub> = 5kΩ, C<sub>L</sub> = 100pF, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE—ANALOG SECTION</b>						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5352A			±0.5	LSB
		MAX5352B			±1.0	
		MAX5352BMJA			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V <sub>OS</sub>			±0.3	±8	mV
Offset-Error Tempco	TCV <sub>OS</sub>			6		ppm/°C
Gain Error (Note 1)	GE			-0.3	±3	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V <sub>DD</sub> ≤ 5.5V			600	μV/V
<b>REFERENCE INPUT</b>						
Reference Input Range	V <sub>REF</sub>		0		V <sub>DD</sub> - 1.4	V
Reference Input Resistance	R <sub>REF</sub>	Code dependent, minimum at code 1554 hex	14	20		kΩ
<b>MULTIPLYING-MODE PERFORMANCE</b>						
Reference -3dB Bandwidth		V <sub>REF</sub> = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V <sub>REF</sub> = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V <sub>REF</sub> = 1Vp-p at 25kHz, code = full scale		77		dB
<b>DIGITAL INPUTS</b>						
Input High Voltage	V <sub>IH</sub>		2.4			V
Input Low Voltage	V <sub>IL</sub>				0.8	V
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0V or V <sub>DD</sub>		0.001	±0.5	μA
Input Capacitance	C <sub>IN</sub>			8		pF

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

MAX5352/MAX5353

## ELECTRICAL CHARACTERISTICS: MAX5352 (continued)

( $V_{DD} = +5V \pm 10\%$ ,  $REF = 2.5V$ ,  $GND = 0V$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DYNAMIC PERFORMANCE</b>						
Voltage Output Slew Rate	SR			0.6		V/ $\mu$ s
Output Settling Time		To $\pm 1/2$ LSB, $V_{STEP} = 2.5V$		14		$\mu$ s
Output Voltage Swing		Rail-to-rail (Note 2)		0 to $V_{DD}$		V
Current into FB				0.001	$\pm 0.1$	$\mu$ A
Start-Up Time				20		$\mu$ s
Digital Feedthrough		$\overline{CS} = V_{DD}$ , $DIN = 100kHz$		5		nV-s
<b>POWER SUPPLIES</b>						
Supply Voltage	$V_{DD}$		4.5		5.5	V
Supply Current	$I_{DD}$	(Note 3)		0.28	0.4	mA
Supply Current in Shutdown		(Note 3)		4	20	$\mu$ A
Reference Current in Shutdown				0.001	$\pm 0.5$	$\mu$ A
<b>TIMING CHARACTERISTICS</b> (Figure 6)						
SCLK Clock Period	$t_{CP}$		100			ns
SCLK Pulse Width High	$t_{CH}$		40			ns
SCLK Pulse Width Low	$t_{CL}$		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	$t_{CSS}$		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	$t_{CSH}$		0			ns
DIN Setup Time	$t_{DS}$		40			ns
DIN Hold Time	$t_{DH}$		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	$t_{CS0}$		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	$t_{CS1}$		40			ns
$\overline{CS}$ Pulse Width High	$t_{CSW}$		100			ns

**Note 1:** Guaranteed from code 11 to code 4095 in unity-gain configuration.

**Note 2:** Accuracy is better than 1LSB for  $V_{OUT} = 8mV$  to  $V_{DD} - 100mV$ , guaranteed by a power-supply rejection test at the end points.

**Note 3:**  $R_L = \infty$ , digital inputs at GND or  $V_{DD}$ .

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

## ELECTRICAL CHARACTERISTICS: MAX5353

( $V_{DD} = +3.15V$  to  $+3.6V$ ,  $V_{REF} = 1.25V$ ,  $GND = 0V$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE—ANALOG SECTION</b>						
Resolution	N		12			Bits
Integral Nonlinearity (Note 4)	INL	MAX5353A			$\pm 1$	LSB
		MAX5353B			$\pm 2$	
		MAX5353BMJA			$\pm 4$	
Differential Nonlinearity	DNL	Guaranteed monotonic			$\pm 1.0$	LSB
Offset Error	$V_{OS}$			$\pm 0.3$	$\pm 8$	mV
Offset-Error Tempco	$TCV_{OS}$			6		ppm/ $^\circ C$
Gain Error (Note 4)	GE			-0.3	$\pm 3$	LSB
Gain-Error Tempco				1		ppm/ $^\circ C$
Power-Supply Rejection Ratio	PSRR				600	$\mu V/V$
<b>REFERENCE INPUT</b>						
Reference Input Range	$V_{REF}$		0		$V_{DD} - 1.4$	V
Reference Input Resistance	$R_{REF}$	Code dependent, minimum at code 1554 hex	14	20		k $\Omega$
<b>MULTIPLYING-MODE PERFORMANCE</b> ( $V_{DD} = +3.3V$ )						
Reference -3dB Bandwidth		$V_{REF} = 0.67V_{p-p}$		650		kHz
Reference Feedthrough		Input code = all 0s, $V_{REF} = 1.9V_{p-p}$ at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	$V_{REF} = 1V_{p-p}$ at 25kHz, code = full scale		72		dB
<b>DIGITAL INPUTS</b>						
Input High Voltage	$V_{IH}$		2.4			V
Input Low Voltage	$V_{IL}$				0.6	V
Input Leakage Current	$I_{IN}$	$V_{IN} = 0V$ or $V_{DD}$		0.001	$\pm 0.5$	$\mu A$
Input Capacitance	$C_{IN}$			8		pF
<b>DYNAMIC PERFORMANCE</b>						
Voltage Output Slew Rate	SR			0.6		V/ $\mu s$
Output Settling Time		To $\pm 1/2$ LSB, $V_{STEP} = 1.25V$		14		$\mu s$
Output Voltage Swing		Rail-to-rail (Note 5)		0 to $V_{DD}$		V
Current into FB				0.001	$\pm 0.1$	$\mu A$
Start-Up Time				20		$\mu s$
Digital Feedthrough		$\overline{CS} = V_{DD}$ , $DIN = 100kHz$		5		nV-s
<b>POWER SUPPLIES</b>						
Supply Voltage	$V_{DD}$		3.15		3.6	V
Supply Current	$I_{DD}$	(Note 6)		0.24	0.4	mA
Supply Current in Shutdown		(Note 6)		1.6	10	$\mu A$
Reference Current in Shutdown				0.001	$\pm 0.5$	$\mu A$

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

MAX5352/MAX5353

## ELECTRICAL CHARACTERISTICS: MAX5353 (continued)

( $V_{DD} = +3.15V$  to  $+3.6V$ ,  $REF = 1.25V$ ,  $GND = 0V$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>TIMING CHARACTERISTICS</b> (Figure 6)						
SCLK Clock Period	$t_{CP}$		100			ns
SCLK Pulse Width High	$t_{CH}$		40			ns
SCLK Pulse Width Low	$t_{CL}$		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	$t_{CSS}$		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	$t_{CSH}$		0			ns
DIN Setup Time	$t_{DS}$		40			ns
DIN Hold Time	$t_{DH}$		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	$t_{CS0}$		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	$t_{CS1}$		40			ns
$\overline{CS}$ Pulse Width High	$t_{CSW}$		100			ns

**Note 4:** Guaranteed from code 22 to code 4095 in unity-gain configuration.

**Note 5:** Accuracy is better than 1LSB for  $V_{OUT} = 8mV$  to  $V_{DD} - 150mV$ , guaranteed by a power-supply rejection test at the end points.

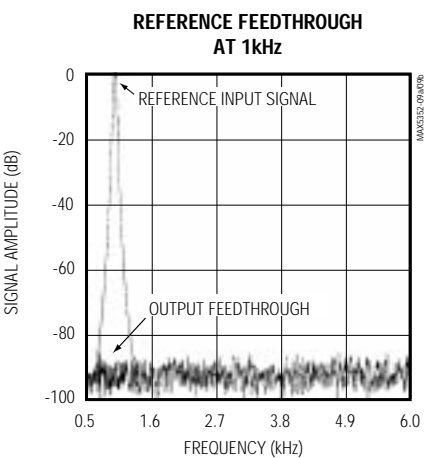
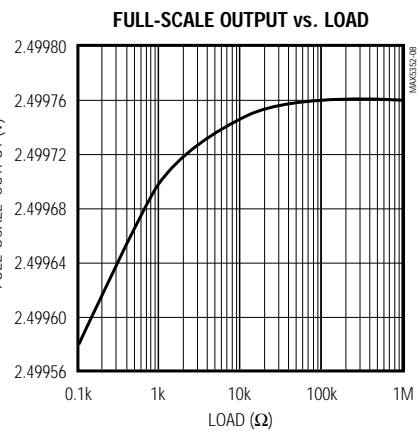
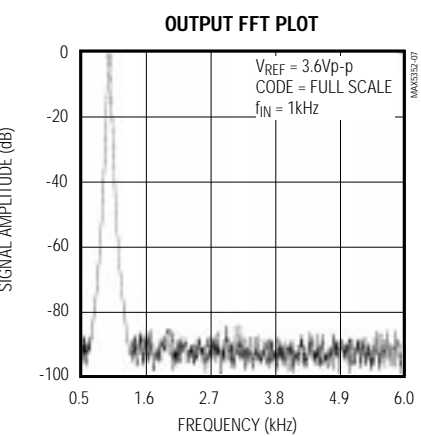
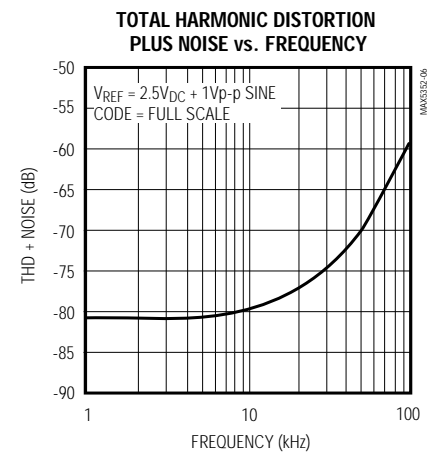
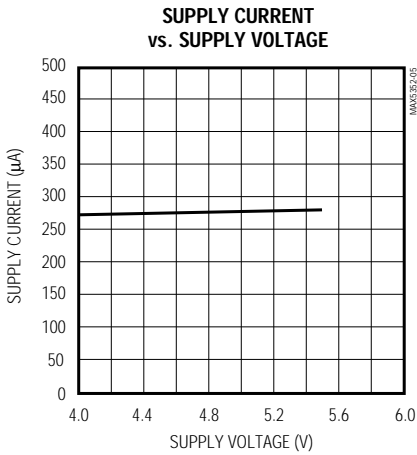
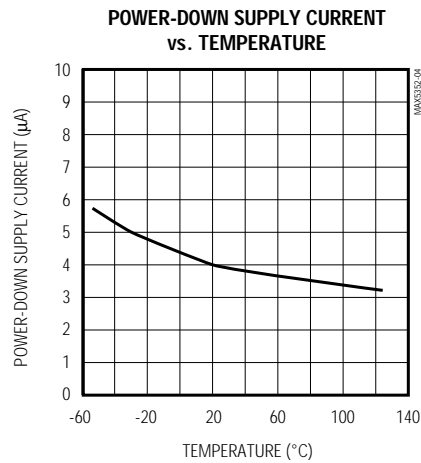
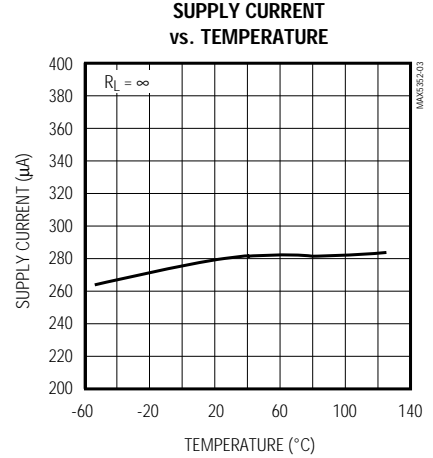
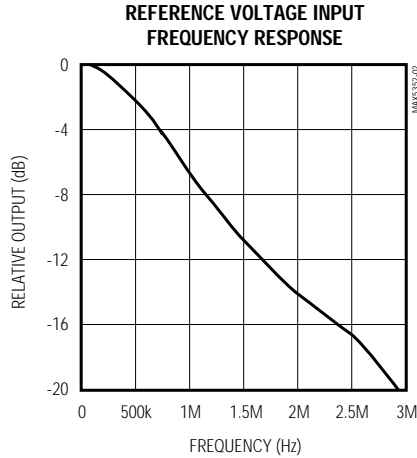
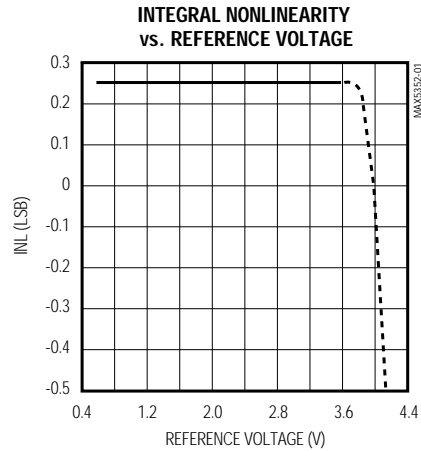
**Note 6:**  $R_L = \infty$ , digital inputs at GND or  $V_{DD}$ .

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

## Typical Operating Characteristics

(MAX5352 only,  $V_{DD} = +5V$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

### MAX5352



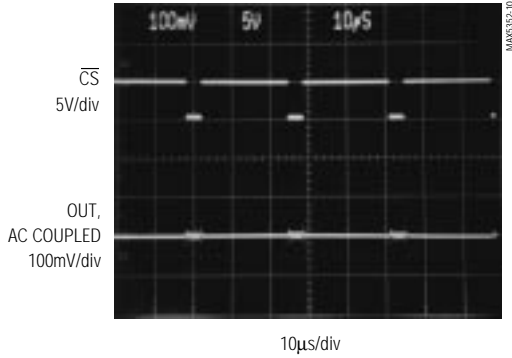
# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

MAX5352/MAX5353

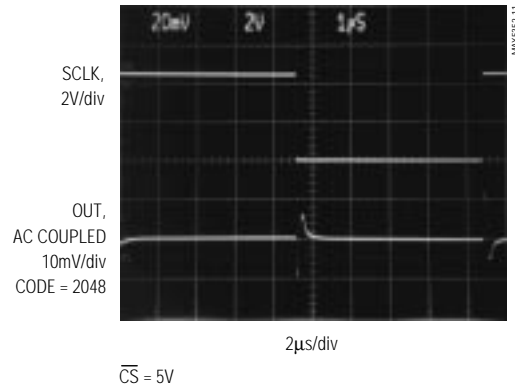
Typical Operating Characteristics (continued)  
(MAX5352 only,  $V_{DD} = +5V$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

## MAX5352 (continued)

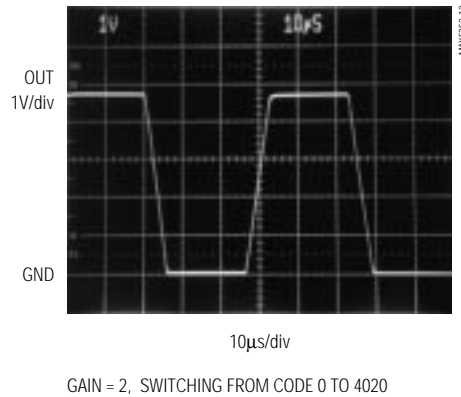
MAJOR-CARRY TRANSITION



DIGITAL FEEDTHROUGH ( $f_{SCLK} = 100kHz$ )



DYNAMIC RESPONSE

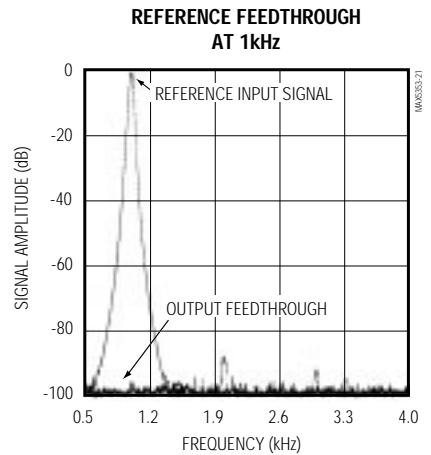
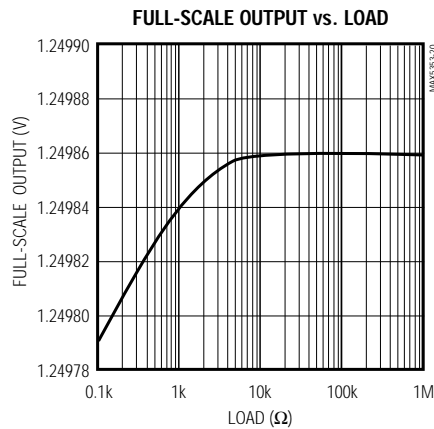
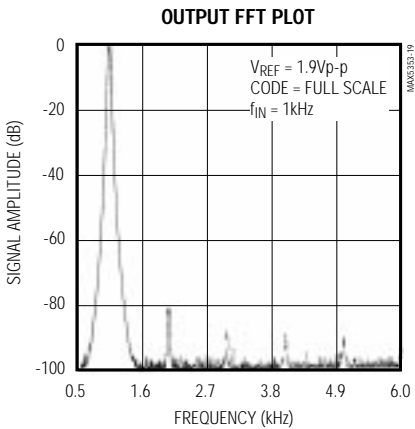
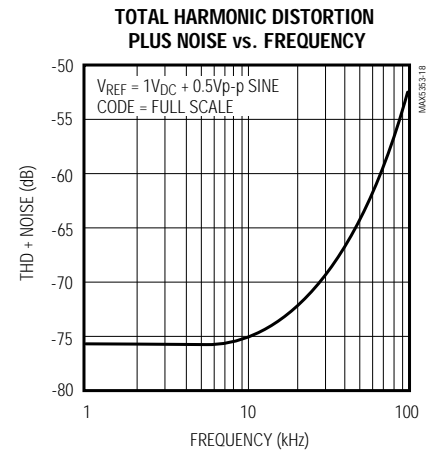
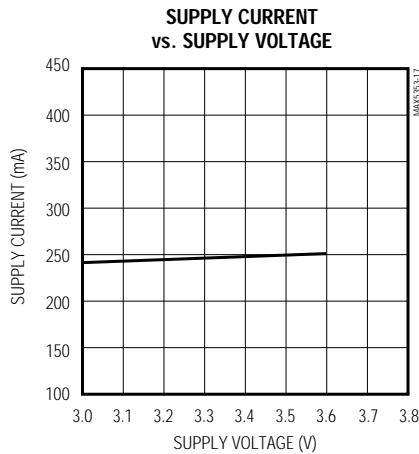
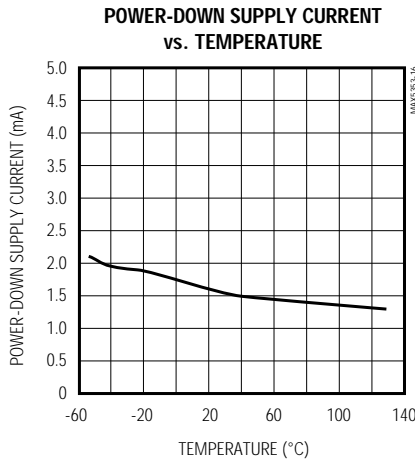
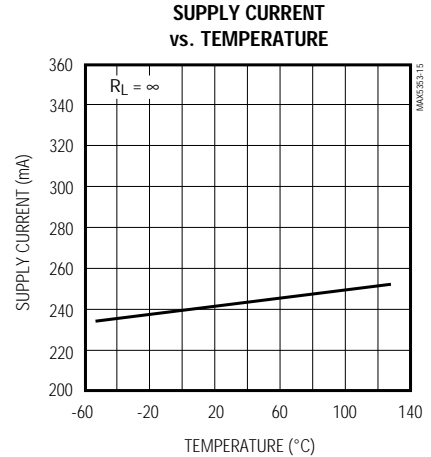
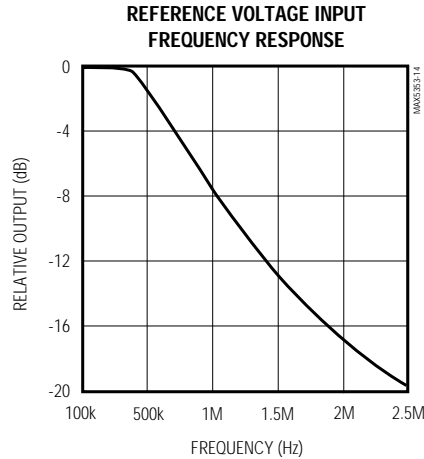
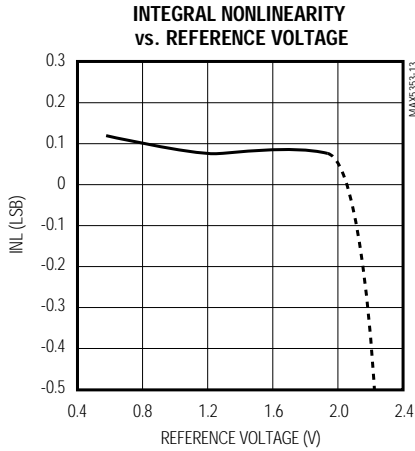


# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

## Typical Operating Characteristics (continued)

(MAX5353 only,  $V_{DD} = +3.3V$ ,  $R_L = 5k\Omega$ ,  $C_L = 100pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

### MAX5353



# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

## Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	$\overline{\text{CS}}$	Chip-Select Input. Active low.
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	FB	DAC Output Amplifier Feedback
6	REF	Reference Voltage Input
7	GND	Ground
8	V <sub>DD</sub>	Positive Power Supply

## Detailed Description

The MAX5352/MAX5353 contain a voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. Each IC includes a 16-bit shift register, and has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a digital input (12 data bits plus one sub-bit) into an equivalent analog output voltage in proportion to the applied reference voltage. Figure 1 shows a simplified circuit diagram of the DAC.

### Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V<sub>DD</sub> - 1.4V). The output voltage (V<sub>OUT</sub>) is represented by a digitally programmable voltage source, as expressed in the following equation:

$$V_{OUT} = (V_{REF} \times \text{NB} / 4096) \times \text{Gain}$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V<sub>REF</sub> is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 14kΩ when the DAC has an input code of 1554 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

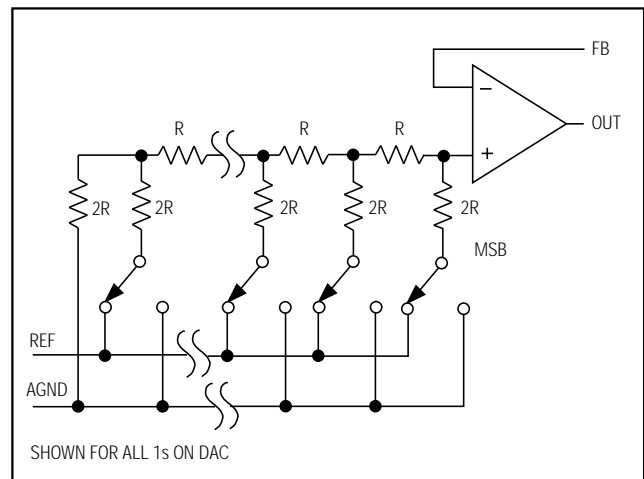


Figure 1. Simplified DAC Circuit Diagram

In shutdown mode, the MAX5352/MAX5353's REF input enters a high-impedance state with a typical input leakage current of 0.001μA.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (at full scale).

The MAX873 +2.5V reference is recommended for the MAX5352.

### Output Amplifier

The MAX5352/MAX5353's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/μs. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5352/MAX5353 output, the typical settling time to ±1/2LSB is 14μs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

### Shutdown Mode

The MAX5352/MAX5353 feature a software-programmable shutdown that reduces supply current to a typical value of 4μA. Writing 111X XXXX XXXX XXXX as the input-control word puts the device in shutdown mode (Table 1).

In shutdown mode, the amplifier's output and the reference input enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX5352/MAX5353



# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

to recall the output state prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or by updating the DAC with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the output to stabilize.

### Serial-Interface Configurations

The MAX5352/MAX5353's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of three control bits followed by 12+1 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX5352/MAX5353's response outlined in Table 1.

The MAX5352/MAX5353's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

The +3.3V MAX5353 can also directly interface with +5V logic.

### Serial-Interface Description

The MAX5352/MAX5353 require 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12+1 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ( $\overline{CS}$  must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 12+1 data bits D11...D0, S0 (Figure 4). Set the sub-bit (S0) to zero. The 3-bit control code determines:

- the register to be updated,
- the configuration when exiting shutdown.

Figure 5 shows the serial-interface timing requirements. The chip-select pin ( $\overline{CS}$ ) must be low to enable the DAC's serial interface. When  $\overline{CS}$  is high, the interface control circuitry is disabled.  $\overline{CS}$  must go low at least  $t_{CSS}$  before the rising serial clock (SCLK) edge to properly clock in the first bit. When  $\overline{CS}$  is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX5352/MAX5353 input/DAC register on  $\overline{CS}$ 's rising edge.

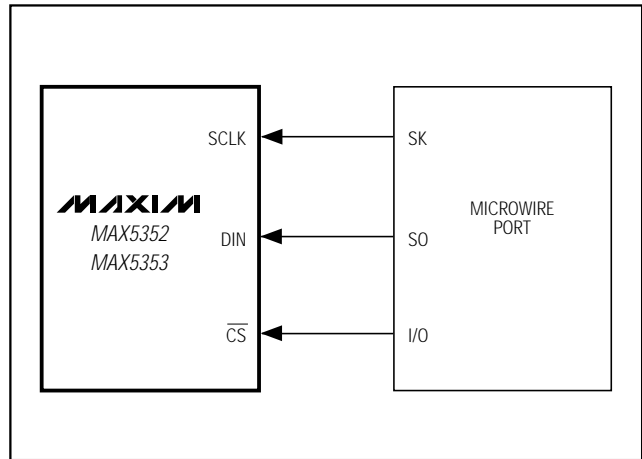


Figure 2. Connections for Microwire

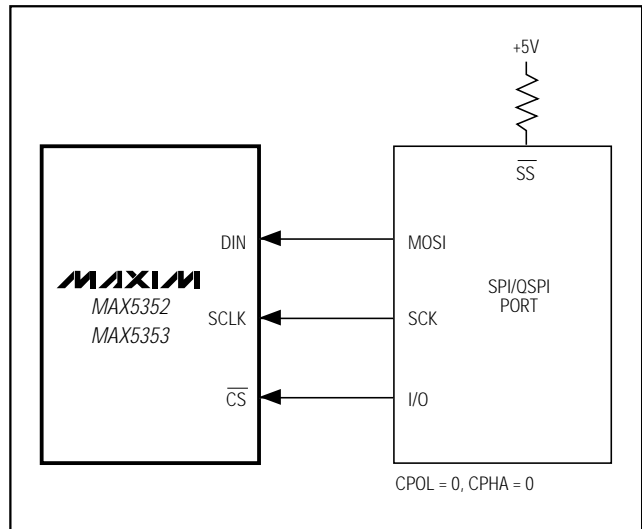


Figure 3. Connections for SPI/QSPI

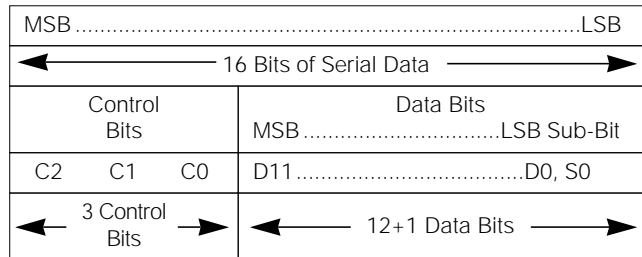


Figure 4. Serial-Data Format

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

MAX5352/MAX5353

**Table 1. Serial-Interface Programming Commands**

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D11.....D0 MSB      LSB	S0	
X	0	0	12 bits of data	0	Load input register; DAC register immediately updated (also exit shutdown).
X	0	1	12 bits of data	0	Load input register; DAC register unchanged.
X	1	0	XXXXXXXXXXXX	X	Update DAC register from input register (also exit shutdown; recall previous state).
1	1	1	XXXXXXXXXXXX	X	Shutdown
0	1	1	XXXXXXXXXXXX	X	No operation (NOP)

\*X\* = Don't care

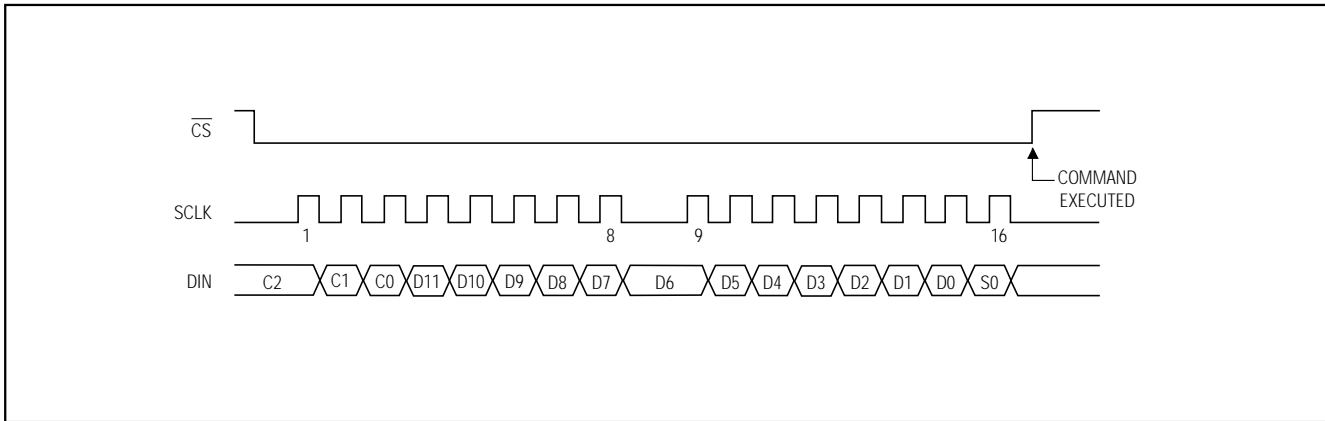


Figure 5. Serial-Interface Timing Diagram

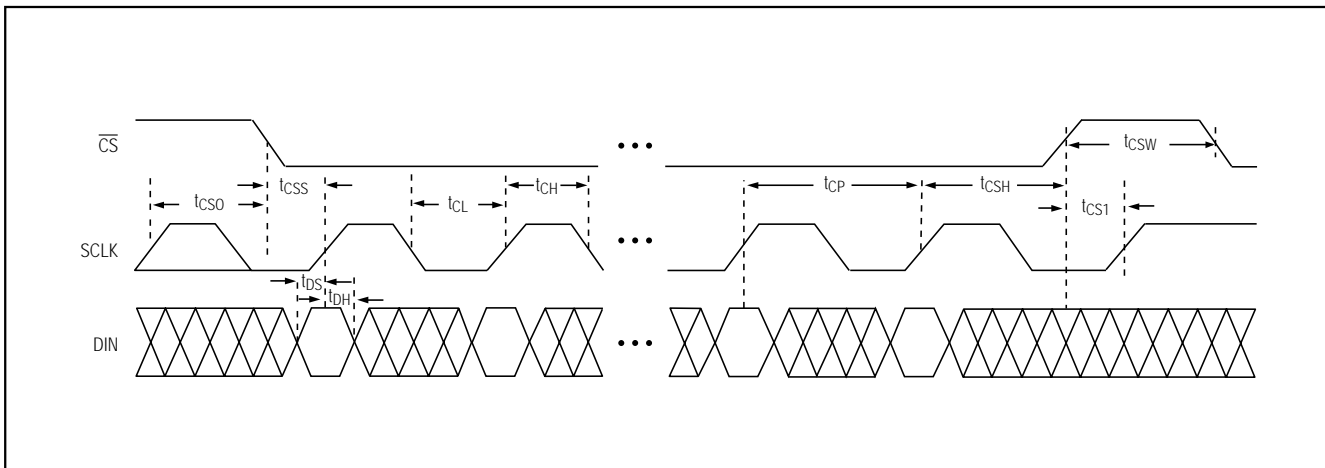


Figure 6. Detailed Serial-Interface Timing Diagram

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

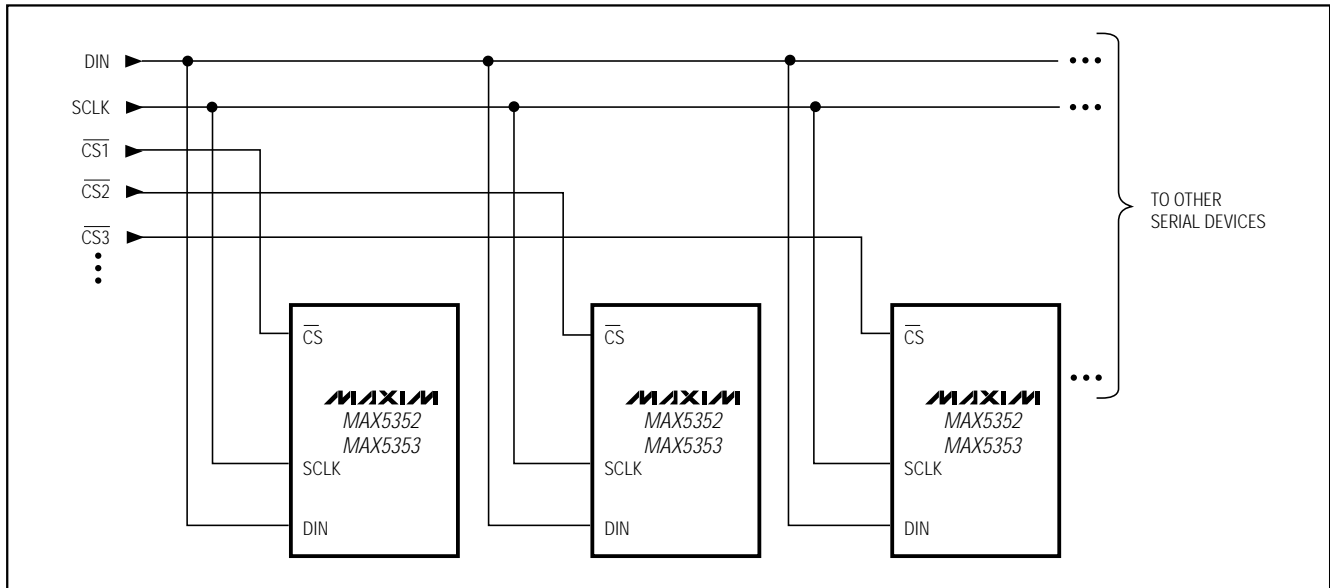


Figure 7. Multiple MAX5352/MAX5353s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX5352/MAX5353s. In this configuration, the clock and the data bus are common to all devices, and separate chip-select lines are used for each IC.

## Applications Information

### Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX5352/MAX5353 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

Figure 9 illustrates a rail-to-rail output. This circuit shows the MAX5352 with the output amplifier configured with a closed-loop gain of +2 to provide a 0V to 5V full-scale range when a 2.5V reference is used. When the MAX5353 is used with a 1.25V reference, this circuit provides a 0V to 2.5V full-scale range.

### Bipolar Output

The MAX5352/MAX5353 output can be configured for bipolar operation using Figure 10's circuit according to the following equation:

$$V_{OUT} = V_{REF} [(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and the corresponding output voltage for Figure 10's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1111	1111 1111 (0)	$+V_{REF} \left( \frac{4095}{4096} \right)$
1000	0000 0001 (0)	$+V_{REF} \left( \frac{2049}{4096} \right)$
1000	0000 0000 (0)	$+V_{REF} \left( \frac{2048}{4096} \right) = \frac{+V_{REF}}{2}$
0111	1111 1111 (0)	$+V_{REF} \left( \frac{2047}{4096} \right)$
0000	0000 0001 (0)	$+V_{REF} \left( \frac{1}{4096} \right)$
0000	0000 0000 (0)	0V

NOTE: ( ) are for sub-bit.

### Using an AC Reference

In applications where the reference has AC-signal components, the MAX5352/MAX5353 have multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

MAX5352/MAX5353

**Table 3. Bipolar Code Table**

DAC CONTENTS MSB	LSB	ANALOG OUTPUT
1111 1111 1111	(0)	$+V_{REF} \left( \frac{2047}{2048} \right)$
1000 0000 0001	(0)	$+V_{REF} \left( \frac{1}{2048} \right)$
1000 0000 0000	(0)	0V
0111 1111 1111	(0)	$-V_{REF} \left( \frac{1}{2048} \right)$
0000 0000 0001	(0)	$-V_{REF} \left( \frac{2047}{2048} \right)$
0000 0000 0000	(0)	$-V_{REF} \left( \frac{2048}{2048} \right) = -V_{REF}$

NOTE: ( ) are for sub-bit.

The MAX5352's total harmonic distortion plus noise (THD+N) is typically less than -77dB (full-scale code), and the MAX5353's THD+N is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz for both devices, as shown in the *Typical Operating Characteristics* graphs.

### Digitally Programmable Current Source

The circuit of Figure 12 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF}/R) \times (NB/4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

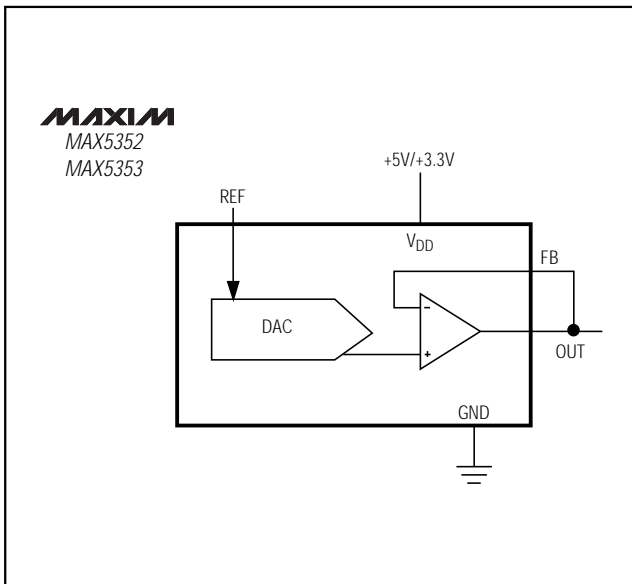


Figure 8. Unipolar Output Circuit

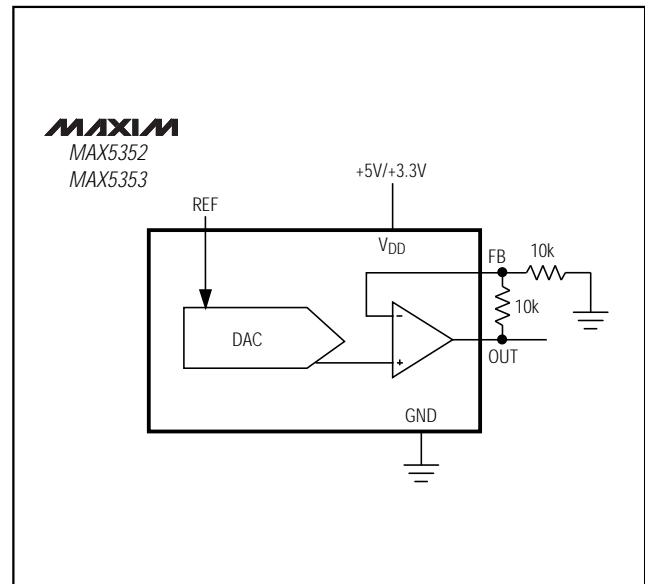


Figure 9. Unipolar Rail-to-Rail Output Circuit

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

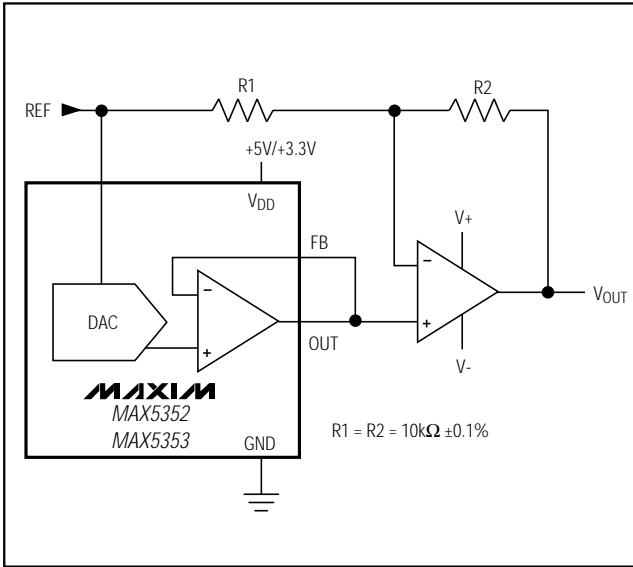


Figure 10. Bipolar Output Circuit

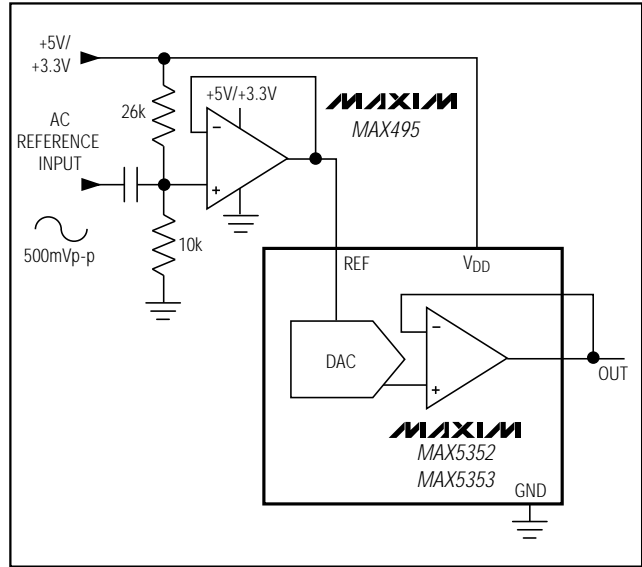


Figure 11. AC Reference Input Circuit

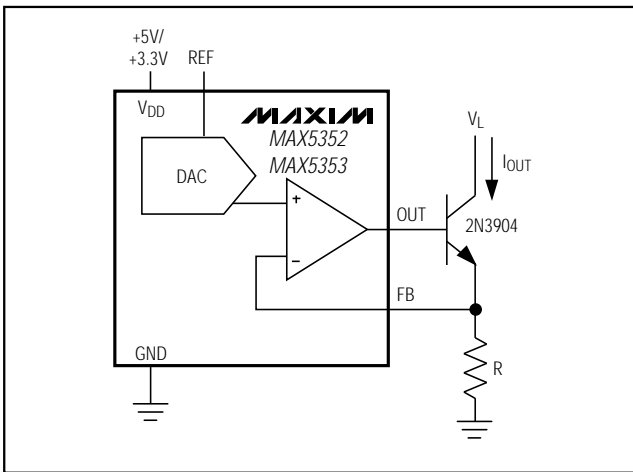


Figure 12. Digitally Programmable Current Source

## Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Tie GND to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

## Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code).

For rated MAX5352/MAX5353 performance, REF must be at least 1.4V below VDD. Bypass VDD with a 4.7μF capacitor in parallel with a 0.1μF capacitor to GND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

MAX5352/MAX5353

## Ordering Information (continued)

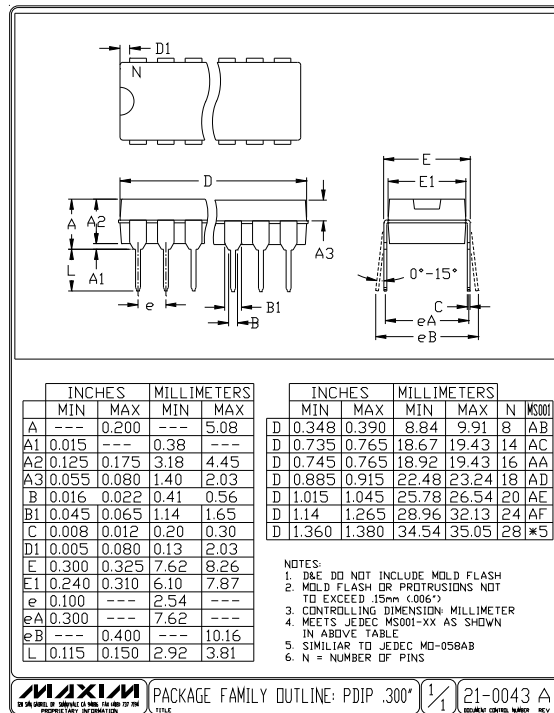
PART*	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5352AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX5352BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5352AEUA	-40°C to +85°C	8 μMAX	±1/2
MAX5352BEUA	-40°C to +85°C	8 μMAX	±1
MAX5352BMJA	-55°C to +125°C	8 CERDIP**	±2
<b>MAX5353</b> ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX5353BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX5353ACUA	0°C to +70°C	8 μMAX	±1
MAX5353BCUA	0°C to +70°C	8 μMAX	±2
MAX5353AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5353BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX5353AEUA	-40°C to +85°C	8 μMAX	±1
MAX5353BEUA	-40°C to +85°C	8 μMAX	±2
MAX5353BMJA	-55°C to +125°C	8 CERDIP**	±4

## Chip Information

TRANSISTOR COUNT: 1677

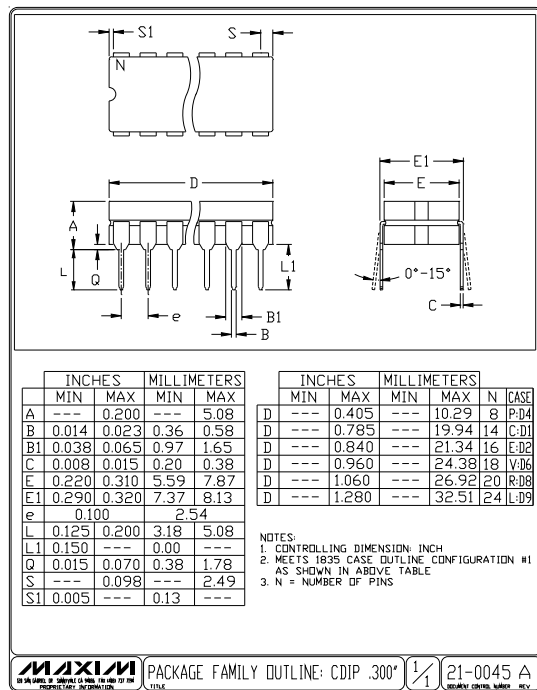
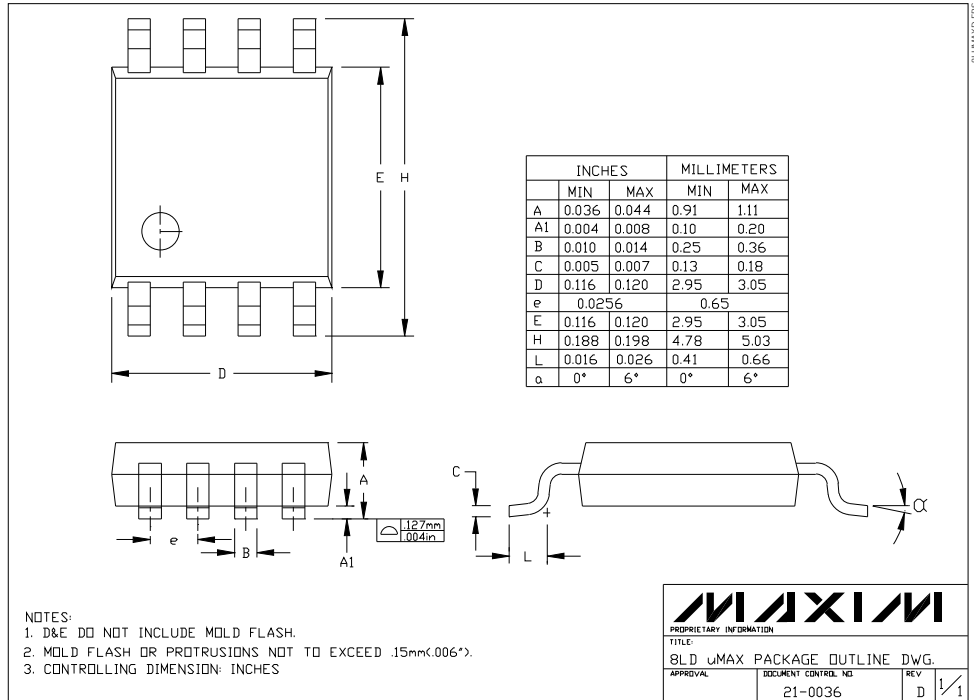
\*Contact factory for availability of 8-pin SO package.  
 \*\*Contact factory for availability and processing to MIL-STD-883.

## Package Information



# Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

## Package Information (continued)



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