

NCP2823 Series

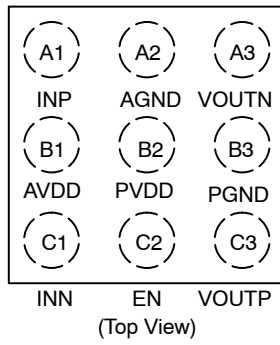


Figure 1. Pin Description

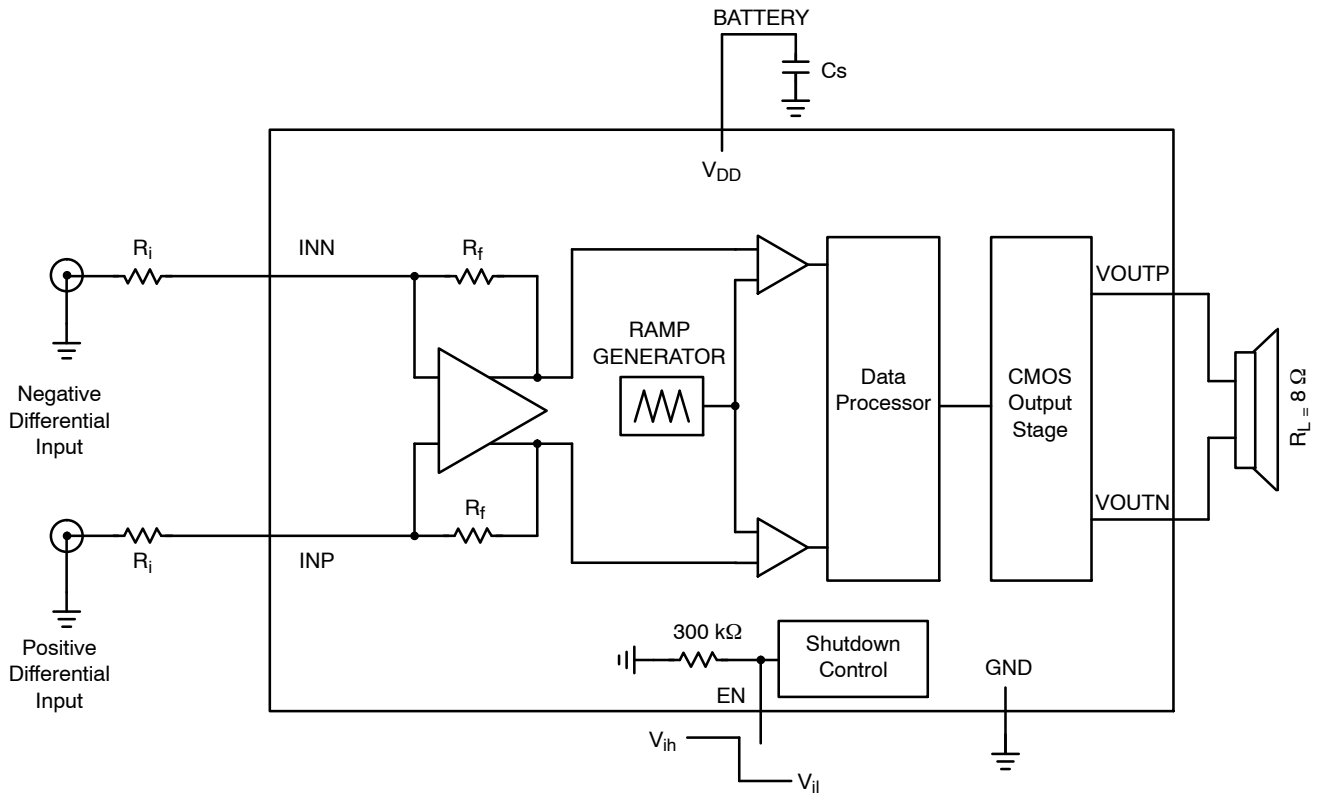


Figure 2. Simplified Block Diagram

NCP2823 Series

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	INP	INPUT	Positive Differential Input
C1	INN	INPUT	Negative Differential Input
B2	PVDD	POWER	Power Supply: This pin is the power supply of the device. A 4.7 μ F ceramic capacitor or larger must bypass this input to the ground. This capacitor should be placed as close as possible to this input.
B1	AVDD	POWER	Analog Power Supply: This pin must be connected to PVDD.
C3	VOU TP	OUTPUT	Positive output Special care must be observed at layout level. See the Layout recommendations.
A3	VOU TN	OUTPUT	Negative output: Special care must be observed at layout level. See the Layout recommendations.
C2	EN	INPUT	Enable: When a High logic is applied to this pin, the device is activated
B3	PGND	POWER	Power Ground: This pin is the power ground and carries the high switching current. A high quality ground must be provided to avoid any noise spikes/uncontrolled operation. Care must be observed to avoid high-density current flow in a limited PCB copper track.
A2	AGND	POWER	Analog Ground: This pin is the analog ground of the device and must be connected to GND plane.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
AVDD, PVDD Pins: Power Supply Voltage (Note 2)	V_P	-0.3 to +6.0	V
INP/N ,Pins: Input (Note 2)	$V_{INP/N}$	-0.3 to + V_{DD}	V
Digital Input/Output: EN Pin: Input Voltage Input Current	V_{DG} I_{DG}	-0.3 to $V_{DD} + 0.3$ 1	V mA
Human Body Model (HBM) ESD Rating are (Note 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 3)	ESD MM	200	V
WCSP 1.5 x 1.5 mm package (Notes 6 and 7) Thermal Resistance Junction-to-Case	$R_{\theta JC}$	90	$^{\circ}C/W$
Operating Ambient Temperature Range	T_A	-40 to +85	$^{\circ}C$
Operating Junction Temperature Range	T_J	-40 to +125	$^{\circ}C$
Maximum Junction Temperature (Note 6)	T_{JMAX}	+150	$^{\circ}C$
Storage Temperature Range	T_{STG}	-65 to +150	$^{\circ}C$
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Maximum electrical ratings are defined as those values beyond which damage to the device may occur at $T_A = 25^{\circ}C$.
- According to JEDEC standard JESD22-A108B.
- This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) +/-2.0 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) +/-200 V per JEDEC standard: JESD22-A115 for all pins.
- Latch up Current Maximum Rating: ± 100 mA per JEDEC standard: JESD78 class II.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.
- The thermal shutdown set to $150^{\circ}C$ (typical) avoids irreversible damage on the device due to power dissipation.
- The $R_{\theta CA}$ is dependent on the PCB heat dissipation. The maximum power dissipation (PD) is dependent on the min input voltage, the max output current and external components selected.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

NCP2823 Series

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ and for V_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$ and $V_{DD} = 3.6\text{ V}$. (see Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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GENERAL PERFORMANCES

V_P	Operational Power Supply		2.5		5.5	V
F_{OSC}	Oscillator Frequency		250	300	350	kHz
I_{DD}	Supply current	NCP2823A $V_P = 3.6\text{ V}$, No Load NCP2823B $V_P = 3.6\text{ V}$, No Load		1.8 2.6	2.4 4.6	mA
I_{sd}	Shutdown current	$V_{ENL} = V_{ENR} = 0\text{ V}$		0.01	1	μA
T_{ON}	Turn ON Time	EN rising edge		7.4		ms
T_{OFF}	Turn Off Time	EN falling edge		4		ms
Z_{sd}	Class D Output impedance in shutdown mode	$V_{ENL} = 0\text{ V}$		20		k Ω
$R_{DS(ON)}$	Static drain-source on-state resistance of power Mosfets			300		m Ω
η	Efficiency	NCP2823A, $V_P = 3.6\text{ V}$, $P_o = 600\text{ mW}$, $R_L = 8\ \Omega$, $F = 1\text{ kHz}$ NCP2823B, $V_P = 3.6\text{ V}$, $P_o = 1\text{ W}$, $R_L = 4\ \Omega$, $F = 1\text{ kHz}$		92 90		%
A_v	Voltage gain		<u>285 kΩ</u> Ri	<u>300 kΩ</u> Ri	<u>315 kΩ</u> Ri	V/V
F_{LP}	-3 dB Cut off Frequency of the Built in Low Pass Filter			30		kHz
T_{SD}	Thermal Shut Down Protection			150		$^{\circ}\text{C}$
T_{SDH}	Thermal Shut Down Hysteresis			10		$^{\circ}\text{C}$
V_{IH}	Rising Voltage Input Logic High		1.2	-	V_{DD}	V
V_{IL}	Falling Voltage Input Logic Low			-	0.4	V
R_{PLD}	Pull Down Resistor			250		k Ω

AUDIO PERFORMANCES

v_{oo}	Output offset			0.3		mV
PSRR	Power supply rejection ratio	$F = 217\text{ Hz}$, Input ac grounded		-77		dB
		$F = 1\text{ kHz}$, Input ac grounded		-63		
SNR	Signal to noise ratio	$V_P = 5\text{ V}$, $P_{out} = 600\text{ mW}$ (A. Weighted)		97		dB
CMRR	Common mode rejection ratio	Input shorted together $V_{IC} = 1\text{ V}_{pp}$, $f = 217\text{ Hz}$		-80		dB
V_n	Output Voltage noise	Input ac grounded, $A_v = 0\text{ dB}$	No weighting	35		μV
			A. Weighted	26		

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at $T_J = T_A = 25^{\circ}\text{C}$.

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
AUDIO PERFORMANCES							
Po	Output Power	NCP2823A RL = 8 Ω F = 1 kHz	THD+N < 1%	V _P = 5 V		1.5	W
				V _P = 3.6 V		0.7	
				V _P = 2.5 V		0.22	
			THD+N < 10%	V _P = 5 V		1.8	
				V _P = 3.6 V		0.87	
				V _P = 2.5 V		0.4	
		NCP2823B RL = 4 Ω F = 1 kHz	THD+N < 1%	V _P = 5 V		1.72	
				V _P = 3.6 V		1.2	
				V _P = 2.5 V		0.58	
			THD+N < 10%	V _P = 5 V		3	
				V _P = 3.6 V		1.57	
				V _P = 2.5 V		0.71	
THD+N	Total harmonic distortion plus noise	V _P = 3.6 V, Av = 6 dB, Po = 0.5 W			0.1	%	
		V _P = 5 V, Av = 6 dB, Po = 1 W			0.08		

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at $T_J = T_A = 25^{\circ}\text{C}$.

NCP2823 Series

TYPICAL OPERATING CHARACTERISTICS

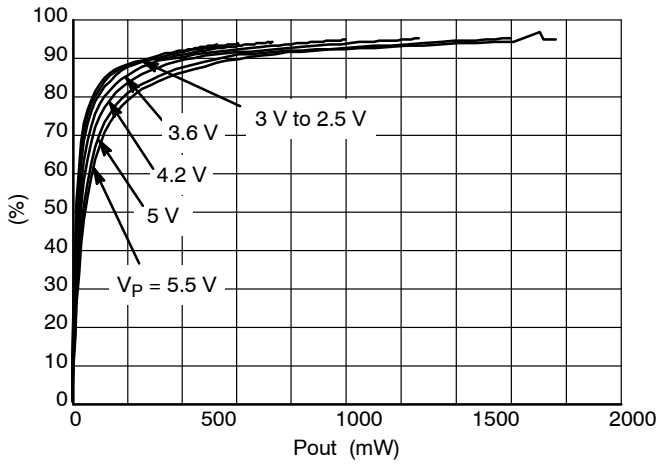


Figure 3. Efficiency vs P_{out}

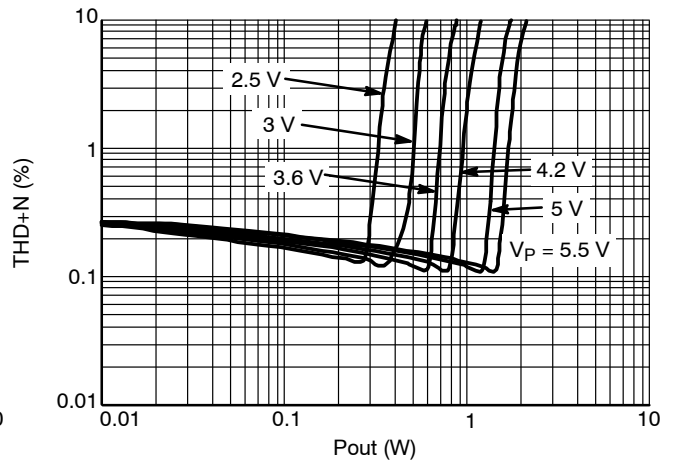


Figure 4. NCP2823A/B, THD+N vs P_{out} , $R_L = 8 \Omega$

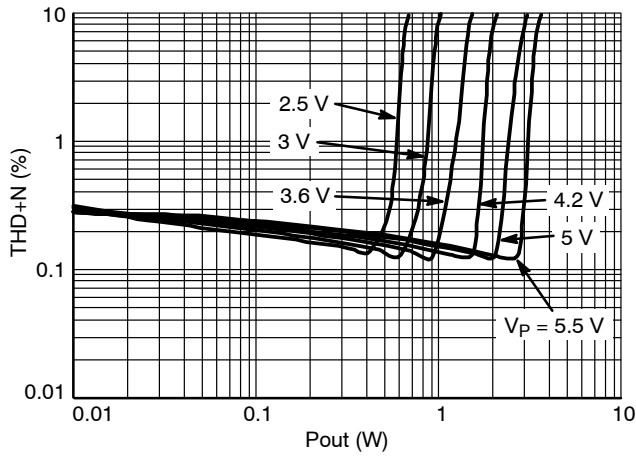


Figure 5. NCP2823B, THD+N vs P_{out} , $R_L = 4 \Omega$

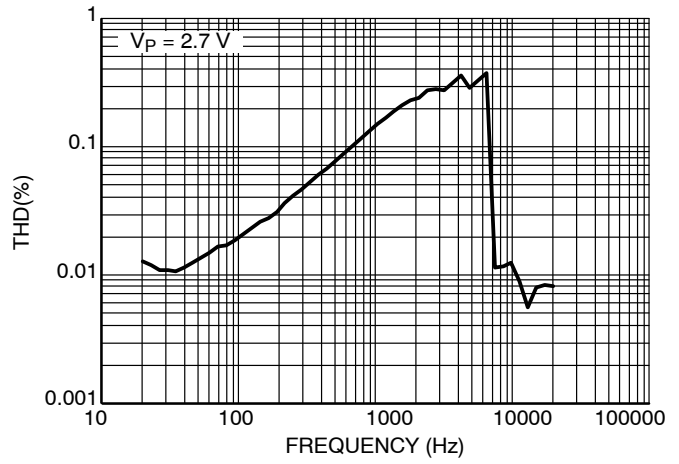


Figure 6. THD+N vs Frequency $P_{out} = 150 \text{ mW}$, $R_L = 8 \Omega$

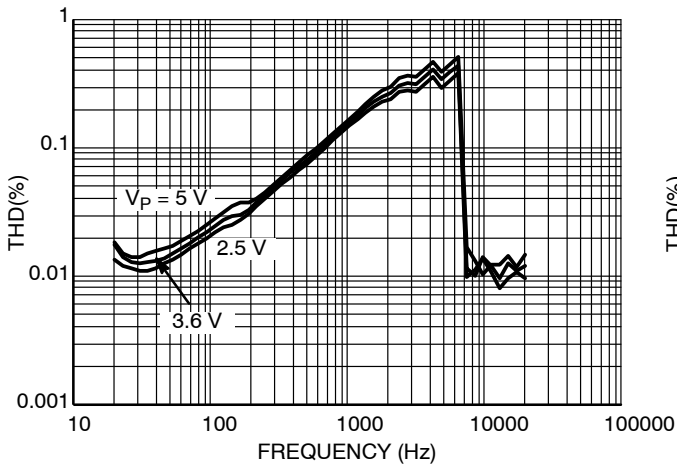


Figure 7. THD+N vs Frequency $P_{out} = 250 \text{ mW}$, $R_L = 8 \Omega$

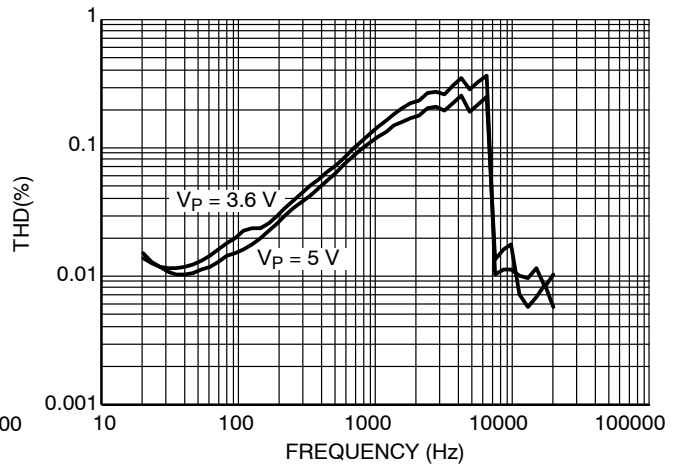


Figure 8. THD+N vs Frequency $P_{out} = 500 \text{ mW}$, $R_L = 8 \Omega$

NCP2823 Series

TYPICAL OPERATING CHARACTERISTICS

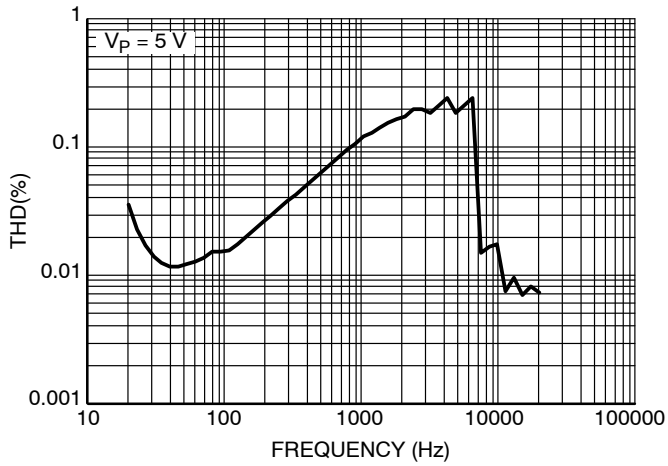


Figure 9. THD+N vs Frequency $P_{out} = 1\text{ W}$, $R_L = 8\ \Omega$

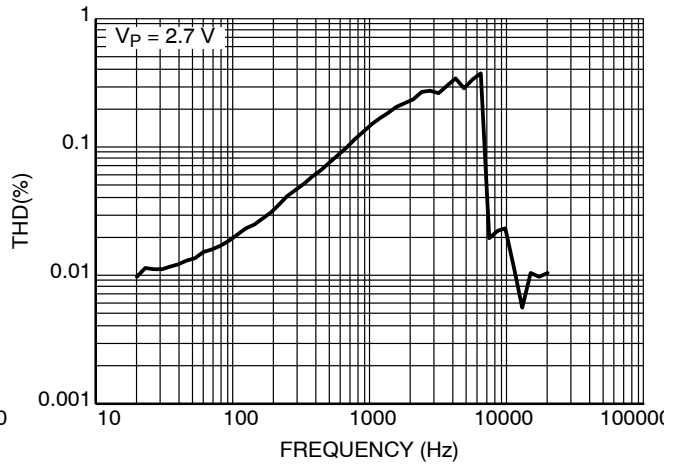


Figure 10. THD+N vs Frequency $P_{out} = 300\text{ mW}$, $R_L = 4\ \Omega$

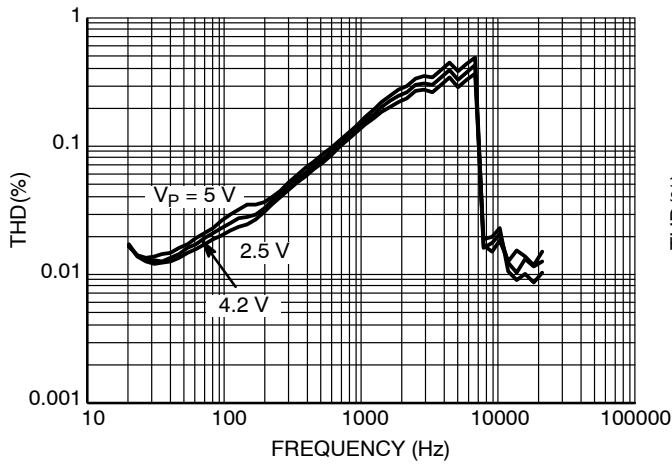


Figure 11. THD+N vs Frequency $P_{out} = 500\text{ mW}$, $R_L = 4\ \Omega$

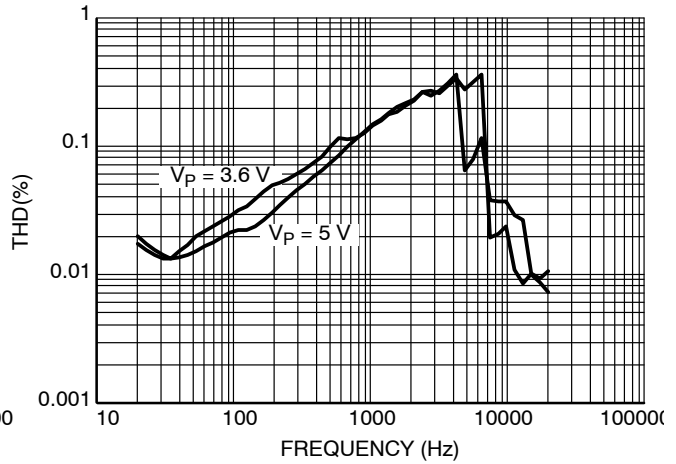


Figure 12. THD+N vs Frequency $P_{out} = 1\text{ W}$, $R_L = 4\ \Omega$

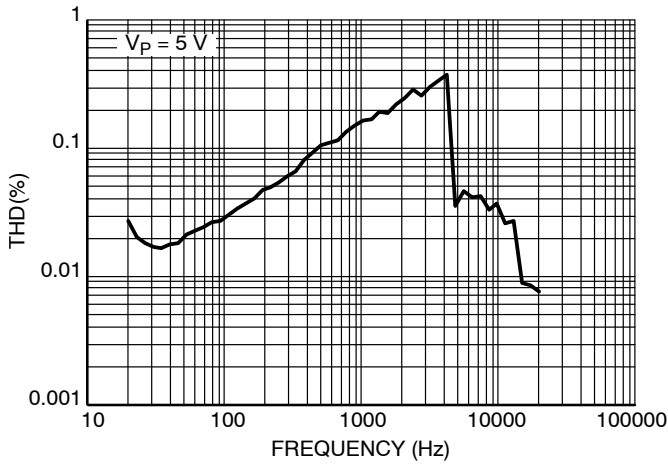


Figure 13. THD+N vs Frequency $P_{out} = 2\text{ W}$, $R_L = 4\ \Omega$

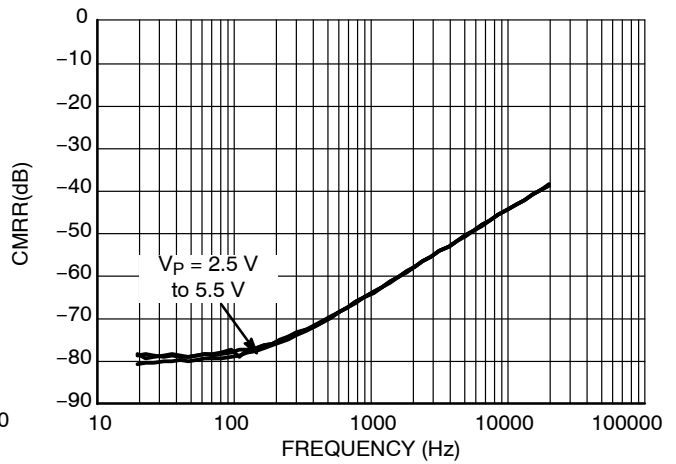


Figure 14. CMRR vs Frequency, $V_{ipp} = 1\text{ V}_{pp}$, $R_L = 8\ \Omega$

NCP2823 Series

TYPICAL OPERATING CHARACTERISTICS

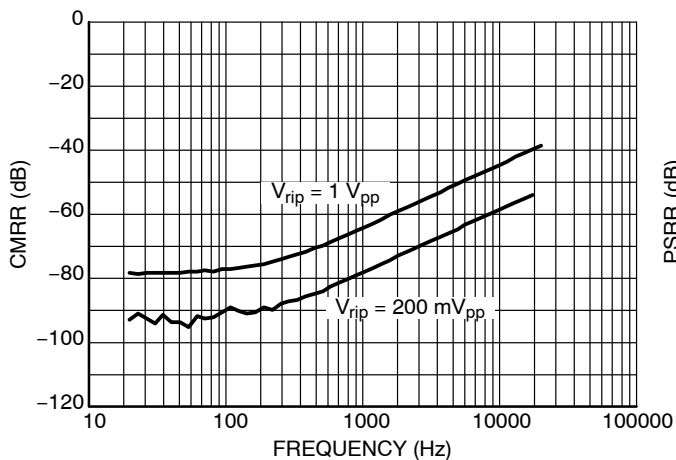


Figure 15. CMRR vs Frequency vs V_p

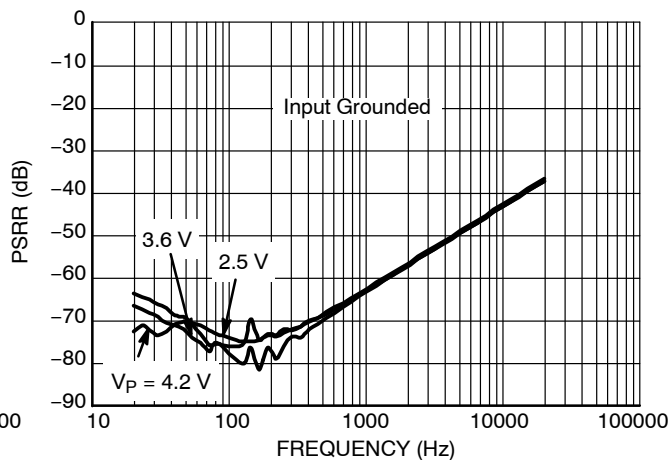


Figure 16. PSRR vs Frequency

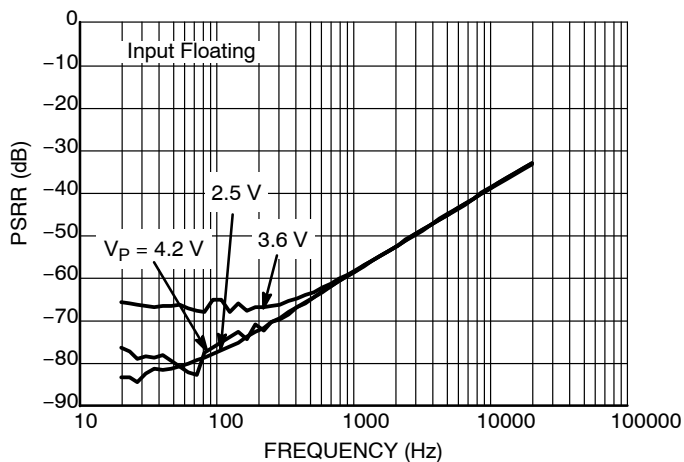


Figure 17. PSRR vs Frequency

NCP2823 Series

DETAIL OPERATING DESCRIPTION

General Description

The basic structure of the NCP2823A/B is composed of one analog pre-amplifier, a pulse width modulator and an H-bridge CMOS power stage. The first stage is externally configurable with gain-setting resistor R_i and the internal fixed feedback resistor R_f (the closed-loop gain is fixed by the ratios of these resistors). The load is driven differentially through two output stages. The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, which the typical cut off values are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver a maximum output power before clipping. The channel resistance (R_{on}) of the NMOS and PMOS transistors is typically 0.3Ω .

Gain Selection

The preamplifier stage amplifies the input signal. The gain is fully configurable by external resistors.

The gain setting is given by the following equation:

$$A_v = \frac{300 \text{ k}\Omega}{R_i} \quad (\text{eq. 1})$$

Turn On and Turn Off Transitions

In order to reduce “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When logic high is applied to the Enable pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly (5.0 ms). Thus, the total turn on time to get full power to the load is 7.4 ms (typical). The device has the same behavior when it is turned-off by a logic low on the Enable pin. No power is delivered to the load 4 ms after a falling edge on the shutdown pin. Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

Shutdown Function

The device enters shutdown mode when the Enable signal is low. During the shutdown mode, the DC Shutdown current of the circuit does not exceed $1 \mu\text{A}$.

The NCP2823A/B has an internal resistor ($R_{PLD} = 250 \text{ k}\Omega$) connected between GND and Enable. The purpose

of this resistor is to eliminate any unwanted state changes when the Enable pin is floating.

30 kHz Built-in Low Pass Filter

This filter allows connecting directly a DAC or a CODEC to the NCP2823 input without increasing the output noise by mixing frequency with the DAC/CODEC output frequency. Consequently, optimized operation with DACs or CODECs is guaranteed without additional external components.

Power Supply Bypassing

The NCP2823 requires a correct decoupling of the power supply in order to guarantee the best operation in terms of audio performances. To achieve these performances, it is necessary to place a $4.7 \mu\text{F}$ low ESR ceramic capacitor as close as possible to the PVDD pin in order to reduce high frequency transient spikes due to parasitic inductance (see Layout considerations).

Input Capacitors C_{in}

Thanks to its fully differential architecture the NCP2823 does not require input capacitors. However, it is possible to use input capacitors when the differential source is not biased or in single ended configuration. In this case it is necessary to take into account the corner frequency which can influence the low frequency response of the NCP2823. The following equation will help choose the adequate input capacitor.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_i \cdot C_{in}} \quad (\text{eq. 2})$$

Over Current Protection

This protection allows detecting an over current in the H-Bridge. When the current is higher than 2A for the NCP2823B or 1A for the NCP2823A, the H-Bridge is positioned in high impedance. When the short circuit is removed or the current is lower, the NCP2823 goes back to normal operation. This protection avoids over current due to a bad assembly (Output shorted together, to V_{DD} or to ground).

Layout Recommendations

For Efficiency and EMI standpoints, it is strongly recommended to use Power and ground plane in order to reduce parasitic resistance and inductance.

For the same reason, it is recommended to keep the output traces short and well shielded in order to avoid them to act as antenna.

NCP2823 Series

The EMI Level is strongly dependent upon the application. However, ferrite beads placed close to the NCP2823 will reduce EMI radiation when it is needed.

Ferrite value is strongly dependent upon the application.

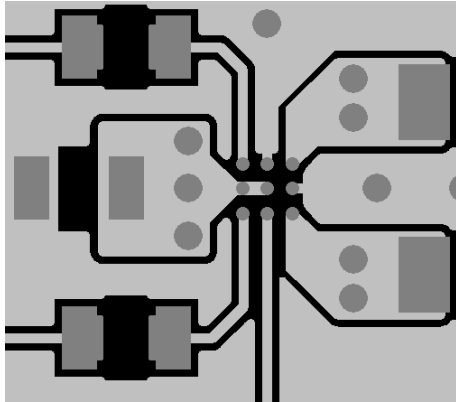


Figure 18. PCB Layout example

ORDERING INFORMATION

Device	Package	Shipping†
NCP2823AFCT2G	WLCSP9 (Pb-Free)	3000 / Tape & Reel
NCP2823AFCCT2G	WLCSP9 (Backside Laminate Coating) (Pb-Free)	3000 / Tape & Reel
NCP2823BFCT1G	WLCSP9 (Pb-Free)	3000 / Tape & Reel
NCP2823BFCT2G	WLCSP9 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Demo Board Available:

NCP2823AGEVB/D and NCP2823BGEVB/D evaluation board configure the device in typical application.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

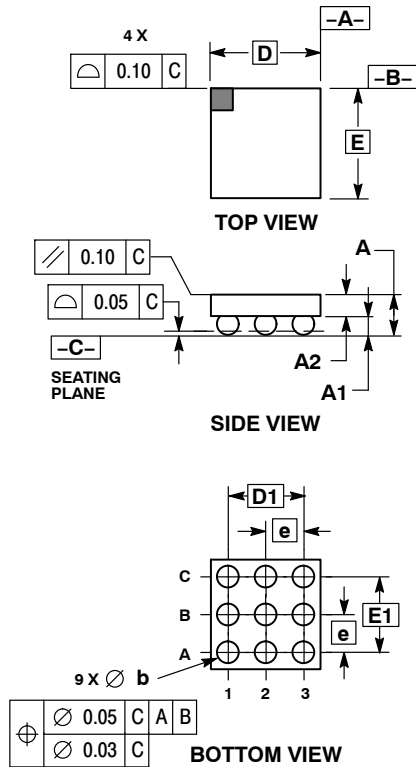


9 PIN FLIP-CHIP CASE 499AL-01 ISSUE O

DATE 30 AUG 2004



SCALE 4:1

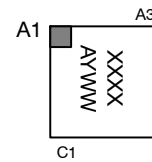


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

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DESCRIPTION:	9 PIN FLIP-CHIP, 1.45 X 1.45 MM	PAGE 1 OF 1

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