Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	−0.5	7.0	V
T_S	Storage Temperature[2]	−65	125	°C
T_J	Junction Temperature	−	125	°C
	Digital Inputs	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Digital Outputs referred to V_{DD}	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Electrostatic Discharge	−	2000	V
	Analog Input	−0.5	7.0	V

Pullable Crystal Specifications

Parameter	Description	Condition	Min	Typ.	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	−	27	−	MHz
C_{LNOM}	Nominal load capacitance		−	14	−	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	−	−	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec.	3	−	−	
DL	Crystal drive level	No external series resistor assumed	−	0.5	2.0	mW
F_{3SEPHI}	Third overtone separation from $3*F_{NOM}$	High side	300	−	−	ppm
F_{3SEPLO}	Third overtone separation from $3*F_{NOM}$	Low side	−	−	−150	ppm
C_0	Crystal shunt capacitance		−	−	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	−	250	
C_1	Crystal motional capacitance		14.4	18	21.6	pF

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	−	70	°C
C_{LOAD}	Max. Load Capacitance	−	−	15	pF
t_{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	−	500	ms

DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} - 0.5$, $V_{DD} = 3.3V$	12	24	−	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24	−	mA
C_{IN}	Input Capacitance		−	−	7	pF
I_{IZ}	Input Leakage Current		−	5	−	μA
$f_{\Delta XO}$	VCXO pullability range		±150	−	−	ppm
V_{VCXO}	VCXO input range		0	−	V_{DD}	V
I_{VDD}	Supply Current		−	25	30	mA

Note
2. Rated for 10 years

[+] Feedback

AC Electrical Characteristics (V_{DD} = 3.3V)

Parameter[3]	Description	Conditions	Min	Typ.	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3 50% of V_{DD}	45	50	55	%
ER_0	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF Figure 4.	0.8	1.4	–	V/ns
EF_1	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF Figure 4.	0.8	1.4	–	V/ns
t_9	Clock Jitter	Peak-Peak period jitter maximum absolute jitter	–	200	250	ps
t_{10}	PLL Lock Time		–	–	3	ms

Figure 2. Test Circuit
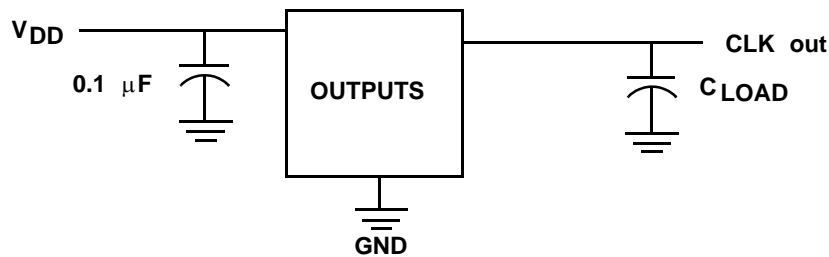
Figure 3. Duty Cycle Definition; DC = t2/t1
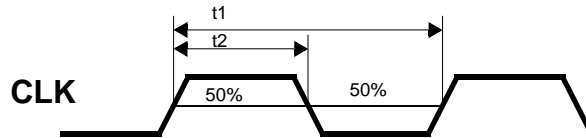
Figure 4. Rise and Fall Time Definitions: ER = 0.6 x V_{DD}/t3, EF = 0.6 x V_{DD}/t4
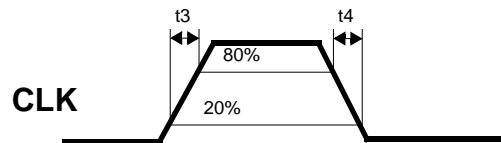
Note
3. Not 100% tested

[+] Feedback

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY24713KSXC	8-pin SOIC	Commercial	3.3V
CY24713KSXCT	8-pin SOIC-Tape and Reel	Commercial	3.3V

Package Diagram

Figure 5. 8-Pin (150-Mil) SOIC S8

PIN 1 ID

4   1

0.150[3.810]
0.157[3.987]

0.230[5.842]
0.244[6.197]

5   8
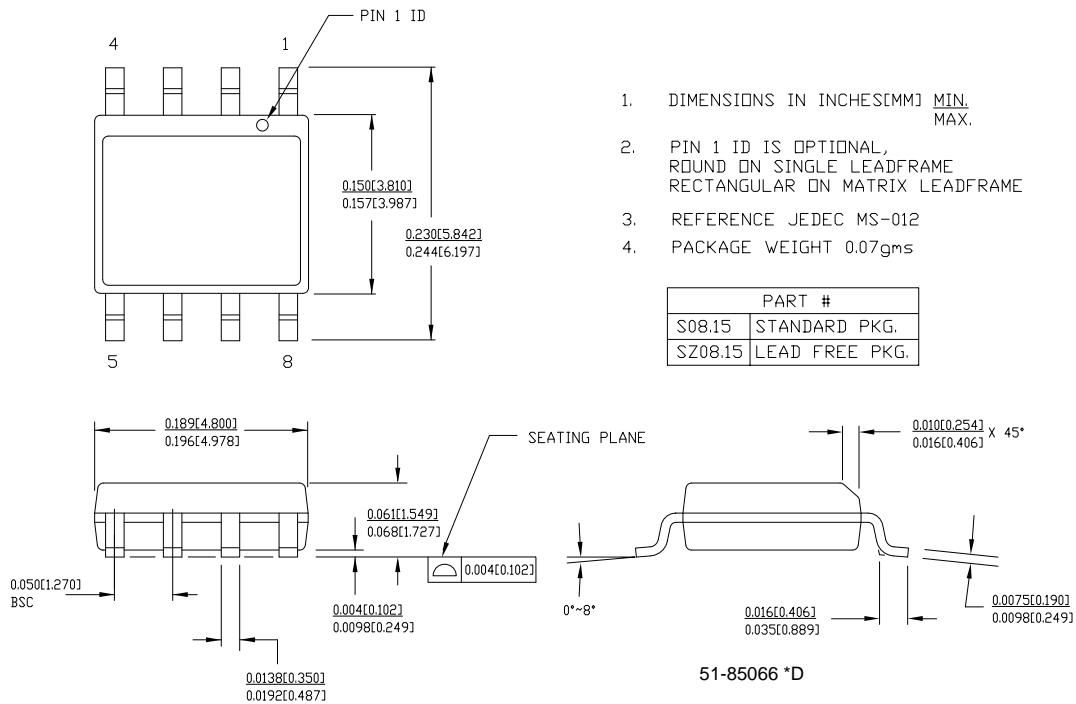
1.   DIMENSIONS IN INCHES[MM] MIN.
                                MAX.

2.   PIN 1 ID IS OPTIONAL,
      ROUND ON SINGLE LEADFRAME
      RECTANGULAR ON MATRIX LEADFRAME

3.   REFERENCE JEDEC MS-012

4.   PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG.
SZ08.15	LEAD FREE PKG.

0.189[4.800]
0.196[4.978]

SEATING PLANE

0.010[0.254] X 45°
0.016[0.406]

0.061[1.549]
0.068[1.727]

0.050[1.270]
BSC

0.004[0.102]

0.004[0.102]
0.0098[0.249]

0°~8°

0.016[0.406]
0.035[0.889]

0.0075[0.190]
0.0098[0.249]

0.0138[0.350]
0.0192[0.487]

51-85066 *D

Document History Page

				Document Title: CY24713 Set-top Box Clock Generator with VCXO Document Number: 38-07396

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	333175	RGL	See ECN	New Data Sheet
*A	2440886	AESA	See ECN	Updated template. Added Note "Not recommended for new designs." Added part number CY24713KSXC, and CY24713KSXCT in ordering information table. Replaced Lead-Free with Pb-Free.
*B	2899683	CXQ	03/26/10	Removed inactive parts from ordering information table Updated package diagram

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