

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	°C
T _J	Junction Temperature	-	125	°C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Digital Outputs referred to V _{DD}	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	-	2000	V
	Analog Input	-0.5	7.0	V

Pullable Crystal Specifications

Parameter	Description	Condition	Min	Typ.	Max	Unit
F _{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	-	27	-	MHz
C _{LNOM}	Nominal load capacitance		-	14	-	pF
R ₁	Equivalent series resistance (ESR)	Fundamental mode	-	-	25	Ω
R ₃ /R ₁	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R ₁ values are much less than the maximum spec.	3	-	-	
DL	Crystal drive level	No external series resistor assumed	-	0.5	2.0	mW
F _{3SEPHI}	Third overtone separation from 3*F _{NOM}	High side	300	-	-	ppm
F _{3SEPLO}	Third overtone separation from 3*F _{NOM}	Low side	-	-	-150	ppm
C ₀	Crystal shunt capacitance		-	-	7	pF
C ₀ /C ₁	Ratio of shunt to motional capacitance		180	-	250	
C ₁	Crystal motional capacitance		14.4	18	21.6	pF

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0	-	70	°C
C _{LOAD}	Max. Load Capacitance	-	-	15	pF
t _{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	-	500	ms

DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ.	Max	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} = 3.3V	12	24	-	mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V	12	24	-	mA
C _{IN}	Input Capacitance		-	-	7	pF
I _{Iz}	Input Leakage Current		-	5	-	μA
f _{ΔXO}	VCXO pullability range		±150	-	-	ppm
V _{VCXO}	VCXO input range		0	-	V _{DD}	V
I _{VDD}	Supply Current		-	25	30	mA

Note

2. Rated for 10 years

AC Electrical Characteristics ($V_{DD} = 3.3V$)

Parameter ^[3]	Description	Conditions	Min	Typ.	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3 50% of V_{DD}	45	50	55	%
ER_0	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD} , $C_{LOAD} = 15\text{ pF}$ Figure 4.	0.8	1.4	–	V/ns
EF_1	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD} , $C_{LOAD} = 15\text{ pF}$ Figure 4.	0.8	1.4	–	V/ns
t_9	Clock Jitter	Peak-Peak period jitter maximum absolute jitter	–	200	250	ps
t_{10}	PLL Lock Time		–	–	3	ms

Figure 2. Test Circuit

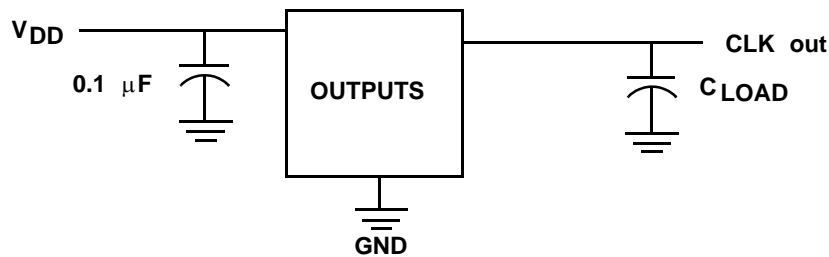


Figure 3. Duty Cycle Definition; $DC = t_2/t_1$

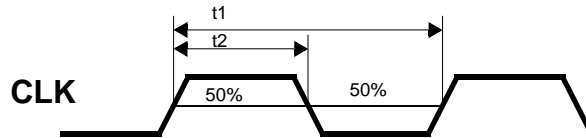
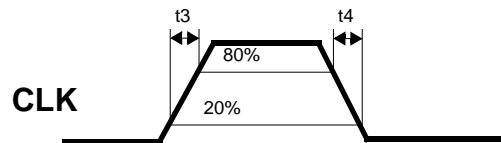


Figure 4. Rise and Fall Time Definitions: $ER = 0.6 \times V_{DD}/t_3$, $EF = 0.6 \times V_{DD}/t_4$



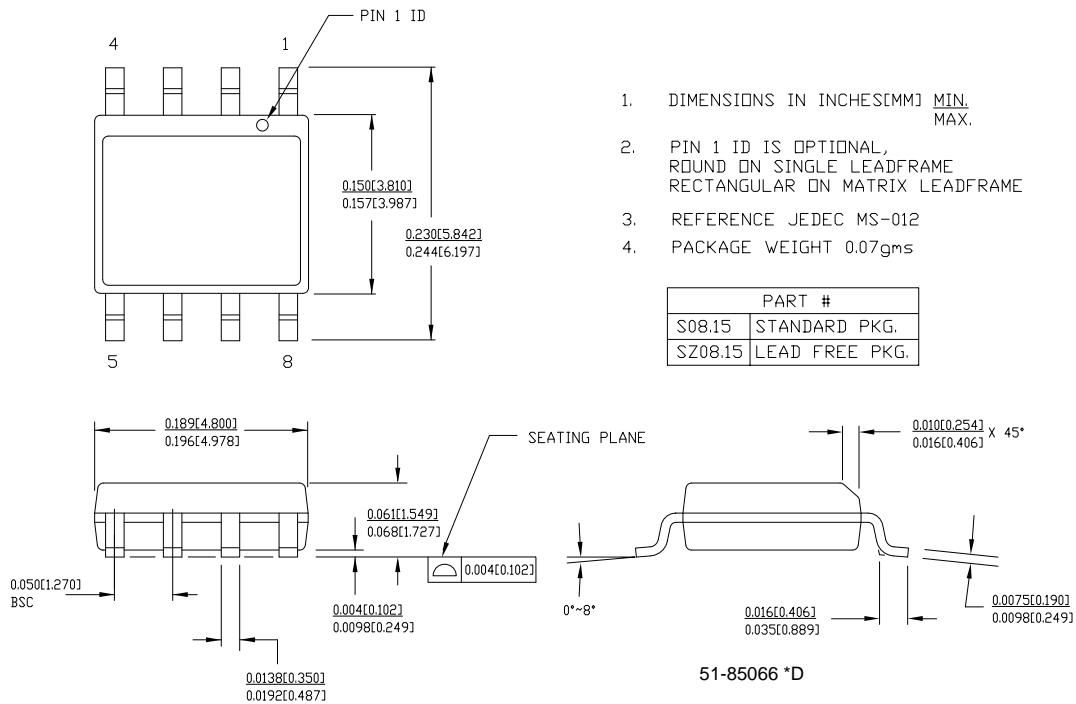
Note
3. Not 100% tested

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY24713KSXC	8-pin SOIC	Commercial	3.3V
CY24713KSXCT	8-pin SOIC-Tape and Reel	Commercial	3.3V

Package Diagram

Figure 5. 8-Pin (150-Mil) SOIC S8



1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG.
SZ08.15	LEAD FREE PKG.

Document History Page

Document Title: CY24713 Set-top Box Clock Generator with VCXO Document Number: 38-07396				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	333175	RGL	See ECN	New Data Sheet
*A	2440886	AESA	See ECN	Updated template. Added Note "Not recommended for new designs." Added part number CY24713KSXC, and CY24713KSXCT in ordering information table. Replaced Lead-Free with Pb-Free.
*B	2899683	CXQ	03/26/10	Removed inactive parts from ordering information table Updated package diagram

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