High-Performance, Step-Up, DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

LX to GND .....-0.3V to +24V
IN to GND .....-0.3V to +24V
$\overline{SHDN}$, V_L to GND.....-0.3V to +7.5V
COMP, SS, FB to GND.....-0.3V to (V_L + 0.3V)
LX Switch Maximum Continuous RMS Current.....3.2A

Continuous Power Dissipation (T_A = +70°C)
10-Pin 3mm x 3mm Thin TDFN
(derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_L = 3V, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Supply Range	V_{OUT} < 18V	2.6		5.5	V
	18V < V_{OUT} < 20V	4.0		5.5	V
OVP Threshold	V_{IN} rising	6.2	6.6	7	V
OVP Switch Resistance		8	12	20	Ω
Output Voltage Range				20	V
VL Undervoltage-Lockout Threshold	V_L rising; typical hysteresis is 50mV; LX remains off below this level	2.30	2.45	2.57	V
IN Quiescent Current	V_{FB} = 1.3V, not switching		0.3	0.6	mA
	V_{FB} = 1.0V, switching		1.5	2.5	
IN Shutdown Supply Current	$\overline{SHDN}$ = GND		160	250	µA
Thermal Shutdown	Temperature rising		160		°C
	Hysteresis		20		
ERROR AMPLIFIER					
Feedback Voltage	Level to produce V_{COMP} = 1.24V	1.23	1.24	1.25	V
FB Input Bias Current	V_{FB} = 1.24V	50	125	225	nA
FB Line Regulation	Level to produce V_{COMP} = 1.24V, 2.6V < V_{IN} < 5.5V		0.05	0.15	%/V
Transconductance		110	300	450	µS
Voltage Gain			2400		V/V
Shutdown FB Input Voltage	$\overline{SHDN}$ = GND	0.05	0.10	0.15	V
OSCILLATOR					
Frequency (f_{OSC})		800	1000	1200	kHz
Maximum Duty Cycle		89	92	95	%
n-CHANNEL MOSFET					
Current Limit	V_{FB} = 1V, 75% duty cycle, V_L = 5V	3.9	4.6	5.3	A
On-Resistance	V_L = 5V (typ value at T_A = +25°C) (Note 1)		110	170	mΩ
	V_L = 3V (typ value at T_A = +25°C) (Note 1)		135	210	
Leakage Current	V_{LX} = 20V		12	25	µA
Current-Sense Transresistance	V_L = 5V	0.09	0.15	0.25	V/A

ELECTRICAL CHARACTERISTICS (continued)

(V_{VL} = 3V, **T_A = 0°C to +85°C,** unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START					
Reset Switch Resistance				25	Ω
Charge Current	V_{SS} = 1.2V	1.5	3.5	5.5	µA
CONTROL INPUTS					
$\overline{SHDN}$ Threshold	$\overline{SHDN}$ rising	1.1	1.16	1.22	V
$\overline{SHDN}$ Input Hysteresis			60		mV
$\overline{SHDN}$ Discharge Resistance	V_L < UVLO		20		Ω
$\overline{SHDN}$ Charge Current		4.25	5	5.75	µA
Charge Current Delay Time			80		µs

ELECTRICAL CHARACTERISTICS

(V_L = 3V, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
IN Supply Range	V_{OUT} < 18V	2.6	5.5	V
	18V < V_{OUT} < 20V	4.0	5.5	V
Output Voltage Range			20	V
Output Switch Resistance		8	20	Ω
VL Undervoltage-Lockout Threshold	V_L rising; typical hysteresis is 50mV; LX remains off below this level	2.30	2.57	V
IN Quiescent Current	V_{FB} = 1.3V, not switching		0.6	mA
	V_{FB} = 1.0V, switching		2.5	
IN Shutdown Supply Current	$\overline{SHDN}$ = GND		250	µA
ERROR AMPLIFIER				
Feedback Voltage	Level to produce V_{COMP} = 1.24V	1.227	1.253	V
FB Input Bias Current	V_{FB} = 1.24V		225	nA
Transconductance		110	450	µS
Shutdown FB Input Voltage	$\overline{SHDN}$ = GND	0.05	0.15	V
OSCILLATOR				
Frequency (f_{OSC})		750	1250	kHz
Maximum Duty Cycle		89	96	%

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ELECTRICAL CHARACTERISTICS (continued)

(V_{VL} = 3V, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 1)

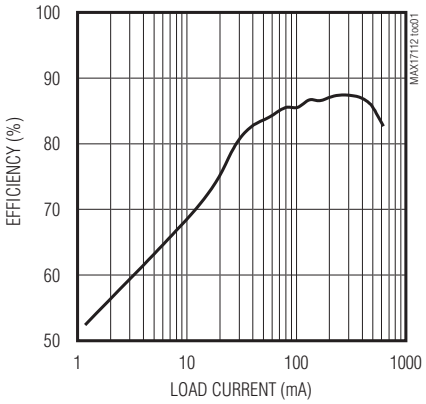
PARAMETER	CONDITIONS	MIN	MAX	UNITS
n-CHANNEL MOSFET				
Current Limit	V_{FB} = 1V, 75% duty cycle, V_L = 5V	3.9	5.3	A
On-Resistance	V_L = 5V		170	mΩ
	V_L = 3V		210	
Current-Sense Transresistance	V_L = 5V	0.09	0.25	V/A
SOFT-START				
Reset Switch Resistance			25	Ω
Charge Current	V_{SS} = 1.2V	1.5	5.5	µA
CONTROL INPUTS				
$\overline{SHDN}$ Threshold	$\overline{SHDN}$ rising	1.19	1.29	V
$\overline{SHDN}$ Charge Current		4.25	5.75	µA

Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

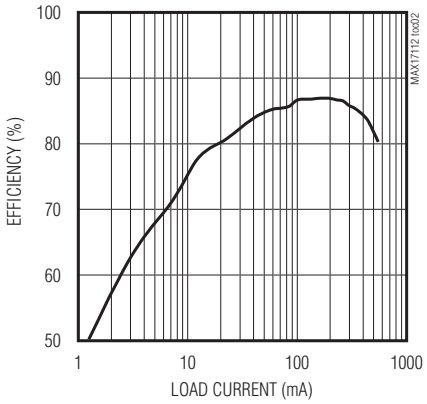
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 15V, T_A = +25°C, unless otherwise noted.)

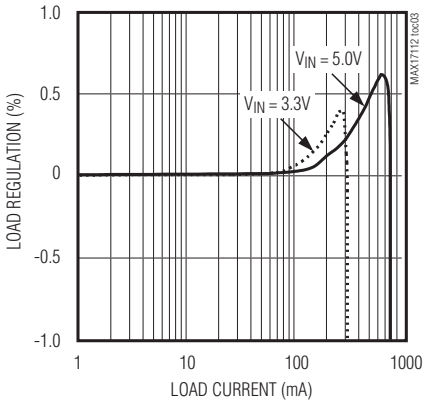
EFFICIENCY vs. LOAD CURRENT (V_{IN} = 5V, V_{OUT} = 15V)



EFFICIENCY vs. LOAD CURRENT (V_{IN} = 3.3V, V_{OUT} = 9V)



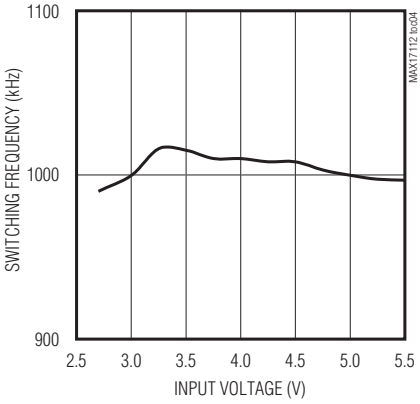
LOAD REGULATION (V_{OUT} = 15V)



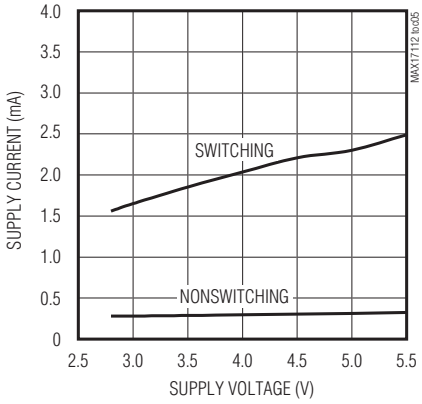
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 5V, V_{MAIN} = 15V, T_A = +25°C, unless otherwise noted.)

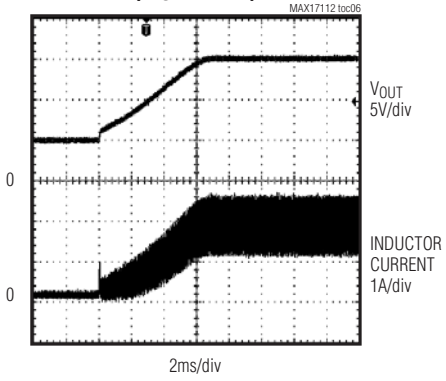
SWITCHING FREQUENCY vs. INPUT VOLTAGE



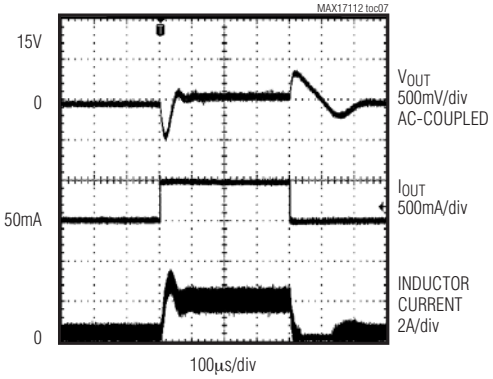
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SOFT-START (R_{LOAD} = 30Ω)

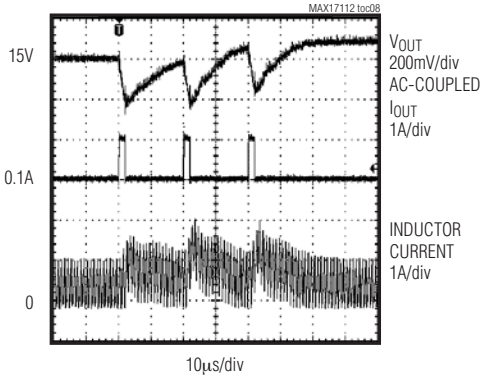


LOAD-TRANSIENT RESPONSE (I_{LOAD} = 50mA TO 550mA)



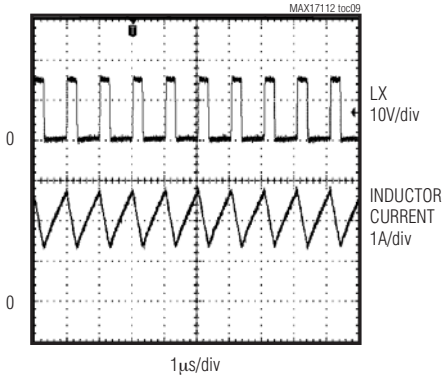
L = 2.7µH
R_{COMP} = 47kΩ
C_{COMP1} = 560pF

PULSED LOAD-TRANSIENT RESPONSE (I_{LOAD} = 100mA TO 1.1A)

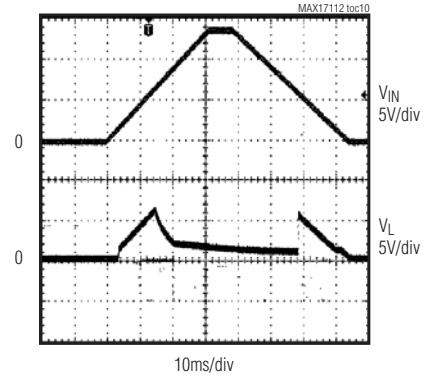


L = 2.7µH
R_{COMP} = 47kΩ
C_{COMP1} = 560pF

SWITCHING WAVEFORMS (I_{LOAD} = 600mA)



V_{IN} OVP PROTECTION



Pin Description

PIN	NAME	FUNCTION
1	COMP	Compensation Pin for Error Amplifier. Connect a series RC from COMP to ground. Typical values are 47kΩ and 580pF.
2	FB	Feedback. The FB regulation voltage is 1.24V nominal. Connect an external resistor-divider center tap here and minimize the trace area. Set V_{OUT} according to the *Output Voltage Selection* section.
3	V_L	IC Supply. There is an internal switch between IN and V_L and the switch disconnects when an overvoltage condition on IN is detected. Bypass V_L to GND with a 1µF capacitor.
4, 5	GND	Ground
6, 7	LX	Switch. LX is the drain of the internal MOSFET.
8	IN	Supply Voltage Input. Bypass IN with a minimum 1µF ceramic capacitor directly to GND.
9	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ high to turn on the MAX17112 for normal operation. Connect a capacitor to the $\overline{SHDN}$ pin to create a delayed turn-on. The time delay is 0.25 x C (typ), C in microfarads. $\overline{SHDN}$ can be driven from a logic signal directly, in which case a resistor is required in series with $\overline{SHDN}$.
10	SS	Soft-Start Control. Connect a soft-start capacitor (C_{SS}). Leave open for no soft-start. The soft-start capacitor is charged at a rate of 4µA/C_{SS}.
—	EP	Exposed Pad. Connect to GND.

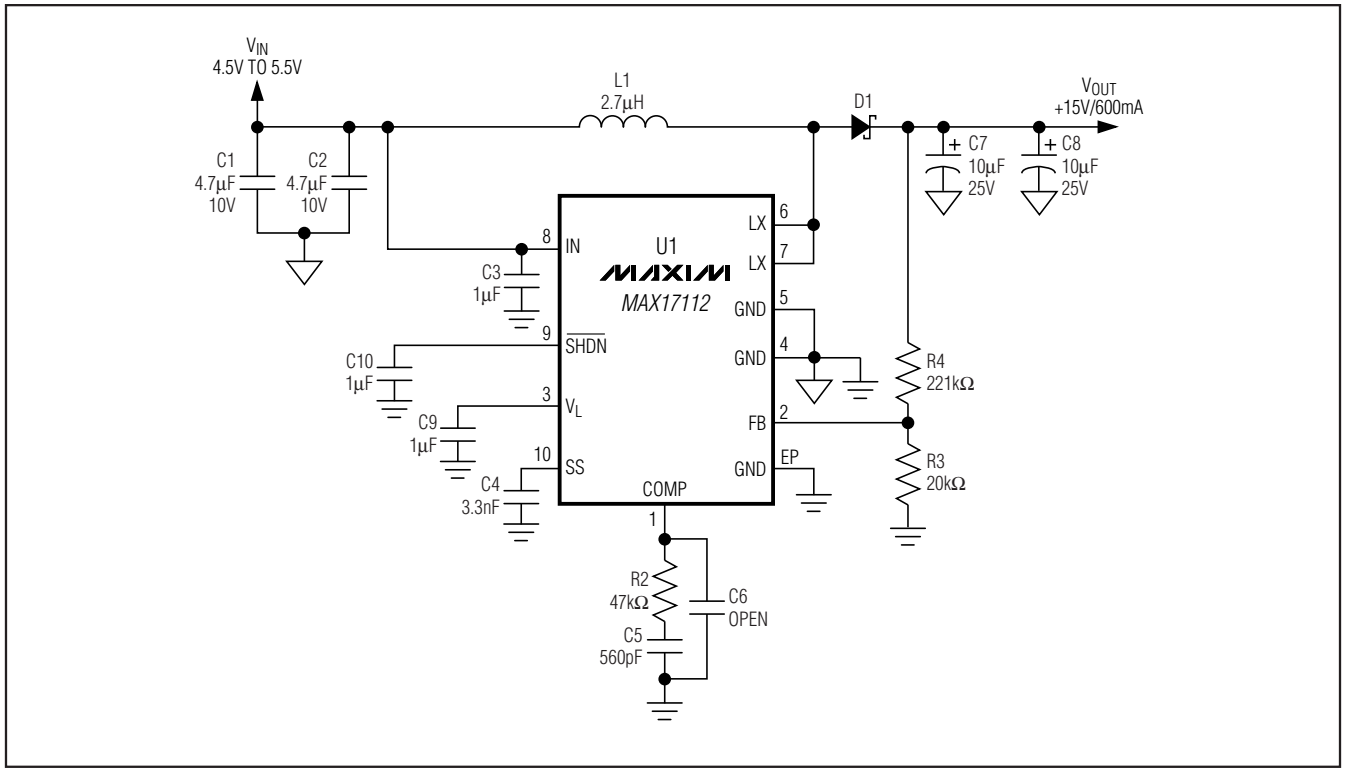


Figure 1. Typical Operating Circuit

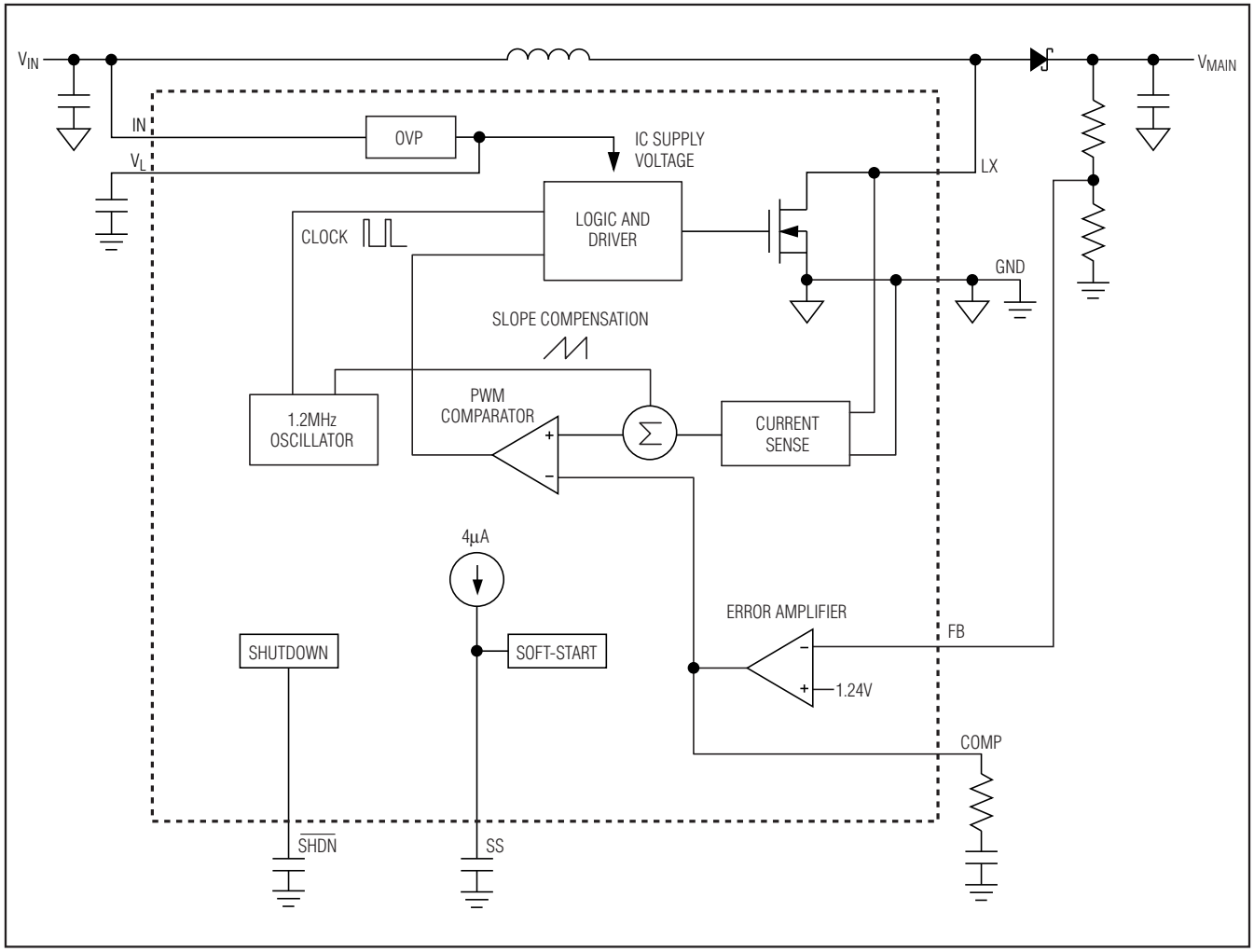


Figure 2. Functional Diagram

Detailed Description

The MAX17112 is a highly efficient, power-management IC that employs a current-mode, fixed-frequency, PWM architecture for fast-transient response and low-noise operation. The high switching frequency (1MHz) allows the use of ultra-small inductors and low-ESR ceramic capacitors. The current-mode architecture provides fast-transient response to pulsed loads. A compensation pin (COMP) gives users flexibility in adjusting loop dynamics. The internal MOSFET can generate output voltages up to 20V from a 2.6V to 5.5V input voltage. The soft-start function slowly ramps the input current and is programmable with an external capacitor. The input overvoltage protection function prevents damage to the MAX17112 from input surge voltages up to 24V.

The error amplifier compares the signal at FB to 1.24V and varies the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load changes, the error amplifier sources or sinks current to the COMP output to command the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal. At light loads, this architecture allows the device to skip cycles to prevent overcharging the output capacitors.

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Output Current Capability

The output current capability of the MAX17112 is a function of current limit, input voltage, operating frequency, and inductor value. Because of the slope compensation used to stabilize the feedback loop, the inductor current limit depends on the duty cycle. The current limit is determined by the following equation:

$$I_{LIM} = (1.26 - 0.35 \times D) \times I_{LIM\_EC}$$

where I_{LIM_EC} is the current limit specified at 75% duty cycle (see the *Electrical Characteristics* table) and D is the duty cycle.

The output current capability depends on the current-limit value and is governed by the following equation:

$$I_{OUT(MAX)} = \left[I_{LIM} - \frac{0.5 \times D \times V_{IN}}{f_{OSC} \times L} \right] \times \frac{V_{IN}}{V_{OUT}} \times \eta$$

where I_{LIM} is the current limit calculated above, η is the regulator efficiency (85% nominal), D is the duty cycle, and f_{OSC} is switching frequency. The duty cycle when operating at the current limit is:

$$D = \frac{V_{OUT} - V_{IN} + V_{DIODE}}{V_{OUT} - I_{LIM} \times R_{ON} + V_{DIODE}}$$

where V_{DIODE} is the rectifier diode forward voltage and R_{ON} is the on-resistance of the internal MOSFET.

Soft-Start

The MAX17112 can be programmed for soft-start upon power-up with an external capacitor. When the shutdown pin is taken high, the soft-start capacitor (C_{SS}) is immediately charged to 0.4V. Then the capacitor is charged at a constant current of 4µA (typ). During this time, the SS voltage directly controls the peak inductor current period. Full current limit is readied at V_{SS} = 1.5V. The maximum load current is available after the soft-start is completed. When $\overline{SHDN}$ is low, SS is discharged to ground.

Overvoltage Protection (OVP)

To prevent damage due to an input surge voltage, the MAX17112 integrates an OVP circuit. There is an internal switch between IN and V_L, which is on when the IN voltage is less than 6.6V (typ). The switch is off when the IN exceeds 6.6V (typ). Since V_L supplies the IC, the switch protects the IC from damage when excessively high voltage is applied to IN.

V_L Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit compares the voltage at V_L with the UVLO (2.45V typ) to ensure that the input voltage is high enough for reliable operation. The 50mV (typ) hysteresis prevents supply transients from causing a restart. Once the V_L voltage exceeds the UVLO-rising threshold, the startup begins. When the input voltage falls below the UVLO-falling threshold, the main step-up regulator turns off.

Startup Using $\overline{SHDN}$

The MAX17112 can be enabled by applying high voltage on the $\overline{SHDN}$ pin. Figure 2 shows the block diagram of the internal $\overline{SHDN}$ pin function. There are two ways to apply this high voltage. When $\overline{SHDN}$ is connected to an external capacitor, an internal 5µA current source charges up this capacitor and when the voltage on $\overline{SHDN}$ passes 1.24V, the IC starts up. Another way to enable the IC through the $\overline{SHDN}$ pin is to directly apply a logic-high signal to $\overline{SHDN}$ instead of connecting a capacitor.

The delay time for startup by connecting an external capacitor at $\overline{SHDN}$ can be estimated using the following equation:

$$t_{Delay} = \frac{1.24V}{5\mu A} \times C_{\overline{SHDN}} \approx 0.25 \times C_{\overline{SHDN}}$$

where $C_{\overline{SHDN}}$ is in microfarads.

When enabling the IC by applying a logic-high signal to $\overline{SHDN}$, a series resistor should be inserted between the logic signal and $\overline{SHDN}$ for protection purposes. This resistor can help limit the current drawn from the logic signal supply into the $\overline{SHDN}$ pin when $\overline{SHDN}$ is discharged to GND through the internal switch at the moment of startup when V_L < UVLO. A typical value for this resistor is 10kΩ. Figure 3 shows the application circuit for this enabling method of applying a logic-high signal to $\overline{SHDN}$ through a 10kΩ resistor.

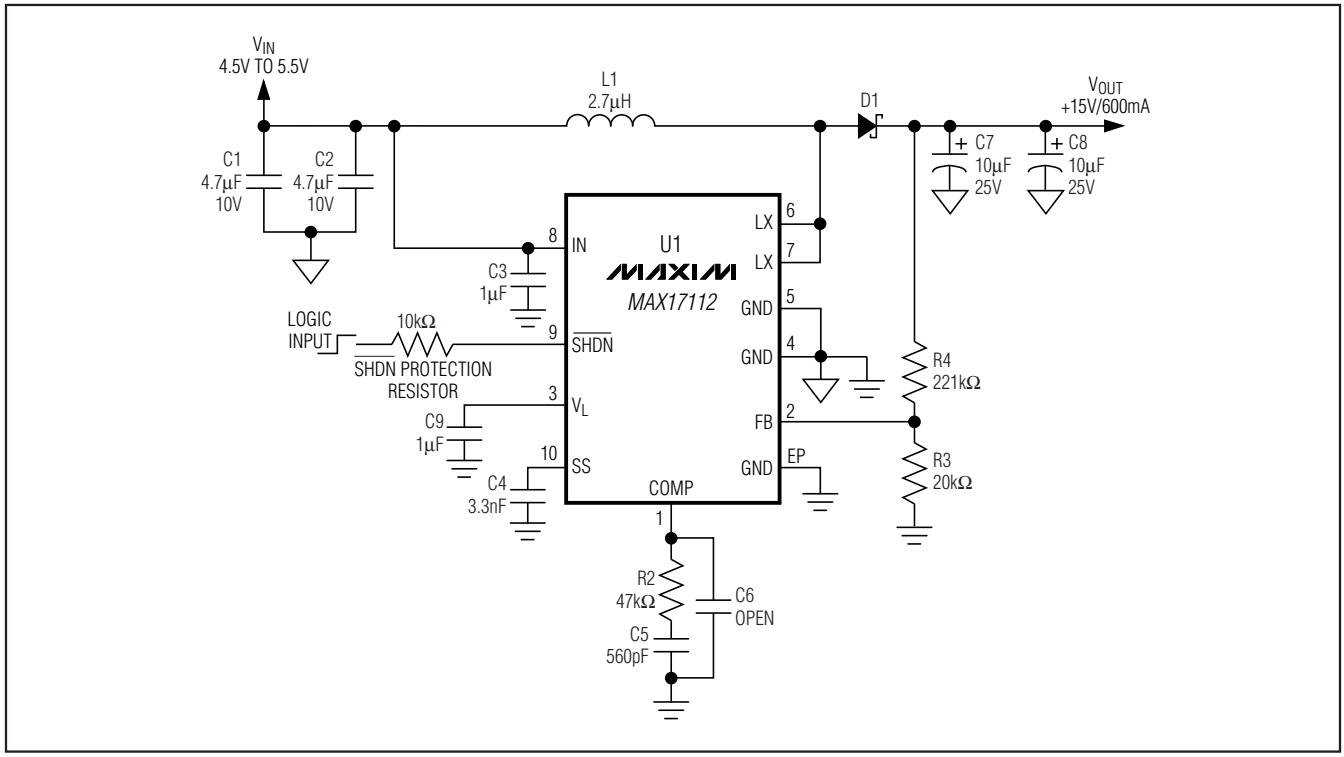

Figure 3. Application Circuit Using Logic Input at $\overline{SHDN}$

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	4.7µF ±10%, 10V X5R ceramic capacitors (0603) TDK C1608X5R1A475K
C7, C8	10µF ±10%, 25V X5R ceramic capacitors (1210) Murata GRM32DR61E106K
L1	2.7µH ±20% power inductor TOKO FDV0630-2R7 (27mΩ, 4.4A) Sumida CDRH5D18BHPNP-2R7M (65mΩ, 3.9A)

Table 2. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Murata	770-436-1300	www.murata.com
Sumida	408-321-9660	www.sumida.com
TDK	516-535-2600	www.component.tdk.com

Applications Information

Step-up regulators using the MAX17112 can be designed by performing simple calculations for a first iteration. All designs should be prototyped and tested prior to production. Table 1 provides a list of power components for the typical applications circuit. Table 2 lists component suppliers.

The choice of external components is primarily dictated by output voltage, maximum load current, and maximum and minimum input voltages. Begin by selecting an inductor value. Once the inductance is known, choose the diode and capacitors.

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. Physical size and cost are also important factors to be considered.

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The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple, and therefore, reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size, but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple is acceptable to reduce the number of turns required, and to increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses through the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage, $V_{IN(MIN)}$, using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{OUT}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17112's LX current limit (I_{LIM}) should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 600mA with a 15V output and a typical input voltage of 5V. Choosing an LIR of 0.5 and estimating 85% efficiency at this operating point:

$$L = \left(\frac{5V}{15V}\right)^2 \left(\frac{15V - 5V}{0.6A \times 1.2MHz}\right)\left(\frac{0.85}{0.5}\right) \approx 2.7\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating 85% efficiency at this operating point:

$$I_{IN(DC,MAX)} = \frac{0.6A \times 15V}{4.5V \times 0.85} \approx 2.35A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{4.5V \times (15V - 4.5V)}{2.7\mu H \times 15V \times 1.2MHz} \approx 0.97A$$

$$I_{PEAK} = 2.35A + \frac{0.97A}{2} = 2.84A$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 4.7µF ceramic capacitors are used in the typical operating circuit in Figure 1 because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in Figure 1. Ensure a low-noise supply at IN by using adequate C_{IN}. Alternatively, greater voltage variation can be tolerated on C_{IN} if IN is decoupled from C_{IN} using an RC lowpass filter (see Figure 1).

Rectifier Diode Selection

The MAX17112 high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. The diode should be rated to handle the output voltage and the peak switch current. Make sure that the diode's peak current rating is at least I_{PEAK} calculated in the *Inductor Selection* section and that its breakdown voltage exceeds the output voltage.

Output Voltage Selection

The MAX17112 operates with an adjustable output from V_{IN} to 20V. Connect a resistive voltage-divider from the output (V_{MAIN}) to GND with the center tap connected to FB (see Figure 1). Select R3 in the 10kΩ to 50kΩ range. Calculate R4 with the following equation:

$$R4 = R3 \times \left(\frac{V_{MAIN}}{V_{FB}} - 1 \right)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.24V (typ). Place R3 and R4 as close as possible to the IC.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{253 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{OUT}}$$

$$C_{COMP} \approx \frac{V_{OUT} \times C_{OUT}}{10 \times I_{OUT} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

Soft-Start Capacitor

The soft-start capacitor should be large enough so that it does not reach final value before the output has reached regulation. Calculate C_{SS} to be:

$$C_{SS} > 21 \times 10^{-6} \times C_{OUT} \times \left[\frac{V_{OUT}^2 - V_{IN} \times V_{OUT}}{V_{IN} \times I_{INRUSH} - I_{OUT} \times V_{OUT}} \right]$$

where C_{OUT} is the total output capacitance including any bypass capacitor on the output bus, V_{OUT} is the maximum output voltage, I_{INRUSH} is the peak inrush current allowed, I_{OUT} is the maximum output current during power-up, and V_{IN} is the minimum input voltage.

The load must wait for the soft-start cycle to finish before drawing a significant amount of load current. The soft-start duration after which the load can begin to draw maximum load current is:

$$t_{MAX} = 2.4 \times 10^5 \times C_{SS}$$

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

1) Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near the LX and GND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of GND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

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2) Create a power ground island (PGND) consisting of the input and output capacitor grounds and GND pins. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the feedback-divider ground connection, the COMP and SS capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the GND pins directly to the exposed backside pad. Make no other connections between these separate ground planes.
3) Place the feedback-voltage-divider resistors as close as possible to the feedback pin. The divider's center trace should be kept short. Placing the resistors far away causes the FB trace to become an antenna that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX or the switching nodes in the charge pumps.
4) Place IN and V_L pin bypass capacitors as close as possible to the device. The ground connections of the IN and V_L bypass capacitor should be connected directly to the AGND with a wide trace.
5) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
6) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as a shield if necessary.

Refer to the MAX17112 evaluation kit for an example of proper board layout.

Chip Information

TRANSISTOR COUNT: 4624

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 TDFN-EP	T1033+2	**21-0137**

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