

Absolute Maximum Ratings

V _{CC} to GND	-0.3V to + 6V	Operating Temperature Range.....	-40°C to +125°C
All Other Pins	-0.3V to (V _{CC} + 0.3V)	Junction Temperature.....	+150°C
Current into IN+, IN-, IN+, IN-	±40mA	Storage Temperature Range	-65°C to +150°C
Current into All Other Pins.....	±20mA	Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit (OUT _L , OUT) to GND.....	10s	Soldering Temperature (reflow).....	+260°C
Continuous Power Dissipation (T _A = +70°C) (Note 1)			
10-Pin μMAX (derate 8.8mW/°C above +70°C).....	707.3mW		
16-Pin QSOP (derate 9.6mW/°C above +70°C).....	771.5mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

μMAX	QSOP		
Junction-to-Ambient Thermal Resistance (θ _{JA})	113.1°C/W	Junction-to-Ambient Thermal Resistance (θ _{JA})	103.7°C/W
Junction-to-Case Thermal Resistance (θ _{JC}).....	42°C/W	Junction-to-Case Thermal Resistance (θ _{JC}).....	37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <http://www.maximintegrated.com/thermal-tutorial>.

Electrical Characteristics

(V_{CC} = 5V, V_{GND} = 0V, MAX9925/MAX9927 gain setting = 1V/V, Mode A1, V_{BIAS} = 2.5V, V_{PULLUP} = 5V, R_{PULLUP} = 1kΩ, C_{COU}T = 50pF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Operating Supply Range	V _{CC}	(Note 3)	4.5		5.5	V
Supply Current	I _{CC}	MAX9924/MAX9925		2.6	5	mA
		MAX9926/MAX9927		4.7	10	
Power-On Time	P _{ON}	V _{CC} > V _{UVLO} = 4.1V, step time for V _{CC} ~ 1μs		30	150	μs
INPUT OPERATIONAL AMPLIFIER (MAX9925/MAX9927)						
Input Voltage Range	IN+, IN-	Guaranteed by CMRR	0		V _{CC}	V
Input Offset Voltage	V _{OS-OA}	Temperature drift			5	μV/°C
				0.5	3	mV
Input Bias Current	I _{BIAS}	(Note 4)		0.1	6	nA
Input Offset Current	I _{OFFSET}	(Note 4)		0.05	2	nA
Common-Mode Rejection Ratio	CMRR	From V _{CM} = 0 to V _{CC}	75	102		dB
Power-Supply Rejection Ratio	PSRR	MAX9925	88	105		dB
		MAX9927	77	94		
Output Voltage Low	V _{OL}	I _{OL} = 1mA			0.050	V
Output Voltage High	V _{OH}	I _{OH} = -1mA	V _{CC} -0.050			V
Recovery Time from Saturation	t _{SAT}	To 1% of the actual V _{OUT} after output saturates		1.2		μs
Gain-Bandwidth Product	GBW			1.4		MHz
Slew Rate	SR			2.3		V/μs
Charge-Pump Frequency	f _{CP}			1.3		MHz

Electrical Characteristics (continued)

(V_{CC} = 5V, V_{GND} = 0V, MAX9925/MAX9927 gain setting = 1V/V, Mode A1, V_{BIAS} = 2.5V, V_{PULLUP} = 5V, R_{PULLUP} = 1kΩ, C_{COU}T = 50pF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT DIFFERENTIAL AMPLIFIER (MAX9924/MAX9926)							
Input Voltage Range	IN+, IN-	Guaranteed by CMRR		-0.3		V _{CC} + 0.3	V
Differential Amplifier Common-Mode Rejection Ratio	CMRR	MAX9924 (Note 5)		60	87		dB
		MAX9926 (Note 5)		55	78		
Input Resistance	R _{IN}	(Note 5)		65	100	135	kΩ
ADAPTIVE PEAK DETECTION							
Zero-Crossing Threshold	V _{ZERO_THRESH}	Mode B operation (Notes 5, 6)	MAX9924/MAX9925	-6.5	0	+6.5	mV
			MAX9926/MAX9927	-6.5	0	+10	
Fixed and Adaptive Peak Threshold	V _{ADAPTIVE}	Adaptive peak threshold			33		%PK
	V _{MIN-THRESH}	Minimum threshold of hysteresis comparator MAX9924/MAX9926 (Notes 5, 6)		4	15	30	mV
		Minimum threshold of hysteresis comparator MAX9925/MAX9927 (Notes 5, 6)		20	30	50	
		V _{MIN-THRESH} - V _{ZERO-THRESH} for MAX9924 (Notes 5, 6)		7	15	26	
		V _{MIN-THRESH} - V _{ZERO-THRESH} for MAX9926 (Notes 5, 6)		2	15	30	
		V _{MIN-THRESH} - V _{ZERO-THRESH} for MAX9925/MAX9927 (Notes 5, 6)		19	30	50	
Watchdog Timeout for Adaptive Peak Threshold	t _{WD}	Timing window to reset the adaptive peak threshold if not triggered (input level below threshold)		45	85	140	ms
ENTIRE SYSTEM							
Comparator Output Low Voltage	V _{COU} T_OL					0.2	V
Propagation Delay	t _{PDZ}	Overdrive = 2V to 3V, zero-crossing path			50		ns
	t _{PDA}	Overdrive = 2V to 3V, adaptive peak path			150		
COUT Transition Time	t _{HL-LH}				2		ns
Propagation Delay Jitter	t _{PD-JITTER}	Includes noise of differential amplifier and comparator, f = 10kHz, V _{IN} = 1V _{P-P} sine wave			20		ns

Electrical Characteristics (continued)

($V_{CC} = 5V$, $V_{GND} = 0V$, MAX9925/MAX9927 gain setting = $1V/V$, Mode A1, $V_{BIAS} = 2.5V$, $V_{PULLUP} = 5V$, $R_{PULLUP} = 1k\Omega$, $C_{COUT} = 50pF$. $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXT						
EXT Voltage Range	V_{EXT}	Mode B, $T_A = +125^\circ C$	1.5		$V_{CC} - 1.1$	V
		Mode C, $T_A = +125^\circ C$	0.14		$V_{CC} - 1.1$	V
Input Current to EXT	I_{EXT}	Mode B, $V_{EXT} > V_{BIAS}$; and Mode C			10	μA
DIRN (MAX9926 Only)						
Output Low Voltage					0.2	V
INT_THRS, ZERO_EN						
Low Input	V_{IL}				$0.3 \times V_{CC}$	V
High Input	V_{IH}		$0.7 \times V_{CC}$			V
Input Leakage	I_{LEAK}				1	μA
Input Current ZERO_EN	I_{SINK}	Pullup resistor = $10k\Omega$, $V_{ZERO_EN} = V_{GND}$		500	800	μA
Switching Time Between Modes A1, A2, and Modes B, C	t_{SW}	With INT_THRS = GND, auto peak-detect is disabled, and EXT_THRS is active		3		μs
BIAS						
Input Current to BIAS	I_{BIAS}	Modes A1, A2, B, C			1	μA
BIAS Voltage Range	V_{BIAS}	Modes A1, B, $T_A = +125^\circ C$	1.5		$V_{CC} - 1.1$	V
		Mode C, $T_A = +125^\circ C$	0.2		$V_{CC} - 1.1$	V
Internal BIAS Reference Voltage	V_{INT_BIAS}	Mode A2 (MAX9924/MAX9926)		2.46		V

Note 2: Specifications are 100% tested at $T_A = +125^\circ C$, unless otherwise noted. All temperature limits are guaranteed by design.

Note 3: Inferred from functional PSRR.

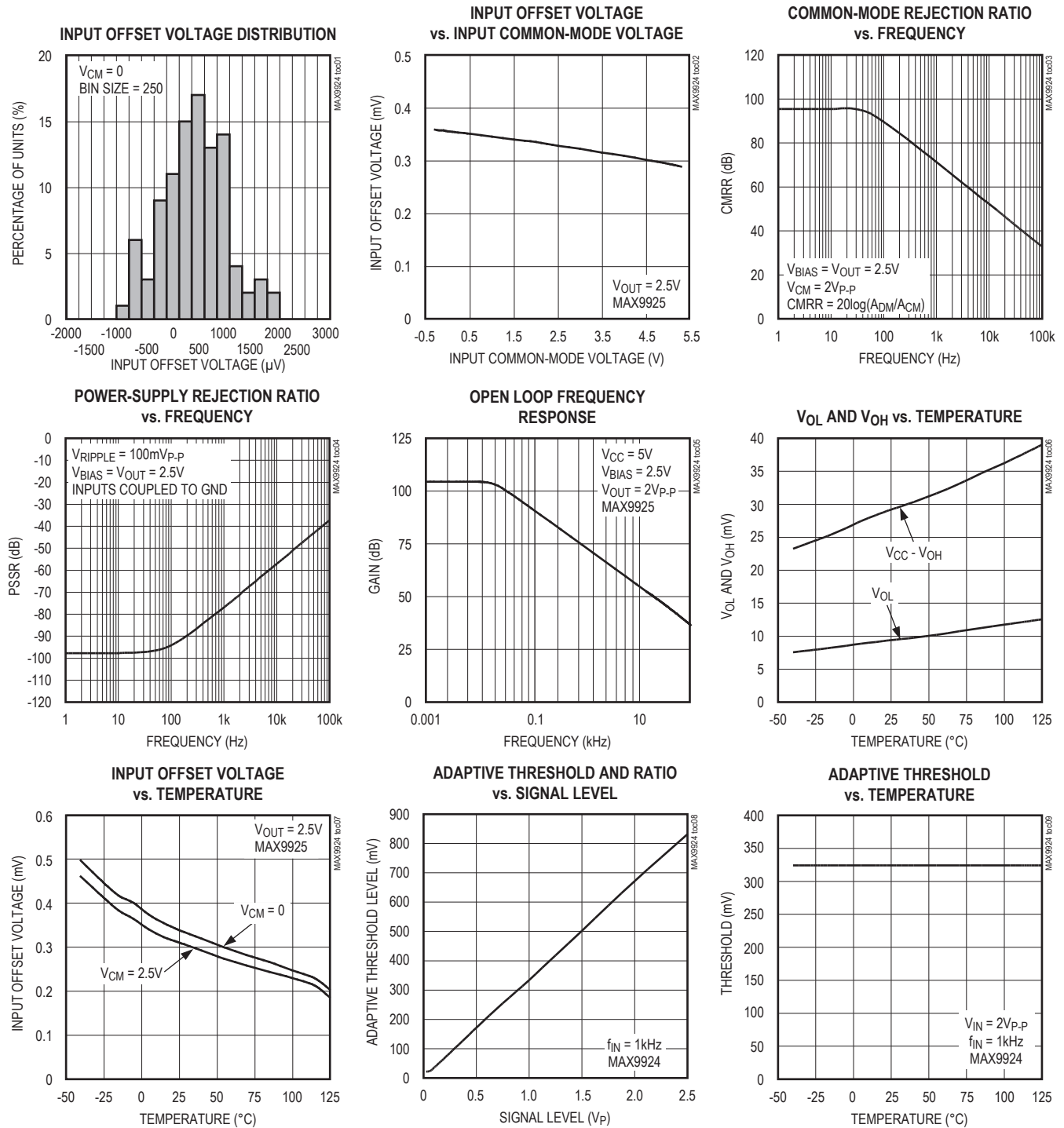
Note 4: CMOS inputs.

Note 5: Guaranteed by design.

Note 6: Includes effect of V_{OS} of internal op amp and comparator.

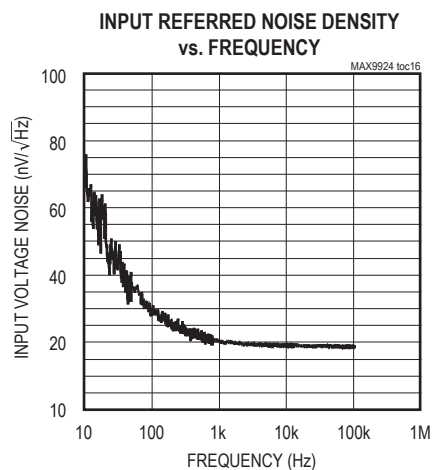
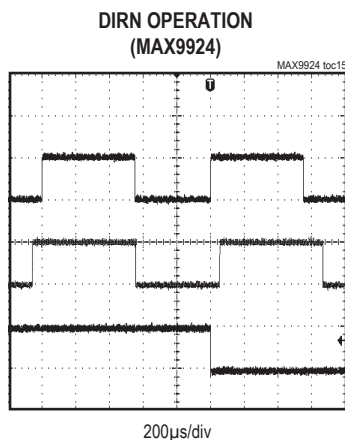
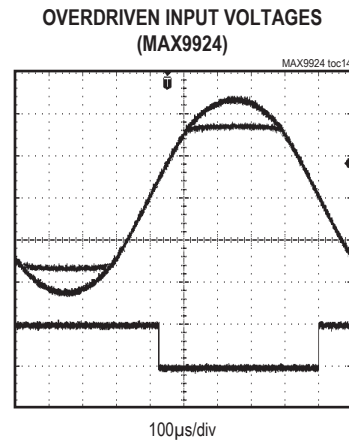
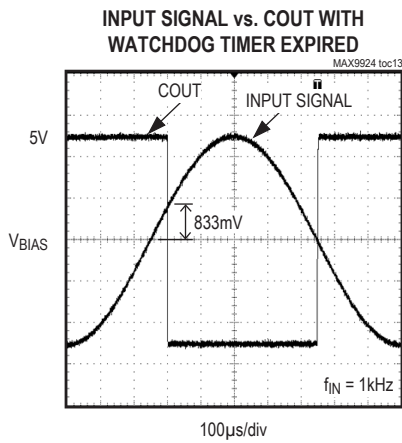
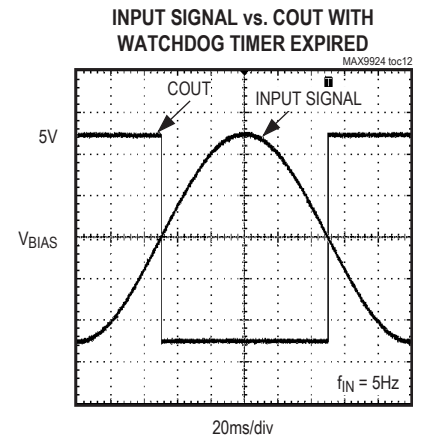
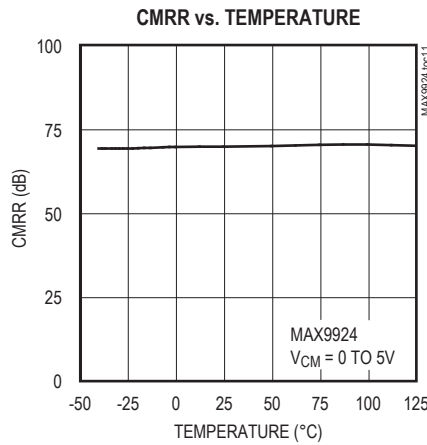
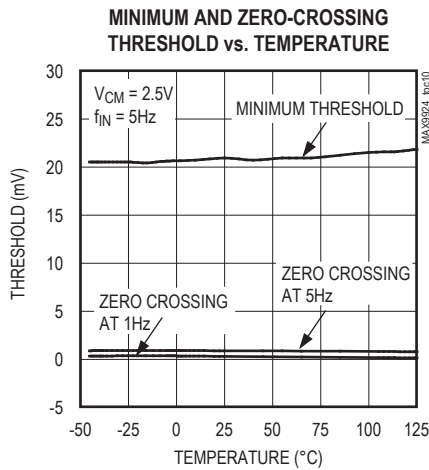
Typical Operating Characteristics

($V_{CC} = 5V$, $V_{GND} = 0V$, MAX9925/MAX9927 gain setting = 1V/V. All values are at $T_A = +25^\circ C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

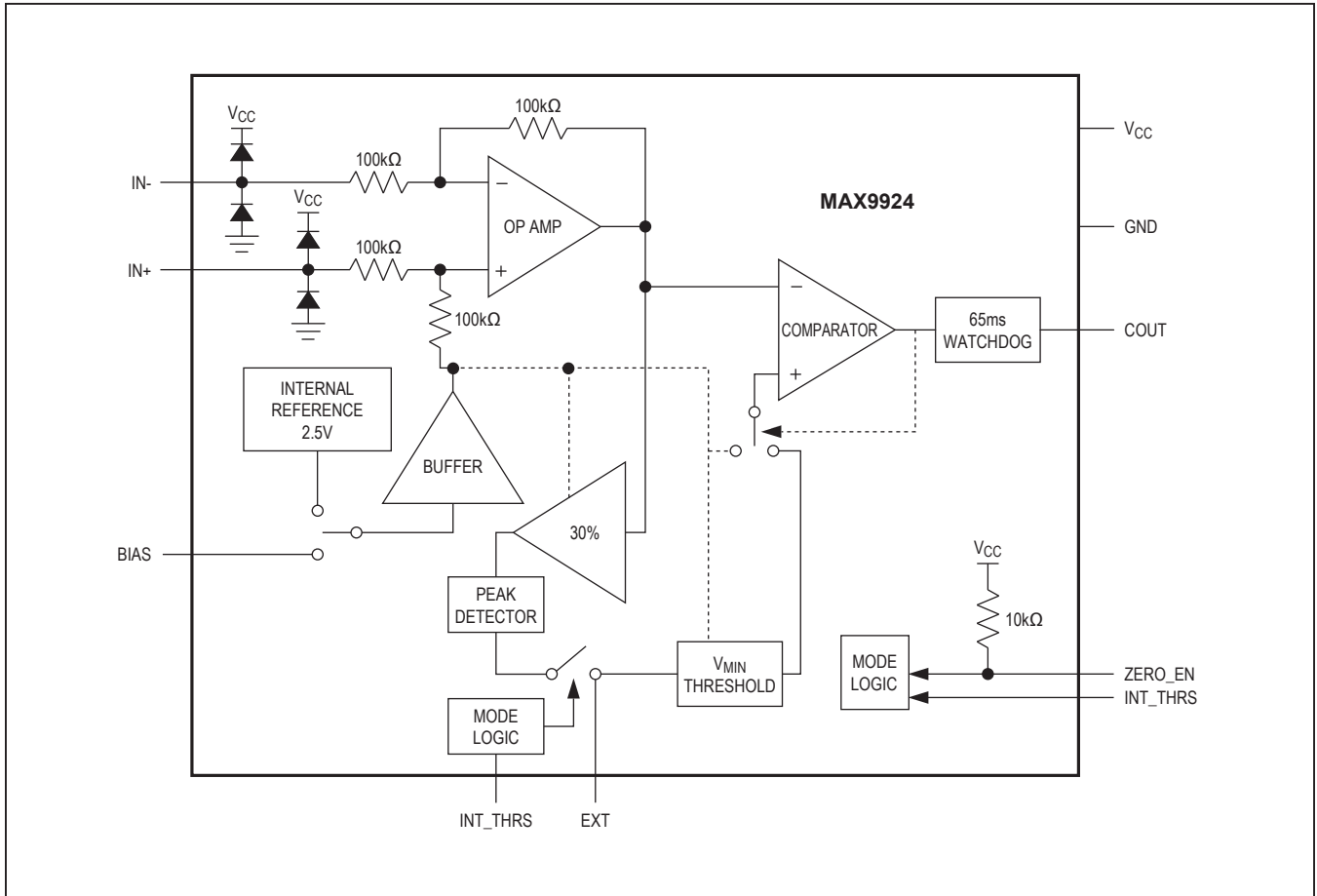
($V_{CC} = 5V$, $V_{GND} = 0V$, MAX9925/MAX9927 gain setting = 1V/V. All values are at $T_A = +25^\circ C$, unless otherwise noted.)



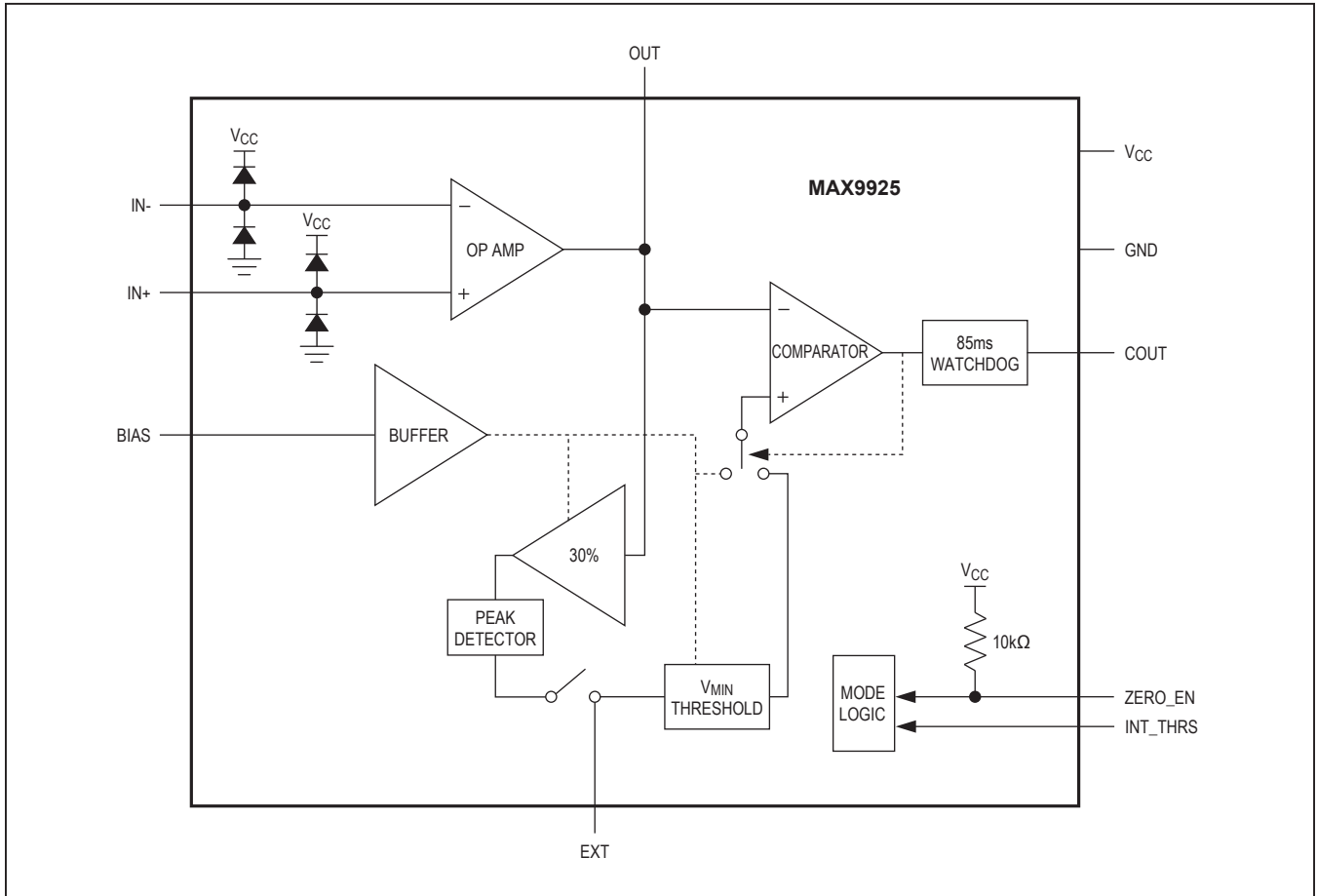
Pin Description

PIN				NAME	FUNCTION
MAX9924	MAX9925	MAX9926	MAX9927		
1	1	—	—	IN+	Noninverting Input
2	2	—	—	IN-	Inverting Input
—	3	—	—	OUT	Amplifier Output
3	—	—	—	N.C.	No Connection. Not internally connected.
4	4	—	—	BIAS	Input Bias. Connect to an external resistor-divider and bypass to ground with a 0.1 μ F and 10 μ F capacitor.
5	5	11	11	GND	Ground
6	6	13	—	ZERO_EN	Zero-Crossing Enable. Mode configuration pin, internally pulled up to V _{CC} with 10k Ω resistor.
7	7	—	—	COUT	Comparator Output. Open-drain output, connect a 10k Ω pullup resistor from COUT to V _{PULLUP} .
8	8	—	—	EXT	External Reference Input. Leave EXT unconnected in Modes A1, A2. Apply an external voltage in Modes B, C.
9	9	—	—	INT_THRS	Internal Adaptive Threshold. Mode configuration pin.
10	10	14	14	V _{CC}	Power Supply
—	—	1	1	INT_THRS1	Internal Adaptive Threshold 1. Mode configuration pin.
—	—	2	2	EXT1	External Reference Input 1. Leave EXT unconnected in Modes A1, A2. Apply an external voltage in Modes B, C.
—	—	3	3	BIAS1	Input Bias 1. Connect to an external resistor-divider and bypass to ground with a 0.1 μ F and 10 μ F capacitor.
—	—	4	4	COUT1	Comparator Output 1. Open-drain output, connect a 10k Ω pullup resistor from COUT1 to V _{PULLUP} .
—	—	5	5	COUT2	Comparator Output 2. Open-drain output, connect a 10k Ω pullup resistor from COUT2 to V _{PULLUP} .
—	—	6	6	BIAS2	Input Bias 2. Connect to an external resistor-divider and bypass to ground with a 0.1 μ F and 10 μ F capacitor.
—	—	7	7	EXT2	External Reference Input 2. Leave EXT unconnected in Modes A1, A2. Apply an external voltage in Modes B, C.
—	—	8	8	INT_THRS2	Internal Adaptive Threshold 2. Mode configuration pin.
—	—	9	9	IN2+	Noninverting Input 2
—	—	10	10	IN2-	Inverting Input 2
—	—	12	—	DIRN	Rotational Direction Output. Open-drain output, connect a pullup resistor from DIRN to V _{PULLUP} .
—	—	—	12	OUT2	Amplifier Output 2
—	—	—	13	OUT1	Amplifier Output 1
—	—	15	15	IN1-	Noninverting Input 1
—	—	16	16	IN1+	Inverting Input 1

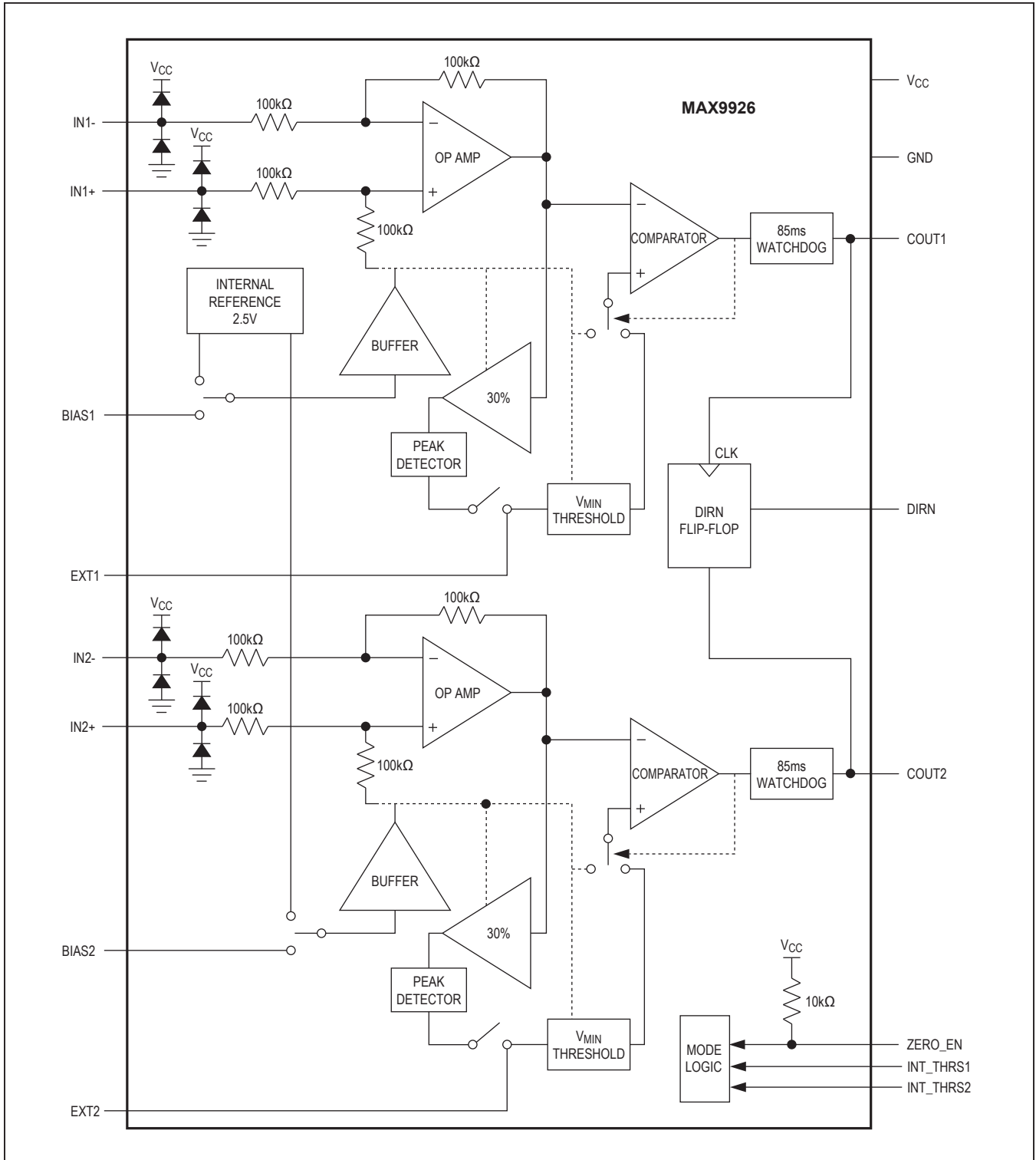
Functional Diagrams



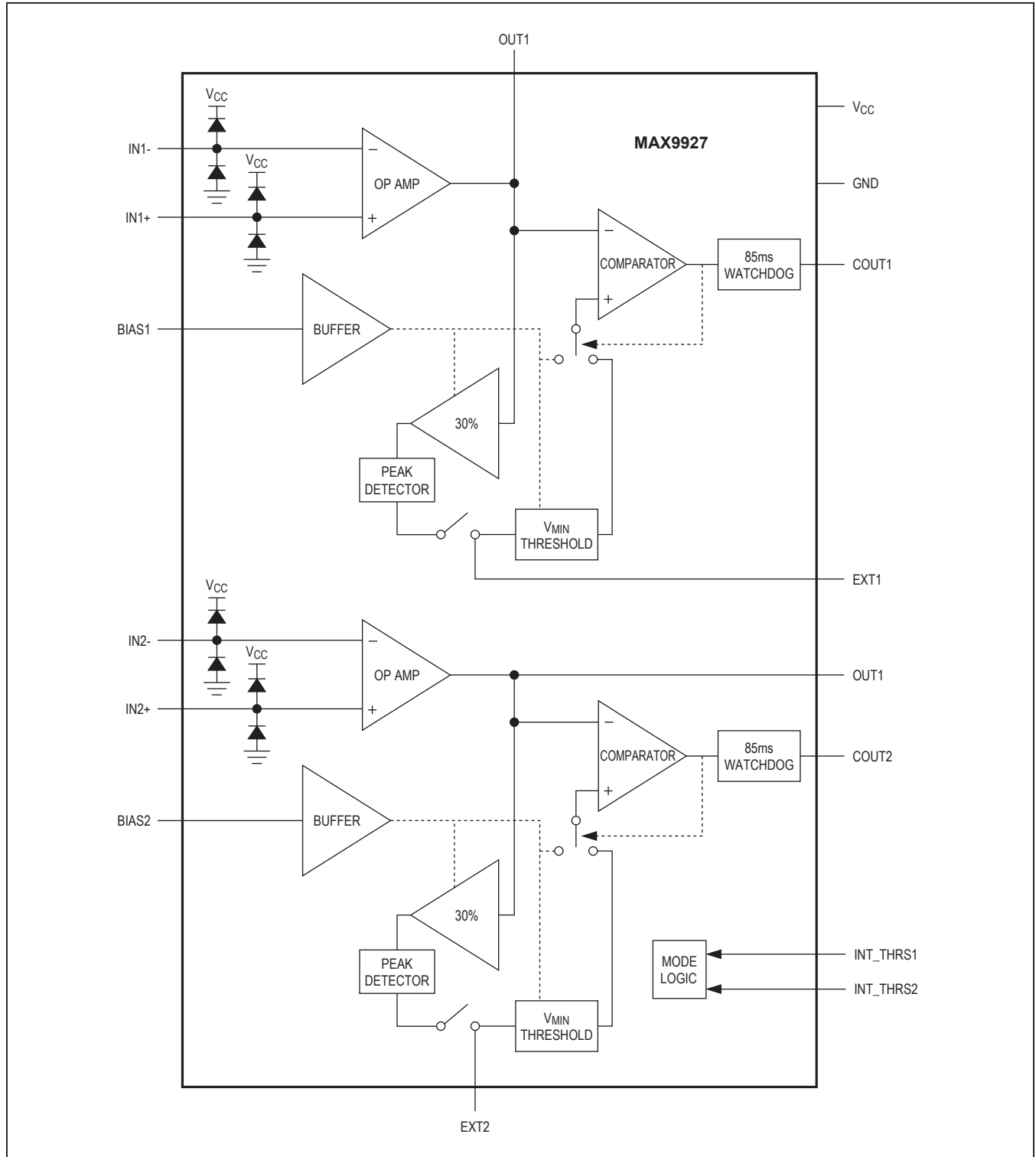
Functional Diagrams (continued)



Functional Diagrams (continued)



Functional Diagrams (continued)



Detailed Description

The MAX9924–MAX9927 interface with variable reluctance (VR) or magnetic coil sensors. These devices produce accurate pulses aligned with flywheel gear-teeth even when the pickup signal is small and in the presence of large amounts of system noise. They interface with new-generation differential VR sensors as well as legacy single-ended VR sensors.

The MAX9924/MAX9925 integrate a precision op amp, a precision comparator, an adaptive peak threshold block, a zero-crossing detection circuit, and precision matched resistors (MAX9924). The MAX9926 and MAX9927 are dual versions of the MAX9924 and MAX9925, respectively. The MAX9926 also provides a rotational output that is useful for quadrature-connected VR sensors used in certain high-performance engines.

The input op amp in the MAX9925/MAX9927 are typically configured as a differential amplifier by using four external resistors (the MAX9924/MAX9926 integrate precision-matched resistors to give superior CMRR performance). This input differential amplifier rejects input common-mode noise and converts the input differential signal from a VR sensor into a single-ended signal. The internal comparator produces output pulses by comparing the output

of the input differential amplifier with a threshold voltage that is set depending on the mode that the device is in (see the *Mode Selection* section).

Mode Selection

The MAX9924/MAX9926 provide four modes of operation: Mode A1, Mode A2, Mode B, and Mode C as determined by voltages applied to inputs ZERO_EN and INT_THRS (see Tables 1, 2, and 3). In Modes A1 and A2, the internal adaptive peak threshold and the zero-crossing features are enabled. In Mode A2, an internally generated reference voltage is used to bias the differential amplifier and all internal circuitry instead of an external voltage connected to the BIAS input—this helps reduce external components and design variables leading to a more robust application. In Mode B, the adaptive peak threshold functionality is disabled, but zero-crossing functionality is enabled. In this mode, an external threshold voltage is applied at EXT allowing application-specific adaptive algorithms to be implemented in firmware. In Mode C, both the adaptive peak threshold and zero-crossing features are disabled and the device acts as a high-performance differential amplifier connected to a precision comparator (add external hysteresis to the comparator for glitch-free operation).

Table 1. MAX9924/MAX9926 Operating Modes

OPERATING MODE	SETTING		DEVICE FUNCTIONALITY		
	ZERO_EN	INT_THRS	ZERO CROSSING	ADAPTIVE PEAK THRESHOLD	BIAS VOLTAGE SOURCE
A1	V _{CC}	V _{CC}	Enabled	Enabled	External
A2	GND	GND	Enabled	Enabled	Internal Ref
B	V _{CC}	GND	Enabled	Disabled	External
C	GND	V _{CC}	Disabled	Disabled	External

Table 2. MAX9925 Operating Modes

OPERATING MODE	SETTING		DEVICE FUNCTIONALITY	
	ZERO_EN	INT_THRS	ZERO CROSSING	ADAPTIVE PEAK THRESHOLD
A1	V _{CC}	V _{CC}	Enabled	Enabled
B	V _{CC}	GND	Enabled	Disabled
C	GND	V _{CC}	Disabled	Disabled

Table 3. MAX9927 Operating Modes

OPERATING MODE	SETTING	DEVICE FUNCTIONALITY	
	INT_THRS	ZERO CROSSING	ADAPTIVE PEAK THRESHOLD
A1	V _{CC}	Enabled	Enabled
B	GND	Enabled	Disabled

Differential Amplifier

The input operational amplifier is a rail-to-rail input and output precision amplifier with CMOS input bias currents, low offset voltage (V_{OS}) and drift. A novel input architecture eliminates crossover distortion at the operational amplifier inputs normally found in rail-to-rail input structures. These features enable reliable small-signal detection for VR sensors.

The MAX9924/MAX9926 include on-chip precision-matched low-ppm resistors configured as a differential amplifier. High-quality matching and layout of these resistors produce extremely high DC and AC CMRR that is important to maintain noise immunity. The matched ppm-drift of the resistors guarantees performance across the entire -40°C to $+125^{\circ}\text{C}$ automotive temperature range.

Bias Reference

In Modes A1, B, and C, a well-decoupled external resistor-divider generates a $V_{CC}/2$ signal for the BIAS input that is used to reference all internal electronics in the device. BIAS should be bypassed with a $0.1\mu\text{F}$ and $10\mu\text{F}$ capacitor in parallel with the lower half of the resistor-divider forming a lowpass filter to provide a stable external BIAS reference.

The minimum threshold, adaptive peak threshold, zero-crossing threshold signals are all referenced to this voltage. An input buffer eliminates loading of resistor-dividers due to differential amplifier operation. Connect BIAS to ground when operating in Mode A2. An internal (2.5V typical) reference is used in Mode A2, eliminating external components.

Adaptive Peak Threshold

Modes A1 and A2 in the MAX9924–MAX9927 use an internal adaptive peak threshold voltage to trigger the output comparator. This adaptive peak threshold voltage scheme provides robust noise immunity to the input VR signal, preventing false triggers from occurring due to broken tooth or off-centered gear-tooth wheel. See Figure 1.

The sensor signal at the output of the differential gain stage is used to generate a cycle-by-cycle adaptive peak threshold voltage. This threshold voltage is $1/3$ of the peak of the previous cycle of the input VR signal. As the sensor signal peak voltage rises, the adaptive peak threshold voltage also increases by the same ratio. Conversely, decreasing peak voltage levels of the input VR signal causes the adaptive peak threshold voltage used to trigger the next cycle also to decrease to a new lower level. This threshold voltage then provides an arming level for the zero-crossing circuit of the comparator (see the *Zero Crossing* section).

If the input signal voltage remains lower than the adaptive peak threshold for more than 85ms, an internal watchdog timer drops the threshold level to a default minimum threshold (V_{MIN_THRESH}). This ensures pulse recognition recovers even in the presence of intermittent sensor connection.

The internal adaptive peak threshold can be disabled and directly fed from the EXT input. This mode of operation is called Mode B, and allows implementations of custom threshold algorithms in firmware. This EXT voltage is typically generated by filtering a PWM-modulated output from an onboard microcontroller (μC). An external operational amplifier can also be used to construct an active lowpass filter to filter the PWM-modulated EXT signal.

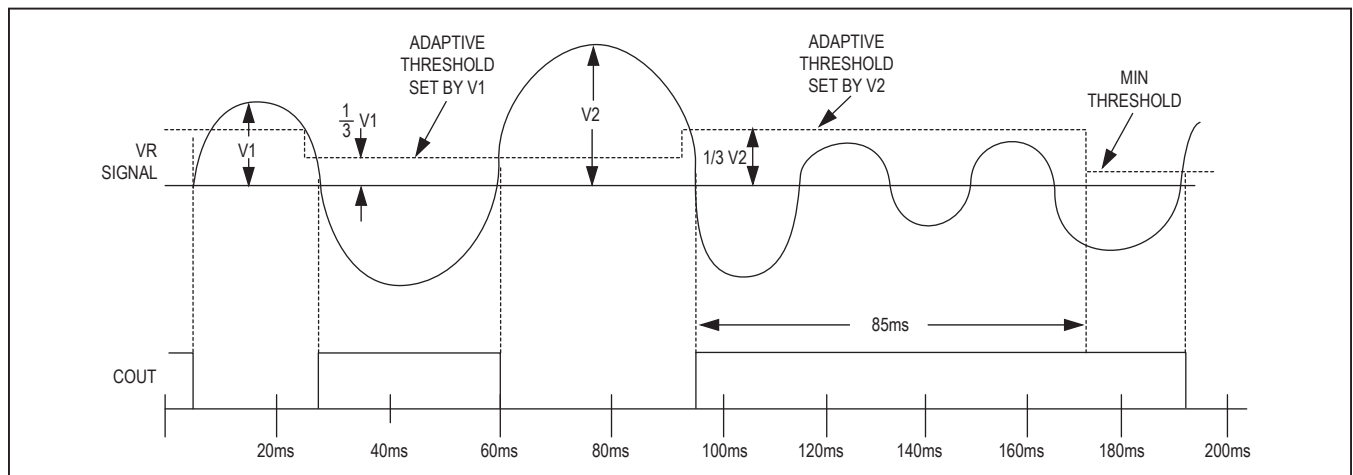


Figure 1. Adaptive Peak Threshold Operation

Zero Crossing

The zero-crossing signal provides true timing information for engine-control applications. The zero-voltage level in the VR sensor signal corresponds to the center of the gear-tooth and is the most reliable marker for position/angle-sensing applications. Since the output of the differential amplifier is level-shifted to the BIAS voltage, the zero of the input VR signal is simply BIAS. The comparator output state controls the status of the input switch that changes the voltage at its noninverting input from the adaptive/external threshold level to the BIAS level. The difference in these two voltages then effectively acts as hysteresis for the comparator, thus providing noise immunity.

Comparator

The internal comparator is a fast open-drain output comparator with low input offset voltage and drift. The comparator precision affects the ability of the signal chain to resolve small VR sensor signals. An open-drain output allows the comparator to easily interface to a variety of μC I/O voltages.

When operating the MAX9924/MAX9925/MAX9926 in Mode C, external hysteresis can be provided by adding external resistors (see Figures 5 and 8). The high and low hysteresis thresholds in Mode C can be calculated using the following equations:

$$V_{\text{TH}} = \left(\frac{R1(V_{\text{PULLUP}} - V_{\text{BIAS}})}{R1 + R2 + R_{\text{PULLUP}}} \right) + V_{\text{BIAS}}$$

and

$$V_{\text{TL}} = \left(\frac{R2}{R1 + R2} \right) \times V_{\text{BIAS}}$$

Rotational Direction Output (MAX9926 Only)

For quadrature-connected VR sensors, the open-drain output DIRN indicates the rotational direction of inputs IN1 and IN2 based on the output state of COUT1 and COUT2. DIRN goes high when COUT1 is leading COUT2, and low when COUT1 is following COUT2.

Applications Information

Bypassing and Layout Considerations

Good power-supply decoupling with high-quality bypass capacitors is always important for precision analog circuits. The use of an internal charge pump for the front-end amplifier makes this more important. Bypass capacitors create a low-impedance path to ground for noise present on the power supply.

The minimum impedance of a capacitor is limited to the effective series resistance (ESR) at the self-resonance frequency, where the effective series inductance (ESL) cancels out the capacitance. The ESL of the capacitor dominates past the self-resonance frequency resulting in a rise in impedance at high frequencies.

Bypass the power supply of the MAX9924–MAX9927 with multiple capacitor values in parallel to ground. The use of multiple values ensures that there will be multiple self-resonance frequencies in the bypass network, lowering the combined impedance over frequency. It is recommended to use low-ESR and low-ESL ceramic surface-mount capacitors in a parallel combination of 10nF, 0.1 μF and 1 μF , with the 10nF placed closest between the V_{CC} and GND pins. The connection between these capacitor terminals and the power-supply pins of the part (both V_{CC} and GND) should be through wide traces (preferably planes), and without vias in the high-frequency current path.

Input Filter Considerations

Add a series 10k Ω resistor to each input of the operational amplifier of the MAX9924/MAX9926 to limit the pin currents in case the internal ESD diodes are turned on. This can happen when the sensor pulse voltage is higher than the V_{CC} voltage. The series resistors lower the gain of the input amplifier and should be accounted for when setting the trigger threshold. Add a filter capacitor between the operational amplifier inputs to limit the input signal bandwidth.

Application Circuits

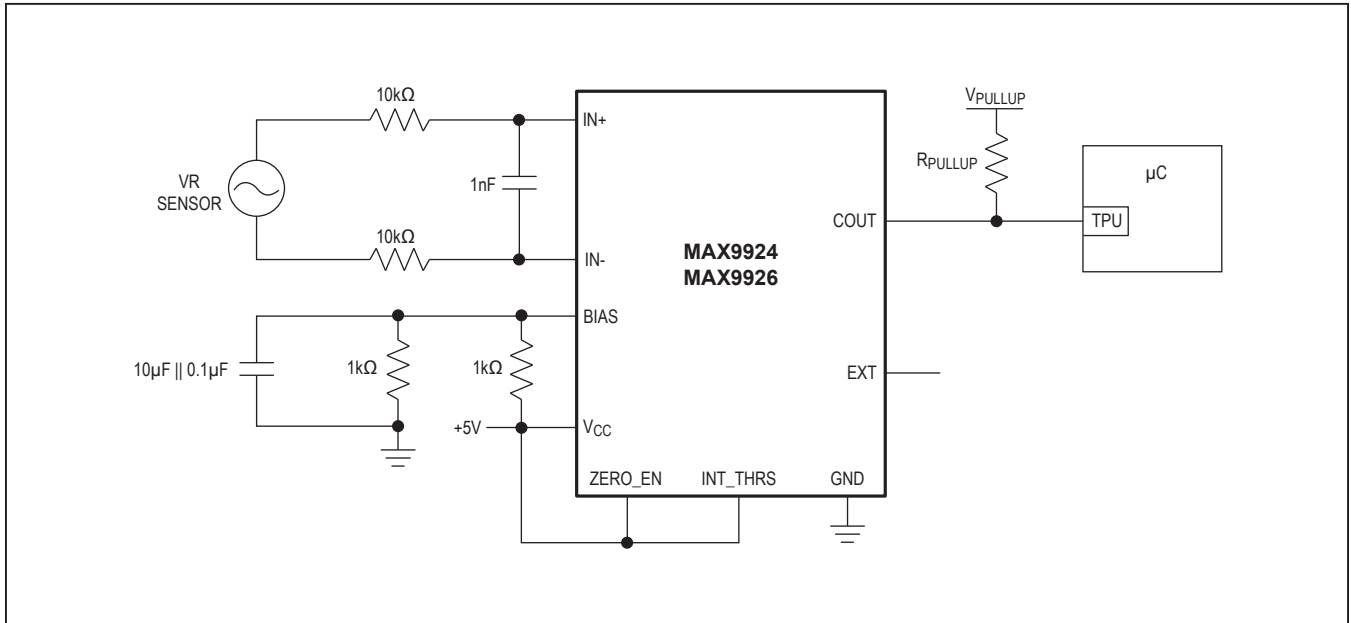


Figure 2. MAX9924/MAX9926 Operating Mode A1

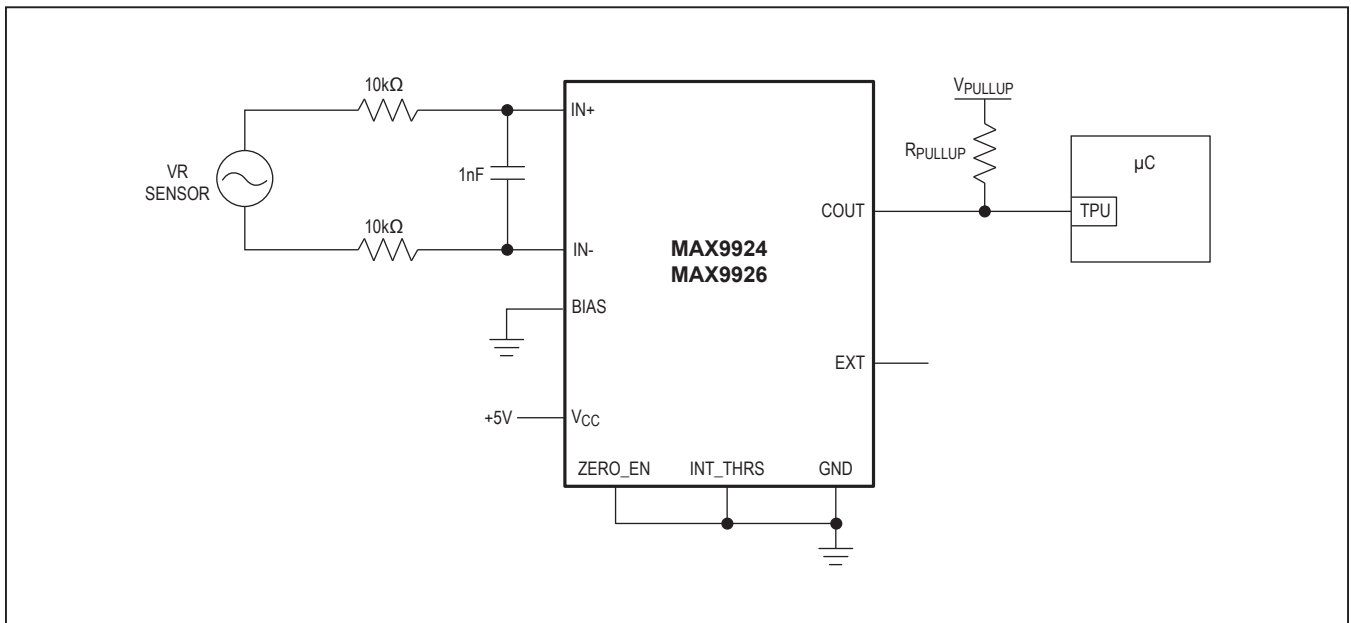


Figure 3. MAX9924/MAX9926 Operating Mode A2

Application Circuits (continued)

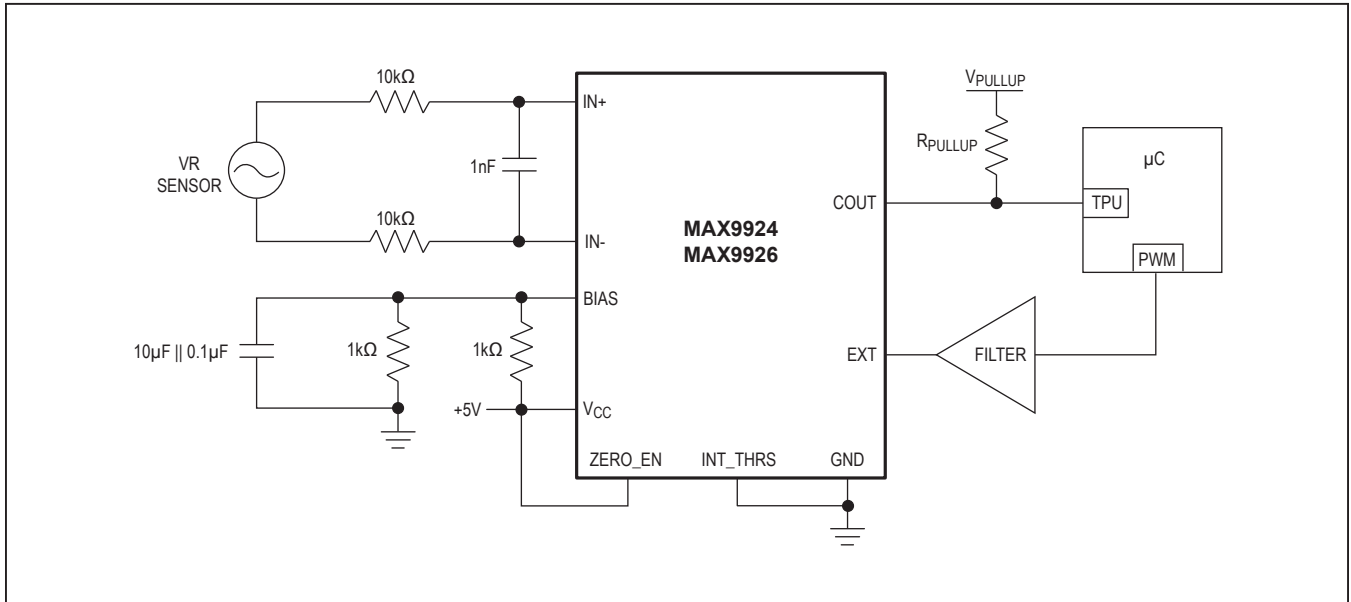


Figure 4. MAX9924/MAX9926 Operating Mode B

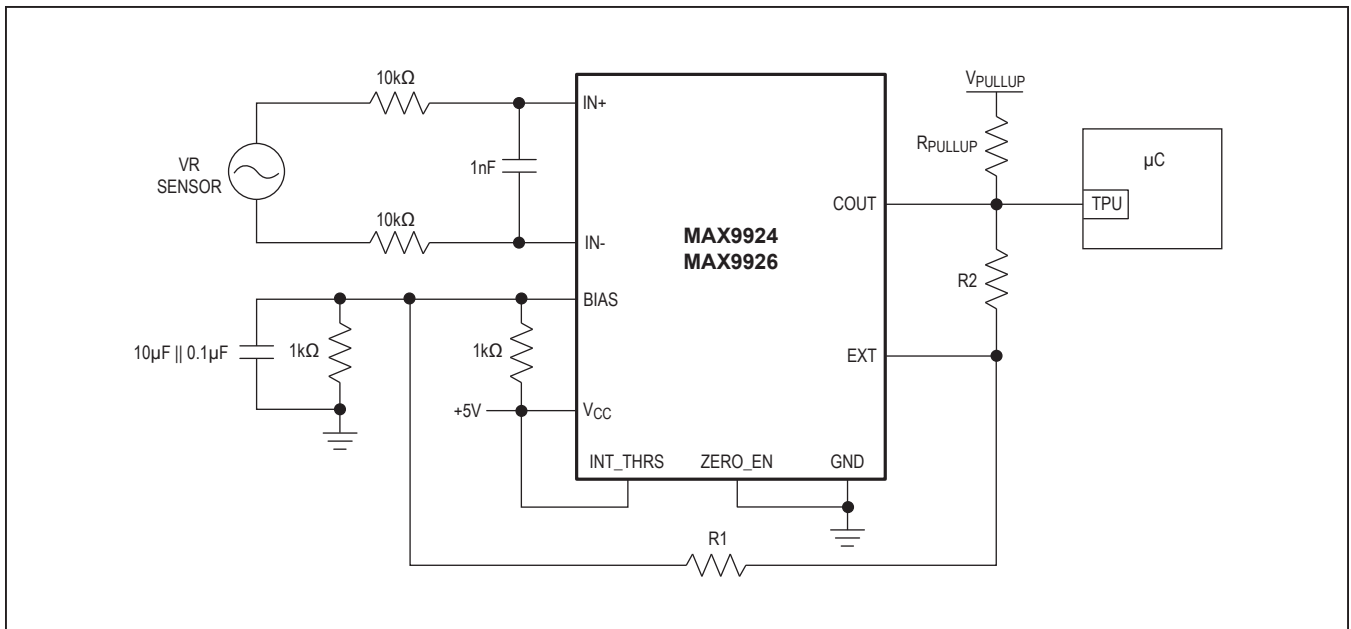


Figure 5. MAX9924/MAX9926 Operating Mode C

Application Circuits (continued)

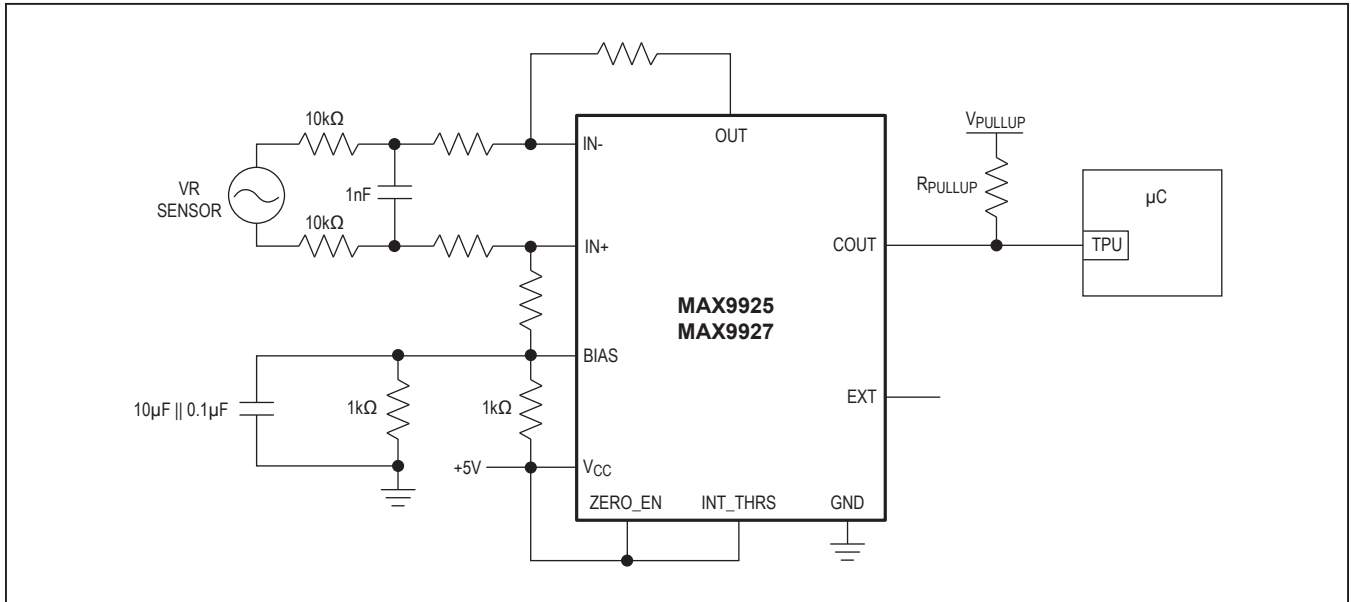


Figure 6. MAX9925/MAX9927 Operating Mode A

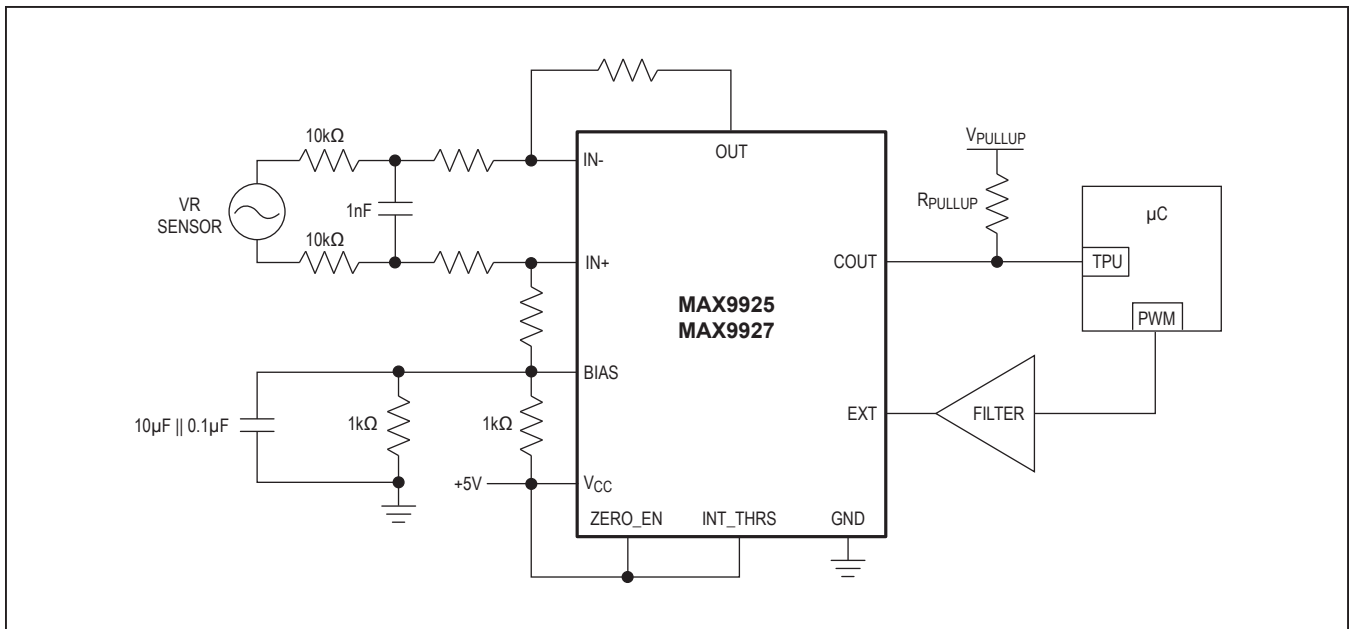


Figure 7. MAX9925/MAX9927 Operating Mode B

Application Circuits (continued)

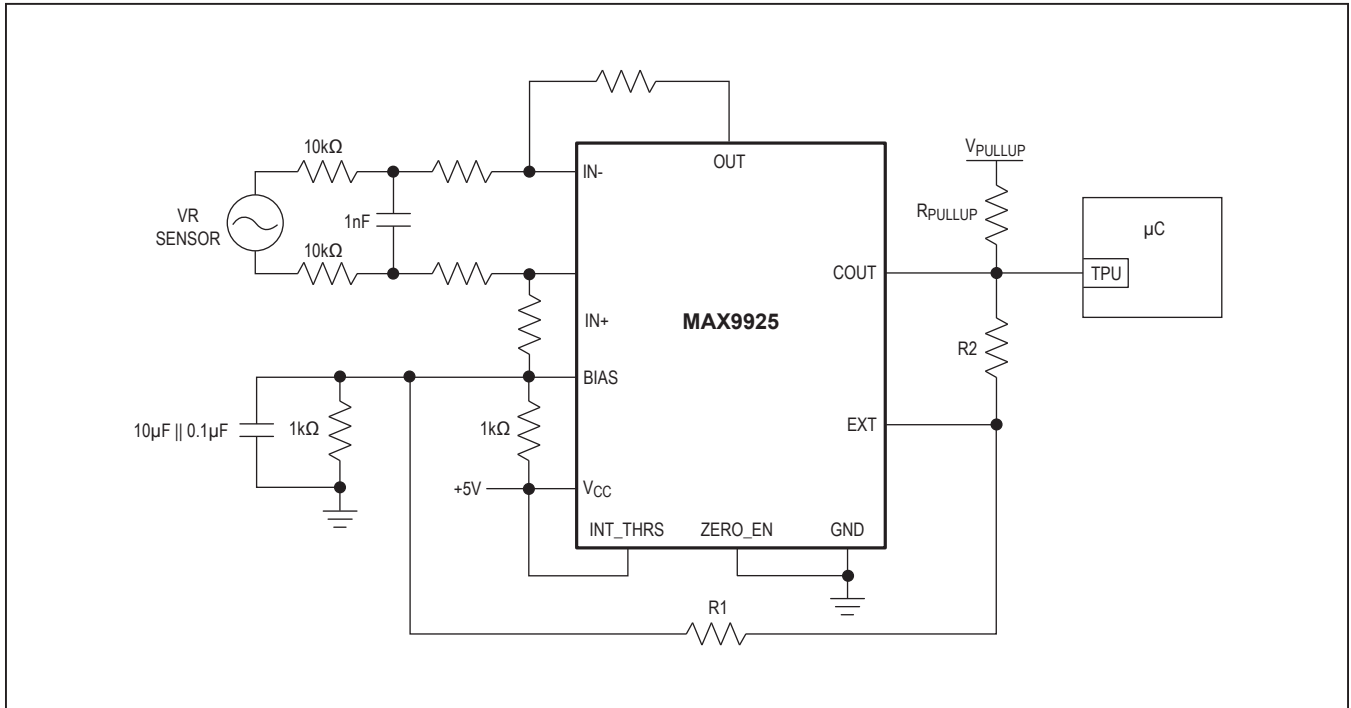
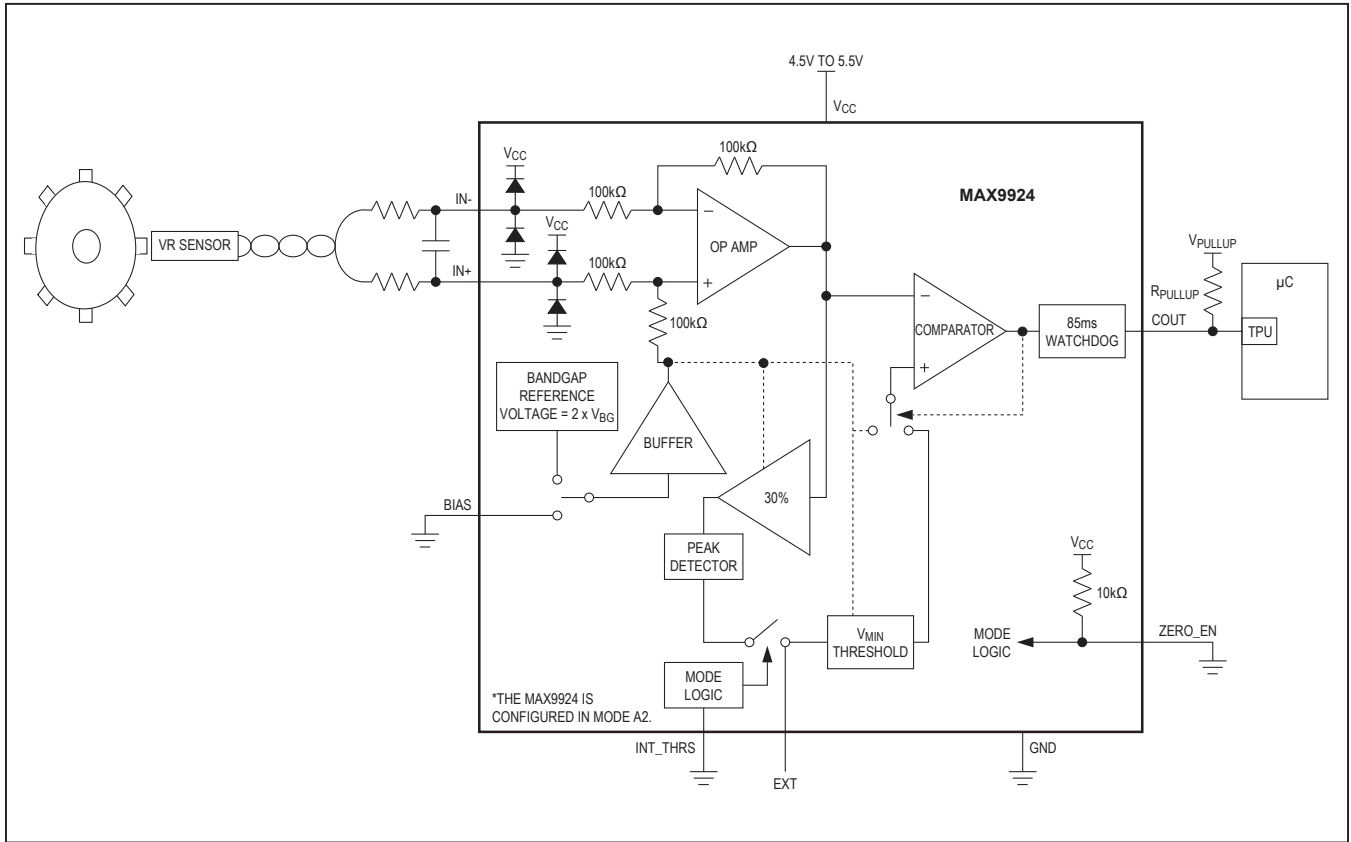
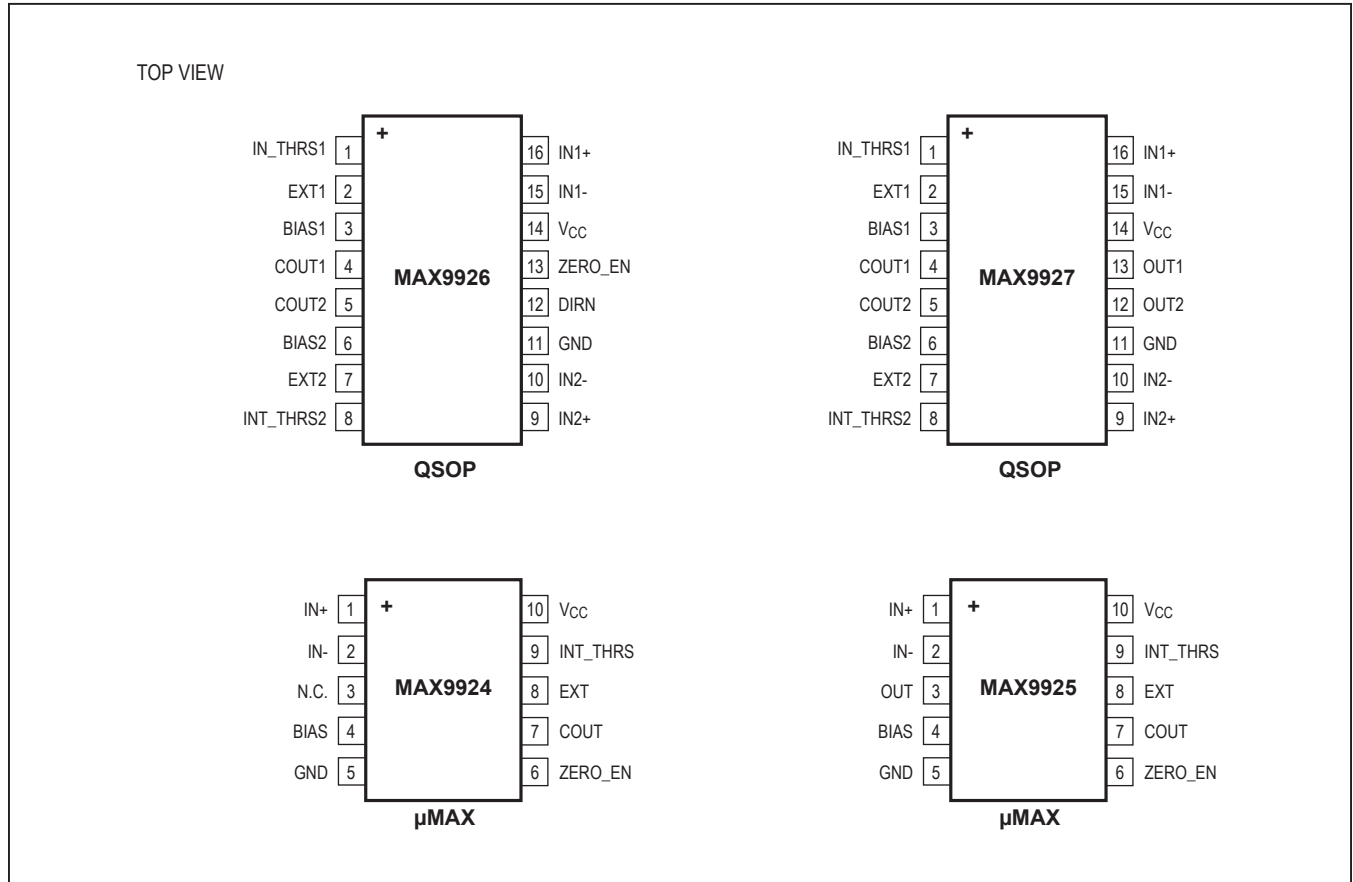


Figure 8. MAX9925 Operating Mode C

Typical Operating Circuit



Pin Configurations



Selector Guide

PART	AMPLIFIER	GAIN
MAX9924UAUB	1 x Differential	1V/V
MAX9925AUB	1 x Operational	Externally Set
MAX9926UAEE	2 x Differential	1V/V
MAX9927AEE	2 x Operational	Externally Set

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 μ MAX	U10+2	21-0061	90-0330
16 QSOP	E16+1	21-0055	90-0167

The drawing includes four views: TOP VIEW, BOTTOM VIEW, FRONT VIEW, and SIDE VIEW. The TOP VIEW shows a square package with 10 pins on the top and bottom edges. Dimensions include pin pitch 'e', pin width 's', marking 'AAAA', a diameter of $\phi 0.50 \pm 0.1$, and a distance of 0.6 ± 0.1 from the pin 1 mark to the center of the diameter. The FRONT VIEW shows the package height 'A', pin height 'A2', and various widths 'D1', 'D2', and 'b'. The SIDE VIEW shows the package profile with dimensions 'E1', 'E2', 'L', 'L1', and 'c', and an angle α . A gage plane is indicated.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037	REF	0.940	REF
b	0.007	0.0106	0.177	0.270
e	0.0197	BSC	0.500	BSC
c	0.0035	0.0078	0.090	0.200
S	0.0196	REF	0.498	REF
α	0°	6°	0°	6°

Pkg Codes: U10–2; U10CN–1

NOTES:
 1. D&E DO NOT INCLUDE MOLD FLASH.
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006”).
 3. CONTROLLING DIMENSION: MILLIMETERS.
 4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION BA.
 5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
 6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

TITLE:
PACKAGE OUTLINE, 10L μ MAX/ μ SOP

APPROVAL	DOCUMENT CONTROL NO. 21–0061	REV. L 1/1
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Package Information (continued)

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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

	INCHES		MILLIMETERS		N	PKG CODES
	MIN.	MAX.	MIN.	MAX.		
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2, E20-3
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PkFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE QSDP .150", .025" LEAD PITCH			
APPROVAL	DOCUMENT CONTROL NO. 21-0055	REV. J	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release	—
1	2/09	Removed future product references for the MAX9926 and MAX9927, updated EC table	1–4
2	3/09	Corrected various errors	2, 3, 4, 6, 13
3	3/11	Updated Figures 6, 7, and 8	17, 18
4	3/12	Added automotive qualifies parts	1
5	6/18	Added <i>Input Filter Considerations</i> section	14

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