OPERATION

All communications to and from the EconoRAM are accomplished via a single interface lead. EconoRAM data is read and written through the use of time slots. All data is preceded by a command byte to specify the type of transaction. **Once a specific transaction has been initiated, either a read or a write, it must be completed for all memory locations before another transaction can be started.**

1–WIRE SIGNALLING

The EconoRAM requires strict protocols to insure data integrity. The protocol consists of three types of signalling on one line: Write 0 time slot, Write 1 time slot and Read Data time slot. All these signals are initiated by the host.

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figures 1 through 3. All time slots are initiated by the host driving the data line low. The falling edge of the data line synchronizes the EconoRAM to the host by triggering a delay circuit in the EconoRAM. During write time slots, the delay circuit determines when the EconoRAM will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the EconoRAM will hold the data line low overriding the 1 generated by the host. If the data bit is a “1”, the EconoRAM will leave the read data time slot unchanged.

COMMAND BYTE

The command byte to specify the type of transaction is transmitted LSB first from the host to the EconoRAM using write time slots. The first bit of the command byte (see Figure 4) is a logic 1. This indicates to the EconoRAM that a command byte is being written. The next two bits are the select bits which denote the physical address of the EconoRAM that is to be accessed (set to 00 currently). The remaining five bits determine whether a read or a write operation is to follow. If a write operation is to be performed, all five bits are set to a logic 1 level. If a read operation is to be performed, any or all of these bits are set to a logic 0 level. All eight bits of the command byte are transmitted to the EconoRAM with a separate time slot for each bit.

READ OR WRITE TRANSACTION

Read or write transactions are performed by initializing the EconoRAM to a known state, issuing a command byte, and then generating the time slots to either read EconoRAM contents or write new data. Each transaction consists of 264 time slots. Eight time slots transmit the command byte, the remaining 256 time slots transfer the data bits. (See Figure 5.) Once a transaction is started, it must be completed before a new transaction can begin.

To initially set the EconoRAM into a known state, 264 Write Zero time slots must be sent by the host. These Write Zero time slots will not corrupt the data in the EconoRAM since a command byte has not been written. This operation will increment the address pointer internal to the EconoRAM to its maximum count value. Upon reaching this maximum value, the EconoRAM will ignore all additional Write Zero time slots issued to it and the internal address pointer will remain locked at the top count value. This condition is removed by the reception of a Write One time slot, typically the first bit of a command byte.

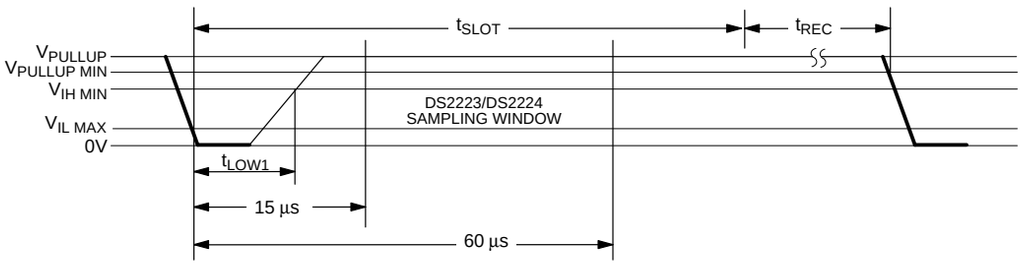
Once the EconoRAM has been set into a known state, the command byte is transmitted to the EconoRAM with eight write time slots. This resets the address pointer internal to the EconoRAM and prepares it for the appropriate operation, either a read or a write.

After the command byte has been received by the EconoRAM, the host controls the transfer of data. In the case of a read transaction, the host issues 256 read time slots. In the case of a write transaction, the host issues 256 write time slots according to the data to be written. All data is read and written least significant bit first.

Although the DS2224 has the first 32 bits replaced by lasered ROM rather than SRAM, it requires 256 write time slots for a complete write transaction. The data being sent during the first 32 write time slots has no effect on the DS2224 other than advancing the internal address pointer. As stated previously, it is not possible to change from read to write or vice versa before a transaction is completed.

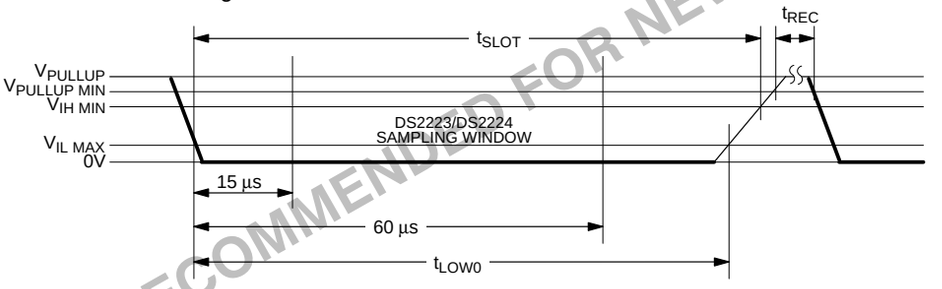
READ/WRITE TIMING DIAGRAM

Write–One Time Slot Figure 1



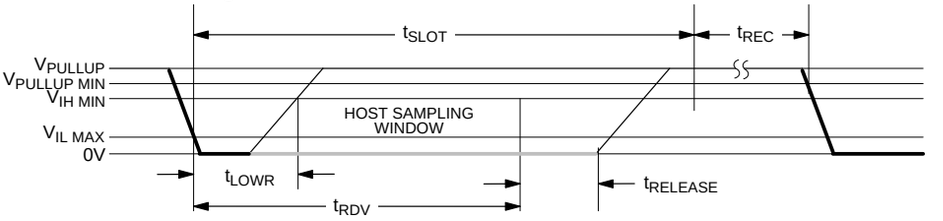
$60\ \mu s \le t_{SLOT} < \infty$
$1\ \mu s \le t_{LOW1} < 15\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

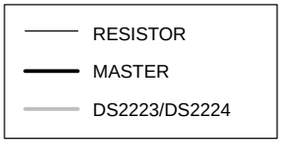
Write–Zero Time Slot Figure 2



$60\ \mu s \le t_{LOW0} < t_{SLOT} < \infty$
$1\ \mu s \le t_{REC} < \infty$

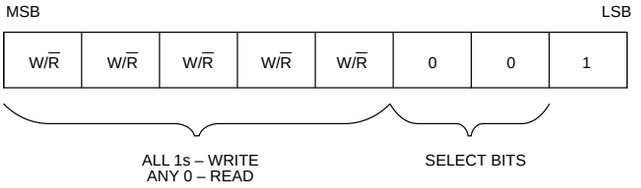
Read–Data Time Slot Figure 3



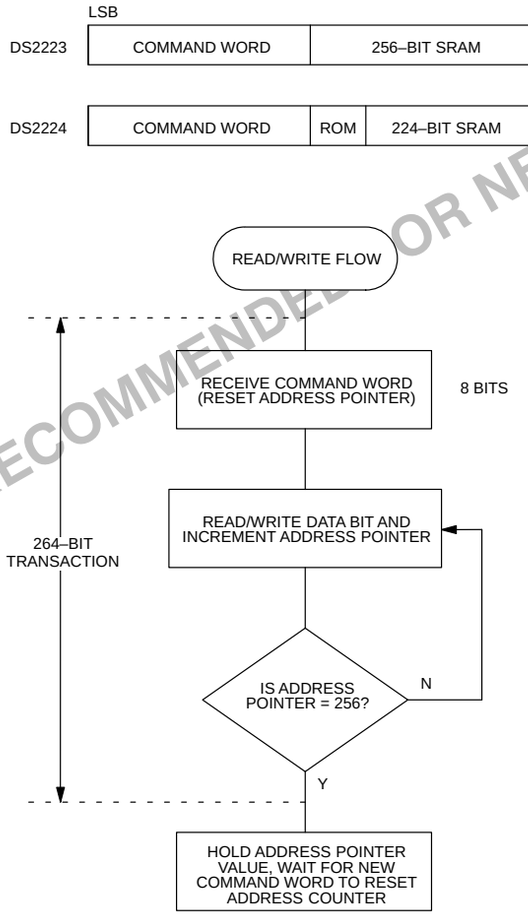


$60\ \mu s \le t_{SLOT} < \infty$
$1\ \mu s \le t_{LOWR} < 15\ \mu s$
$0 \le t_{RELEASE} < 45\ \mu s$
$1\ \mu s \le t_{REC} < \infty$
$t_{RDV} = 15\ \mu s$

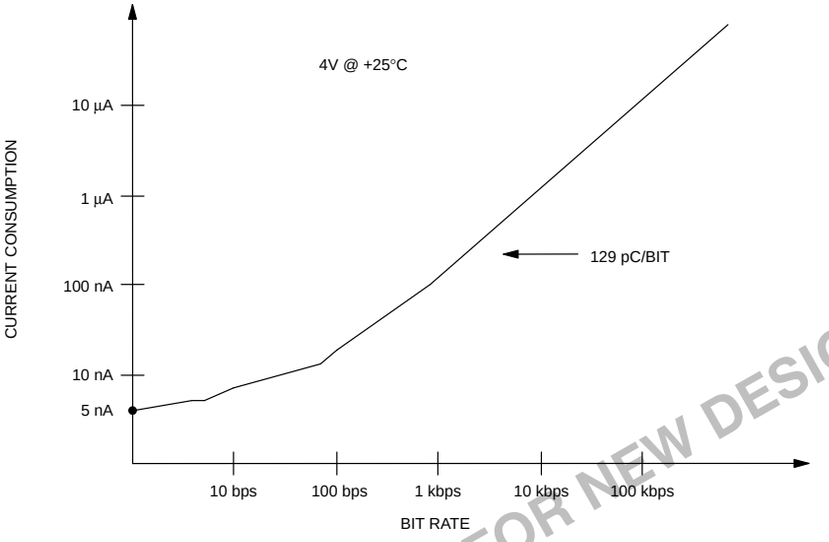
COMMAND WORD Figure 4



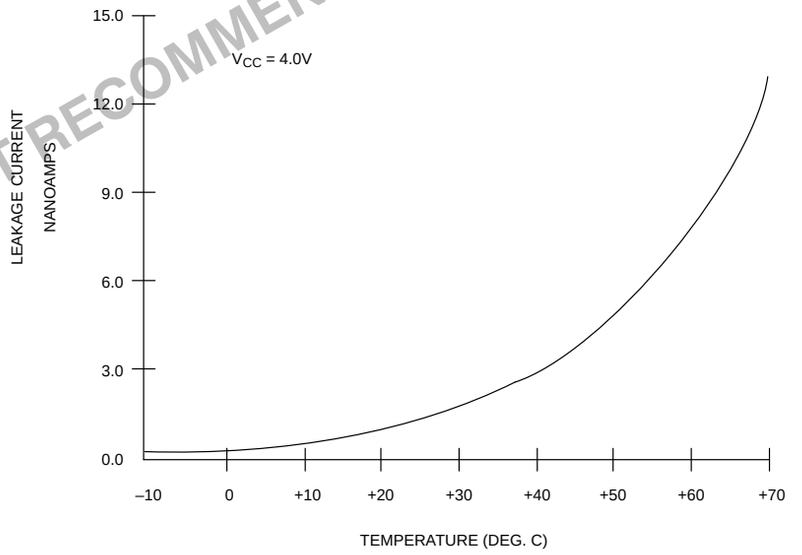
READ/WRITE TRANSACTION Figure 5



TYPICAL CURRENT CONSUMPTION VS. BIT RATE Figure 6



TYPICAL LEAKAGE CURRENT VS. TEMPERATURE Figure 7



1–WIRE INTERFACE

The 1–Wire interface has only a single line by definition; it is important that host and EconoRAM be able to drive it at the appropriate time. The EconoRAM is an open drain part with an internal circuit equivalent to that shown in Figure 8. The host can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together.

The 1–Wire interface requires a pull–up resistor with a value of approximately 5 kΩ to system V_{CC} on the data signal line. The EconoRAM has an internal open–drain driver with a 500 kΩ pull–down resistor to ground. The open–drain driver allows the EconoRAM to be powered by a small standby energy source, such as a single 1.5 volt alkaline battery, and still have the ability to produce CMOS/TTL output levels. The pull–down resistor holds the DQ pin at ground when the EconoRAM is not connected to the host.

APPLICATION EXAMPLES

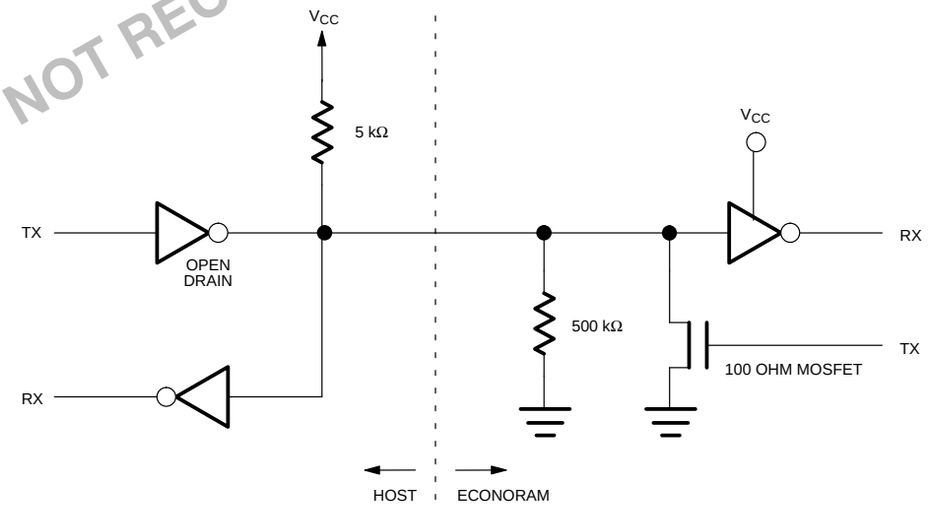
EconoRAMs are extremely conservative with power. Data can be retained in these small memories for as long as a month using the energy stored in a capacitor. Data is retained as long as the voltage on the V_{CC} pin of the EconoRAM (V_{CAP}) is at least 1.2 volts. A typical circuit is shown in Figure 9.

When V_{CC} is applied, capacitor C1 is charged and the EconoRAM receives power directly from V_{CC}. After power is removed, the diode CR1 prevents current from leaking back into the system, keeping the capacitor charged.

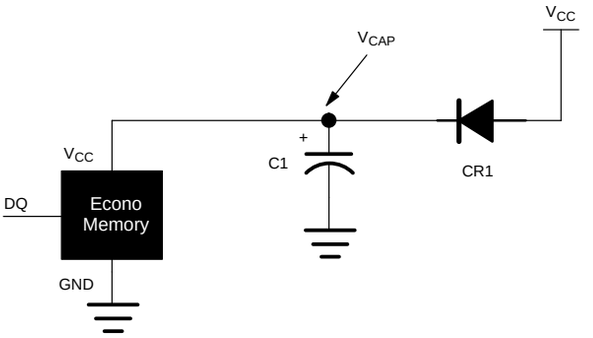
In the standby mode, the EconoRAM typically consumes only 12 nA at 25°C. However, the power–down process of the system can cause a slightly higher current drain. This is due to the fact that as system power ramps down, the signal attached to the DQ pin of the EconoRAM transitions slowly through the linear region, while the V_{CAP} voltage remains at its initial value. While in this region, the part draws more current as a function of the DQ pin voltage (see Figure 10).

The data retention time can be estimated with the aid of Figure 11. In this figure, the vertical axis represents the value of the capacitor C1; the horizontal axis is the data retention time in hours. The two curves represent initial V_{CAP} voltages of 3 and 5 volts. These curves are based on the assumption that the time the DQ pin is in the linear region is less than 100 ms.

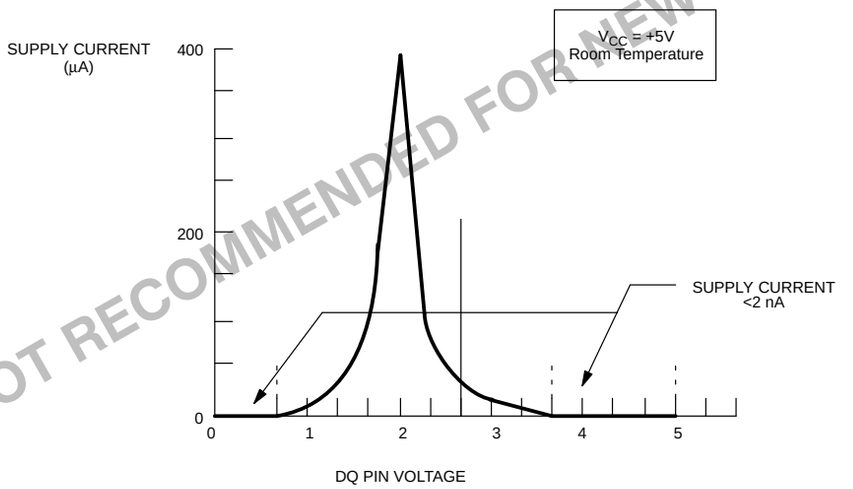
HOST TO ECONORAM INTERFACE Figure 8



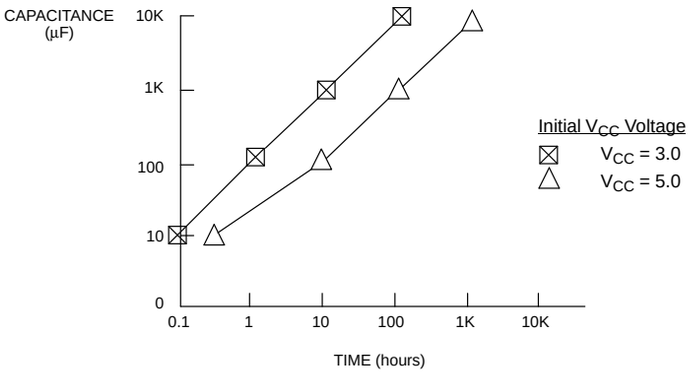
SUGGESTED CIRCUIT Figure 9



ICC VS. DQ VOLTAGE Figure 10

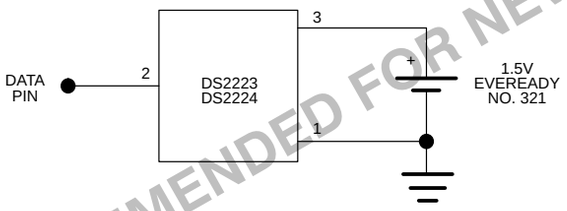


DATA RETENTION TIME VS. CAPACITANCE Figure 11



Using Battery Backup

14 mA–Hr => 144 million transactions



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +6.5V
Operating Temperature	–40°C to +85°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(–40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Pin	DQ	–0.5		6.0	V	1
Supply Voltage	V_{CC}	1.2		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=2.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	–0.5	0.4	0.8	V	1
Input Logic High	V_{IH}	V_{CC}–0.5		6.0	V	1
Sink Current	I_L	1	2		mA	4
Output Logic Low	V_{OL}			0.4	V	1
Output Logic High	V_{OH}	V_{PUP}		5.5	V	1, 2
Input Resistance	I_R		500		kΩ	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		2	25	nA	6

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC}=1.4V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Logic Low	V_{IL}	–0.5		0.2	V	1
Input Logic High	V_{IH}	1.0		6.0	V	1
Sink Current	I_L	1	2		mA	7
Output Logic Low	V_{OL}			0.4	V	4
Output Logic High	V_{OH}	V_{PUP}		5.5	V	1, 2
Input Resistance	I_R		500		kΩ	3
Operating Current	I_{OP}			36	nC	5
Standby Current	I_{STBY}		2	15	nA	6

AC ELECTRICAL CHARACTERISTICS (–40°C to +85°C; V_{CC}=1.4V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	70			µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60			µs	
Data Setup Time	t_{SU}			1	µs	8
Recovery Time	t_{REC}	1			µs	

AC ELECTRICAL CHARACTERISTICS (–40°C to +85°C; V_{CC}=2.0V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60			µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60			µs	
Data Setup Time	t_{SU}			1	µs	8
Recovery Time	t_{REC}	1			µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{PUP} = external pull–up voltage to system sypply.
3. Input pull–down resistance to ground.
4. @ V_{OL}=0.4V
5. 36 nanocoulombs per 264 time slots @ 1.5V (see Figure 6).
6. See Figure 7 for typical values over temperature.
7. @ V_{OL}=0.2V
8. Read data setup time refers to the time the host must pull the 1–Wire line low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum (15 µs total from falling edge on the 1–Wire line).

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