Block Diagram

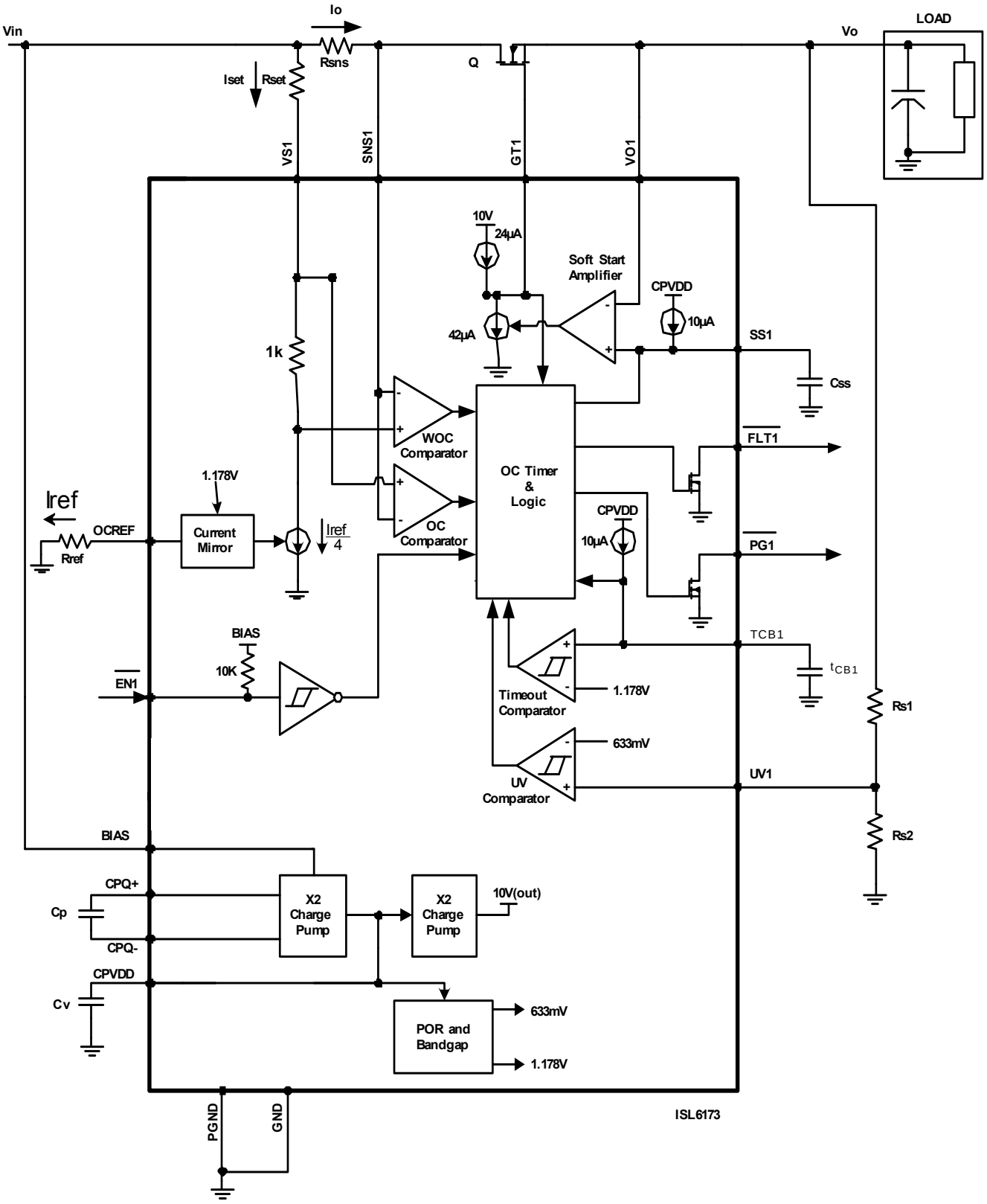
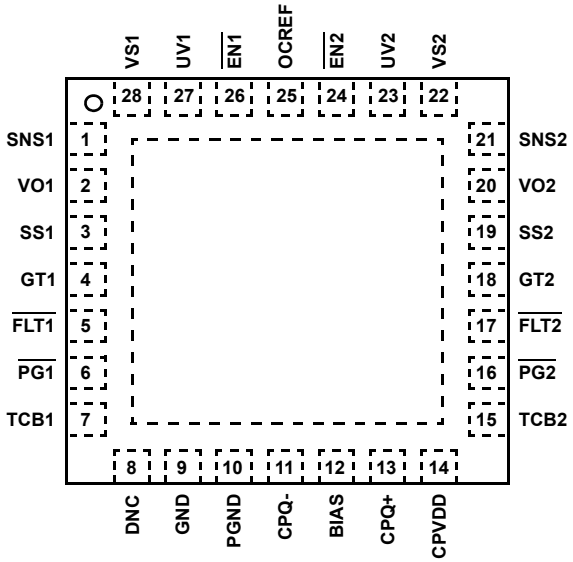


FIGURE 2. ISL6174 - INTERNAL BLOCK-DIAGRAM OF THE IC - CHANNEL ONE ONLY

Pinout

28 LEAD QFN
TOP VIEW



Pin Descriptions

PIN	NAME	FUNCTION	DESCRIPTION
1	SNS1	Current Sense Input	This pin is connected to the current sense resistor and control MOSFET Drain node. It provides current sense signal to the internal comparator in conjunction with VS1 pin.
2	VO1	Output Voltage 1	This pin is connected to the control MOSFET switch source, which connects to a load. Internally, this voltage is used for SS control.
3	SS1	Soft-Start Duration Set Input	A capacitor from this pin to ground sets the output soft-start ramp slope. This capacitor is charged by the internal 10µA current source setting the soft-start ramp. The output voltage ramp tracks the SS ramp by controlled enhancement of FET gate. Once ramp-up is completed, the capacitor continues to charge to the CPVDD voltage rail. If common capacitor is used (by tying SS1, SS2 together and the capacitor to GND from the connection) then both the outputs track each other as they ramp up.
4	GT1	Gate Drive Output	Direct connection to the gate of the external N-Channel MOSFET. At turn-on the Gate will charge to 4 X Vbias or 10V(max) from the 24µA source.
5	$\overline{FLT1}$	Fault Output	This is an open drain output. It asserts (pulls low) once the circuit breaker delay (determined by the TCB timeout cap) has expired. This output is valid for Vbias>1V.
6	$\overline{PG1}$	Power Good Output	This is an active low, open drain output. When asserted (logic zero), it indicates that the voltage on UV1 pin is more than 643mV (633mV + 10mV hysteresis). This output is valid at VBIAS >1V.
7	TCB1	Circuit Breaker Delay Timer	A capacitor from this pin to ground sets the delay from the onset of an over current event to channel shutdown (circuit breaker delay). Once the voltage on TCB cap reaches V_{CT_Vth} the GATE output is pulled down and the $\overline{FLT}$ is asserted. The time for circuit breaker delay (t_{CB}) = (C_{TCB}*1.178)/10µA.
8	DNC	Do not connect	Do not connect
9	GND	Chip Gnd	This pin is also internally shorted to the metal tab at the bottom of the IC.
10	PGND		Charge pump ground. Both GND and PGND must be tied together externally.
11	CPQ-	Charge Pump Capacitor Low Side	Flying cap lowside.

Pin Descriptions (Continued)

PIN	NAME	FUNCTION	DESCRIPTION
12	BIAS	Chip Bias Voltage	Provides IC Bias. Should be 2V to 4V for IC to function normally. This pin can be powered from a supply voltage that is not being controlled. It is preferable to use 3.3V even if the channels being controlled are 2.5V or lower because more gate drive voltage will be available to the MOSFETs.
13	CPQ+	Charge Pump Capacitor High Side	Flying cap highside. Use of 0.1µF for 2.5V bias and 0.022µF for 3.3V bias is recommended.
14	CPVDD	Charge Pump Output	This is the voltage used for some internal pull-ups and bias. Use of 0.47µF (minimum) is recommended.
15	TCB2	Timer Capacitor	Same function as pin 7
16	$\overline{PG2}$	Power Good Output	Same function as pin 6
17	$\overline{FLT2}$	Fault Output	Same as pin 5
18	GT2	Gate Drive Output	Same as pin 4
19	SS2	Soft-Start Duration Set Input	Same as pin 3
20	VO2	Output Voltage 2	Same as pin 2
21	SNS2	Current Sense Input	Same as pin 1
22	VS2	Current Sense Reference	Voltage input for one of the two voltages. Provides a 20µA current source for the ISET series resistor which sets the voltage to which the sense resistor IR drop is compared.
23	UV2	Undervoltage Monitor Input	This pin is one of the two inputs to the undervoltage comparator. The other input is the 633mV reference. It is meant to sense the output voltage through a resistor divider. If the output voltage drops so that the voltage on the UV pin goes below 633mV, $\overline{PG2}$ is deasserted.
24	$\overline{EN2}$	Enable	This is an active low input. When asserted (pulled low), the SS and gate drive are released and the output voltage gets enabled. When deasserted (pulled high or left floating), the reverse happens.
25	OCREF	Ref. Current Adj.	Allows adjustment of the reference current through R_{SET} and the internal Circuit Breaker set resistor, thus setting the thresholds for CR, OC and WOC.
26	$\overline{EN1}$	Enable Input	Same as pin 24
27	UV1	Undervoltage Monitor Input	Same as pin 23
28	VS1	Current Sense Reference	Same as pin 22

Absolute Maximum Ratings

VBIAS . . . . . +5.5V
GTx, CPQ+ . . . . . -0.3V to +12V
ENx, SNSx, PGx, FLTx, VSx, TCBx, UVx,
SSx, CPQ-, CPVDD. . . . . -0.3V to 5.5VDC
Output Current . . . . . Short Circuit Protected

Thermal Information

Thermal Resistance (Typical, Notes 1, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5x5 QFN Package	42	12.5

Maximum Storage Temperature Range. . . . . -65°C to +150°C
For recommended soldering conditions, see Tech Brief TB389.
(QFN - Leads Only)
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

VBIAS / VIN1 Supply Voltage Range. . . . . +2.25V to +3.63V
Temperature Range (T_A) -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. All voltages are relative to GND, unless otherwise specified.
3. 1V (min) on the BIAS pin required for $\overline{FLT}$ to be valid.
4. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside..

Electrical Specifications

V_{DD} = 2.5V to +3.3V, V_S = 1V,T_A = T_J = -40°C to +85°C, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CIRCUIT BREAKER CONTROL						
ISET Current	I_{SET}	R_{OCREF} = 14.7kΩ	19	20	21	µA
Over Current Comparator Offset Voltage	Vio	V_{VS} - V_{SNS} with I_{OUT} = 0A	-1.25	-0.05	1.25	mV
Circuit Breaker Threshold Voltage	V_{CRVTH}	V_{VS} - V_{SNS} at $\overline{FLT}$ assertion, R_{ISET} = 1.0k, I_{SET} = 20µA		19.7		mV
TCB Threshold Voltage	V_{CT_Vth}	Peak Voltage	1.128	1.178	1.202	V
TCB Charging Current	I_{CT}		9	10	11	µA
TCB Default Delay	T_{CT}	TCB = Open		3		µs
GATE DRIVE						
GATE Response Time from WOC (Open)	pd_woc_open	GATE open 100mV of overdrive on the WOC comparator		3		ns
GATE Response Time from WOC (Loaded)	pd_woc_load	GATE = 1nF 100mV of overdrive on the WOC comparator		100		ns
GATE Turn-On Current	IGATE_on	GATE = 2V, V_{VS} = 2V, V_{SNS} = 2.1V	21	24	27	µA
GATE Turn-Off Current	IGATE_off	OC or WOC Turn-off Gate Current		100		mA
GATE Voltage	V_{GATE}	Bias = 2.5V (Figure 5, 6)	8.2	8.8	9.3	V
		2.1 < Bias < 2.5 (Figure 5, 6)		7		V
BIAS						
Supply Current	I_{BIAS}	V_{BIAS} = 3.3V	6	9.3	12	mA
POR Rising Threshold	VIN_POR_L2H		1.85	2.02	2.12	V
POR Falling Threshold	VIN_POR_H2L		1.80	1.98	2.10	V
POR Threshold Hysteresis	VIN_POR_HYS		5	33		mV

Electrical Specifications V_{DD} = 2.5V to +3.3V, V_S = 1V,T_A = T_J = -40°C to +85°C, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O						
Undervoltage Comparator Falling Threshold	V_{UV_VTHF}		620	635	650	mV
Undervoltage Comparator Hysteresis	V_{UV_HYST}		9	17	25	mV
$\overline{EN}$ Rising Threshold	PWR_Vth_R	V_{BIAS} = 2.5V	1.75	2.04	2.25	V
$\overline{EN}$ Falling Threshold	PWR_Vth_F	V_{BIAS} = 2.5V	0.97	1.11	1.20	V
$\overline{EN}$ Hysteresis	PWR_HYST	V_{BIAS} = 2.5V	600	905	1175	mV
$\overline{PG}$ Pull-Down Voltage	VOL_PG	I_{PG} = 8mA	0.05	0.15	0.3	V
$\overline{FLT}$ Pull-Down Voltage (Note 3)	VOL_FLT	I_{FLT} = 8mA	0.05	0.15	0.3	V
Soft-Start Charging Current	I_{SS}	VSS = 1V	9	10	11	µA
CHARGE PUMP						
CPVDD	V_CPVDD	V_{BIAS} = 3.3V	4.9	5.2	5.5	V
CPVDD	V_CPVDD	V_{BIAS} = 3.3V T = +25°C External User Load = 6mA		5.0		V

Typical Performance Curves (at +25°C unless otherwise specified)

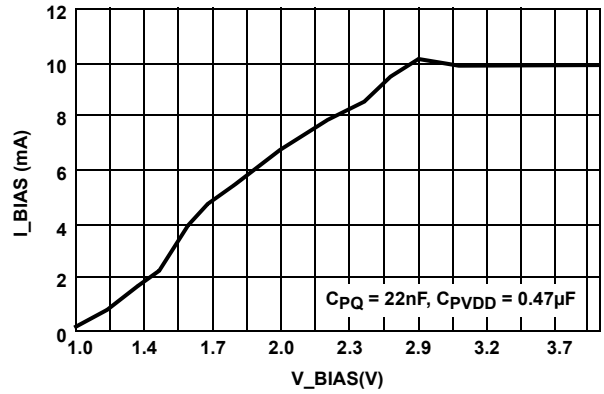


FIGURE 3. I_BIAS vs V_BIAS

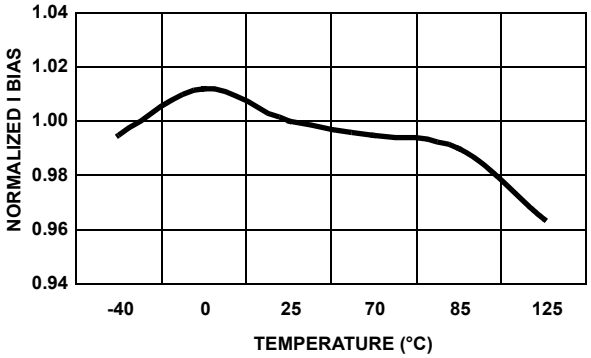


FIGURE 4. NORMALIZED I BIAS (VBIAS = 3.3V) vs TEMPERATURE

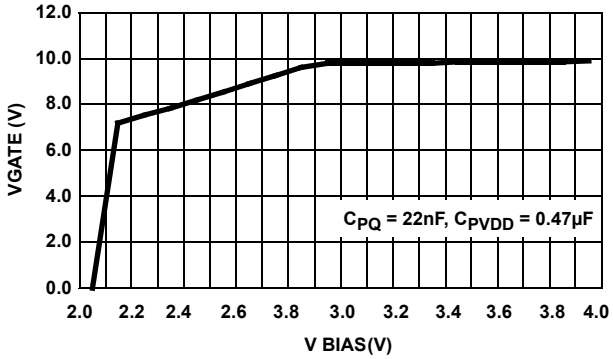


FIGURE 5. V_{GATE} vs V_BIAS

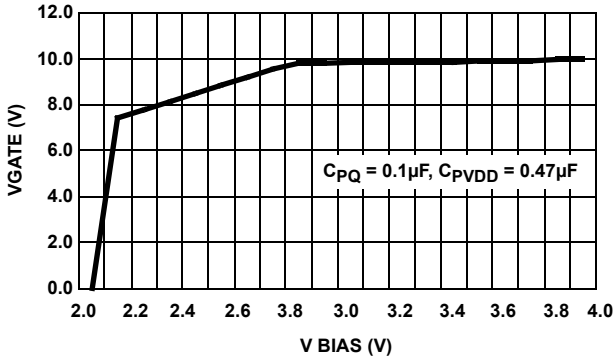


FIGURE 6. V_{GATE} vs V_BIAS

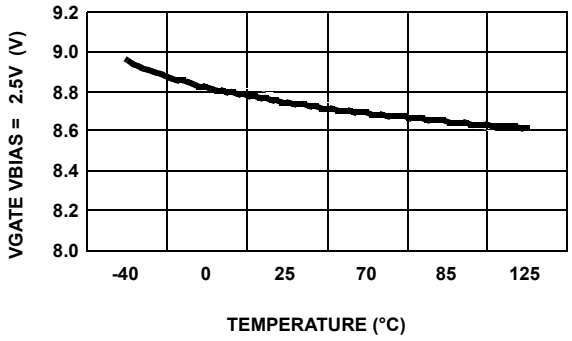


FIGURE 7. GATE VOLTAGE vs TEMPERATURE

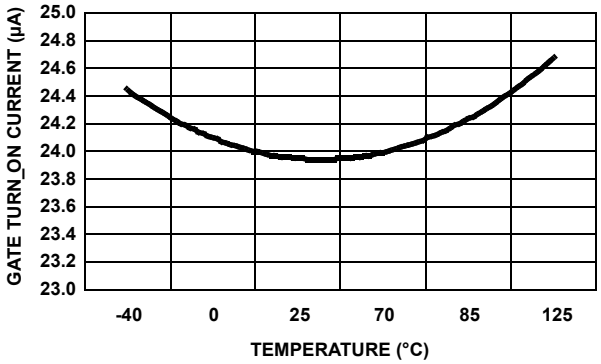


FIGURE 8. GATE TURN-ON CURRENT vs TEMPERATURE

Typical Performance Curves (at +25°C unless otherwise specified) **(Continued)**

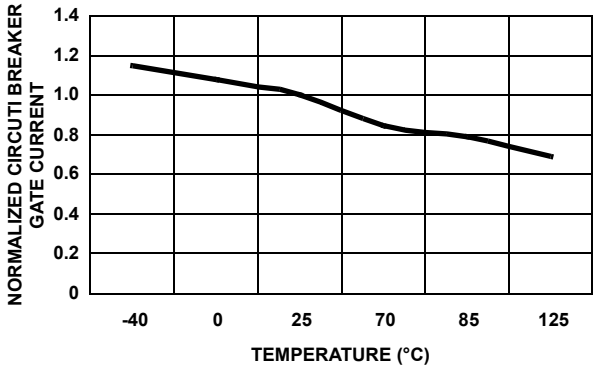


FIGURE 9. CIRCUIT BREAKER GATE TURN-OFF CURRENT vs TEMPERATURE

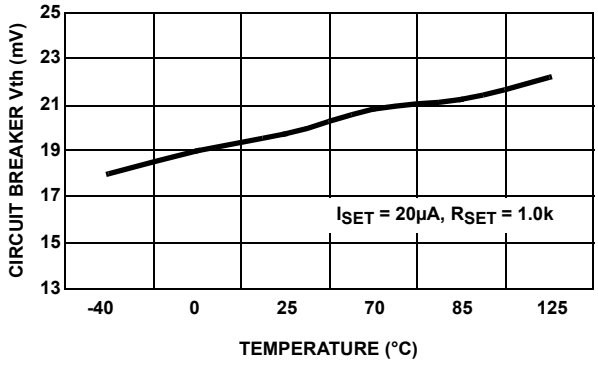


FIGURE 10. CIRCUIT BREAKER Vth vs TEMPERATURE

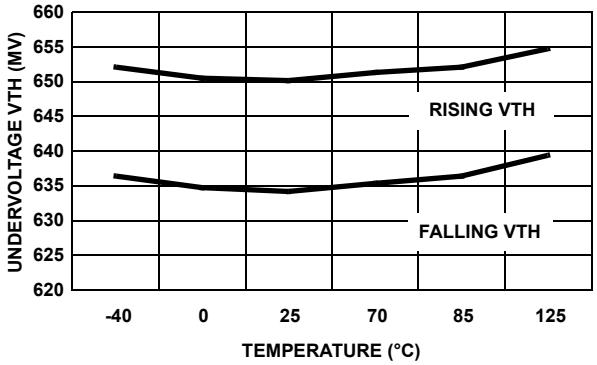


FIGURE 11. UNDERVOLTAGE Vth vs TEMPERATURE

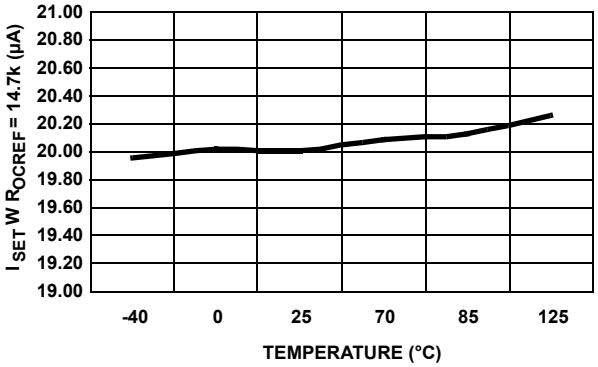


FIGURE 12. I_{SET} vs TEMPERATURE

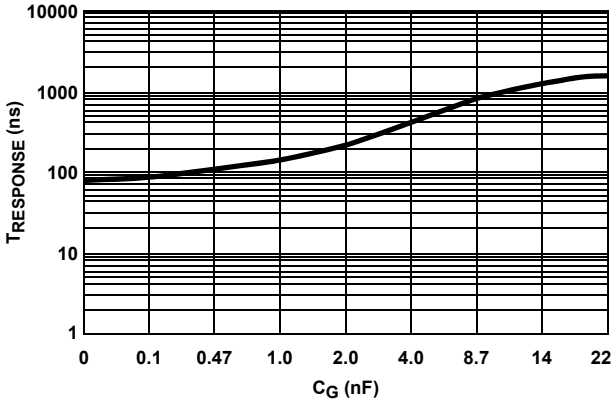


FIGURE 13. WOC RESPONSE vs LOAD CAPACITANCE

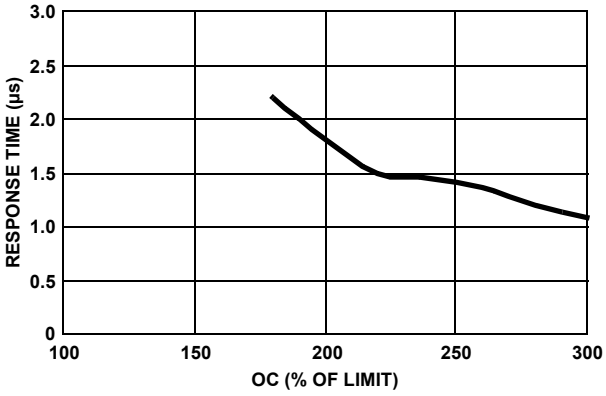


FIGURE 14. RESPONSE TIME vs I_O*R_{SNS}

Detailed Description of Operation

ISL6174 targets dual voltage hot-swap applications with a bias of 2.1V to 3.6VDC and the voltages being controlled down to 0.7VDC. The IC's main functions are to control start-up inrush current and provide circuit breaker protection of the sourcing supplies from OC loads. This is achieved by enhancing an external MOSFET in a controlled manner. In order to fully enhance the MOSFET, the IC must provide adequate gate to source voltage, which is typically 5V or greater. Hence, the final steady-state voltage on Gate (GT) pin must be a minimum of 5V above the load voltage. Two internal charge-pumps allow this to happen.

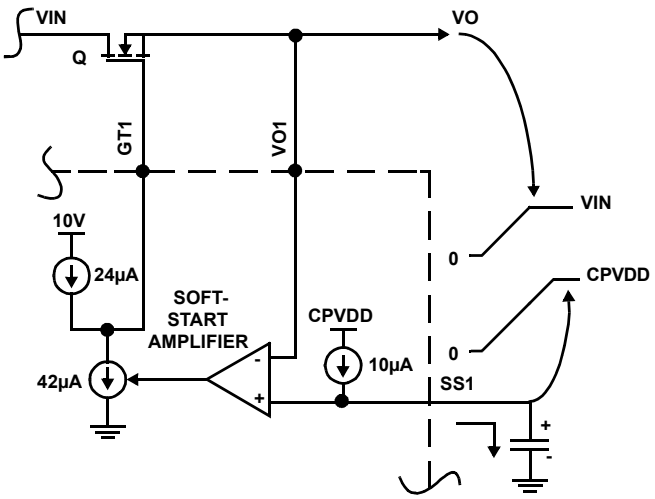


FIGURE 15. SOFT-START OPERATION

Controlled Soft-Start

The output voltages are monitored through the Vo pins and slew up at a rate determined by the capacitors on the Soft-start (SS) pin, as illustrated in Figure 15. 24µA of gate charge current is available. The soft-start amplifier controls the output voltage by robbing some of the gate charge current thus slowing down the MOSFET enhancement. When the load voltage reaches its set level, as sensed by its respective UV pin through an external resistor divider, the Power Good ($\overline{PG}$) output goes active.

Current Monitoring and Circuit Breaker Protection

The IC monitors the load current (Io) by sensing the voltage-drop across the low value current sense resistor (R_{SNS}), which is connected in series with the MOSFET (as shown in the "Block Diagram" on page 2), through Sense (SNS) and voltage set (VS) pins. The latter is through a resistor, R_{SET}, as shown. Two levels of overcurrent detection are available to protect against all possible fault scenarios. These levels are:

- Timed Circuit Breaker (CB)
- Way Overcurrent Circuit Breaker (WOC)

Each of these modes is described in detail as follows:

TIMED CIRCUIT BREAKER (CB) MODE

When the load current reaches the Circuit Breaker threshold (I_{CB}) the ISL6174 enters the timed Circuit Breaker Mode. When the circuit enters this mode, the OC comparator which directly looks at the voltage drop across R_{SNS} detects it and starts the CB delay timer. TCB begins to charge whatever capacitance is on that pin from an internal 10µA current source. The amount of time it takes for this capacitance to charge to ~1.18V (V_{CT_Vth}) sets up the Circuit Breaker delay. Upon expiration of the CB delay (t_{CB}), the MOSFET gate is pulled down quickly.

If during and prior to t_{CB} expiring the load current falls below I_{CB} then in that case, the Circuit Breaker mode is no longer active and the IC discharges the C_{TCB} cap.

The Circuit Breaker threshold (I_{CB}) is set by sinking a reference current, I_{SET}, through R_{SET} by selecting an appropriate resistor between OCREF and GND, which sets I_{REF}. The relationship between I_{REF} and I_{SET} is $I_{REF} = 4*I_{SET}$, where I_{REF} = Vocref/Rocref = 1.178/Rocref. I_{REF} would typically be set at 80µA. This $I_{SET} * R_{SET}$ voltage is then compared to the voltage across a load current series sense low ohmic resistor.

Selecting appropriate values for R_{SET} and R_{SNS} such that when $I_O = I_{CR}$,

$$Io*R_{SNS} = I_{SET}*R_{SET} \quad \text{(EQ. 1)}$$

WAY OVERCURRENT CIRCUIT BREAKER (WOC) MODE

This mode is designed to handle very fast, very low impedance shorts on the load side, which can result in very high di/dt transients on the input current. The WOC circuit breaker level is typically 200% of the Circuit Breaker limit. In this mode the comparator, which directly looks at the voltage drop across R_{SNS} and once the WOC level is exceeded the IC pulls the gate very quickly to GND, the SSx capacitor is discharged, $\overline{FLT}$ is asserted and a new SS sequence is allowed to begin after $\overline{ENx}$ recycle.

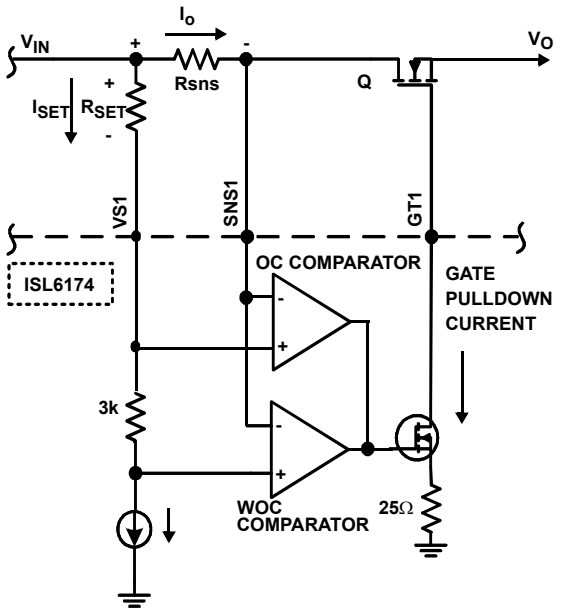


FIGURE 16. OC / WOC OPERATION

Bias and Charge Pump Voltages:

The BIAS pin feeds the chip bias voltage directly to the first of the two internal charge pumps, which are cascaded. The output of the first charge pump, in addition to feeding the second charge pump, is accessible on the CPVDD pin. The voltage on the CPVDD pin is approximately 5V. It also provides power to the POR and band-gap circuitry as shown in the block diagram. A capacitor connected externally across CPQ+ and CPQ- pins of the IC is the “flying” cap for the charge-pump.

The second charge-pump is used exclusively to drive the gates of the MOSFETs during soft start through the 24µA current sources, one for each channel. The output of this charge pump is approximately 10V as shown in the “Block Diagram” on page 2.

Typical Hot-plug Power Up Sequence

1. When power is applied to the IC on the BIAS pin, the first charge pump immediately powers up.
2. If the BIAS voltage is 2.1V or higher, the IC comes out of POR. Both SS and TCB caps remain discharged and the gate (GT) voltage remains low.
3. $\overline{\text{ENx}}$ pin, when pulled below it’s specified threshold, enables the respective channel.
4. SSx cap begins to charge up through the internal 10µA current source, the gate (GT) voltage begins to rise and the corresponding output voltage begins to rise at the same rate as the SS cap voltage. This is tightly controlled by the soft-start amplifier shown in the block diagram.
5. SS cap begins to charge but the corresponding TCBx cap is held discharged.
6. Fault ($\overline{\text{FLT}}$) remains deasserted (stays high) and the output voltage continues to rise.
7. If the load current on the output exceeds the set current limit for greater than the circuit breaker delay, $\overline{\text{FLT}}$ gets asserted and the channel shutdown occurs.
8. If the voltage on UV pin exceeds 633mV threshold as a result of rising Vo, the Power Good ($\overline{\text{PG}}$) output goes active.
9. At the end of the SS interval, the SS cap voltage reaches CPVDD and remains charged as long as $\overline{\text{EN}}$ remains asserted or there is no other fault condition present that would attempt to pull down the gate.

Applications Information

Selection of External Components

The typical application circuit of Figure 2 has been used for this section, which provides guidelines to select the external component values.

MOSFET (Q1)

This component should be selected on the basis of its $r_{DS(ON)}$ specification at the expected Vgs (gate to source voltage) and the effective input gate capacitance (Ciss). One needs to ensure that the combined voltage drop across the Rsense and $r_{DS(ON)}$ at the desired maximum current (including transients) will still keep the output voltage above the minimum required level.

Ciss of the MOSFET influences the overcurrent response time. It is recommended that a MOSFET with Ciss of less than 10nF be chosen. Ciss will also have an impact on the SS cap value selection as seen later.

Current Sense Resistor (R_{SNS})

The voltage drop across this resistor, which represents the load current (Io), is compared against the set threshold of the Circuit Breaker comparator. The value of this resistor is determined by how much combined voltage drop is tolerable between the source and the load. It is recommended that at least 20mV drop be allowed across this resistor at max load current. This resistor is expected to carry maximum full load current indefinitely. Hence, the power rating of this resistor must be greater than $I_{O(MAX)}^2 * R_{SNS}$.

This resistor is typically a low value resistor and hence the voltage signal appearing across it is also small. In order to maintain high current sense accuracy, current sense trace routing is critical. It is recommended that either a four wire resistor or the routing method as shown in Figure 17 be used.

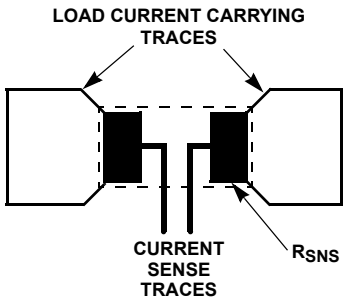


FIGURE 17. RECOMMENDED CURRENT SENSE RESISTOR PCB LAYOUT

Current Set Resistor (R_{SET})

This resistor sets the threshold for the Circuit Breaker comparator in conjunction with R_{SNS}. Once R_{SNS} has been selected, use Equation 1 to calculate R_{SET}. Use 20µA for I_{SET} in a typical application.

Reference Current Set Resistor (R_{REF})

This resistor sets up the current in the internal current source, $I_{REF}/4$, shown in Figure 2 for the comparators. The voltage at the OCREF pin is the same as the internal bandgap reference. The current (I_{REF}) flowing through this resistor is simply:

$I_{REF} = 1.178/R_{REF}$

This current, I_{REF}, should be set at 80µA to force 20µA in the internal current source as shown in Figure 2, because of the 4:1 current mirror. This equates to the resistor value of 14.7k.

Selection of Rs1 and Rs2

These resistors set the UV detect point. The UV comparator detects the undervoltage condition when it sees the voltage at UV pin drop below 0.633V. The resistor divider values should be selected accordingly.

Charge Pump Capacitor Selection (C_P and C_V)

C_P is the “flying cap” and C_V is the smoothing cap of the charge pump, which operates at 450kHz set internally. The output resistance of the charge pump, which affects the regulation, is dependent on the C_P value and its ESR, charge-pump switch resistance, and the frequency and ESR of the smoothing cap, C_V.

It is recommended that C_P be kept within 0.022µF (minimum) to 0.1µF (maximum) range. Only ceramic capacitors are recommended. Use 0.1µF cap if CPVDD output is expected to power an external circuit, in which case the current draw from CPVDD must be kept below 10mA.

C_V should at least be 0.47µF (ceramic only). Higher values may be used if low ripple performance is desired.

Time-out Capacitor Selection (C_T)

This capacitor determines the current regulation delay period. As shown in Figure 2, when the voltage across this capacitor exceeds 1.178V, the time-out comparator detects it and the gate voltage is pulled to 0V thus shutting down the channel. An internal 10µA current source charges this capacitor. Hence, the value of this capacitor is determined by Equation 2.

$$C_T = (10\mu A \bullet T_{OUT})/1.178 \quad \text{(EQ. 2)}$$

Where,

T_{OUT} = Desired time-out period.

Soft-Start Capacitor Selection (C_{SS})

The rate of change of voltage (dv/dt) on this capacitor, which is determined by the internal 10µA current source, is the same as that on the output load capacitance. Hence, the value of this capacitor directly controls the inrush current amplitude during hot swap operation.

$$C_{SS} = C_O \bullet (10\mu A/I_{INRUSH}) \quad \text{(EQ. 3)}$$

Where,

C_O = Load Capacitance

I_{INRUSH} = Desired Inrush Current

I_{INRUSH} is the sum of the DC steady-state load current and the load capacitance charging current. If the DC steady-state load remains disabled until after the soft-start period expires ($\overline{PGx}$ could be used as a load enable signal, for example), then only the capacitor charging current should be used as I_{INRUSH}. The Css value should always be more than (1/2.4) of that of Ciss of the MOSFET to ensure proper soft-start operation. This is because the Ciss is charged from 24µA current source, whereas the Css gets charged from a 10µA current source (Figure 15). In order to make sure both V_{SS} and V_O track during the soft-start, this condition is necessary.

ISL6174 Evaluation Platform

The **ISL617XEVAL1Z** is the primary evaluation board for this IC. For the BOM, schematic and photograph, see the “BOM for ISL617XEVAL1Z Board and Schematic” on page 15.

The evaluation board has been designed with a typical application in mind and with accessibility to all the featured pins to enable a user to understand and verify these features of the IC. The two circuit breaker levels are programmed to 2.2A for each input rail but they can easily be scaled up or down by adjusting some component values.

There are two input voltages, one for each channel that are switched by a dual N-Channel MOSFET (Q1) to the output connectors.

Pins SS1 and SS2 of the IC are available as jumper test points so that they can be tied together to achieve concurrent tracking between Vo1 and Vo2. Both the $\overline{EN}$ inputs must be turned on together to check this function, jumpers are provide to facilitate this.

Each channel is preloaded with the resistive load that makes up the UV threshold level. Additional loading can be externally applied as desired.

The internal Circuit Breaker amplifier is fast enough to respond to very fast di/dt events.

On this board, the timeout capacitor value for side ‘1’ is 0.15µF, which corresponds to a timeout period of 17.67ms.

The scope shots are taken from the ISL6174EVAL1 to demonstrate the ISL6174s critical operational waveforms.

Figure 18 illustrates the circuit breaker operation which will be evident with a slow ramping output current at the programmed 2.2A level, I_{CB}. This mode of operation will be invoked while the OC event is < ~2X the I_{CB}. as shown in Figure 19. Characteristic of this operational mode is the TCB pin ramping to V_{CB} to establish the circuit breaker delay.

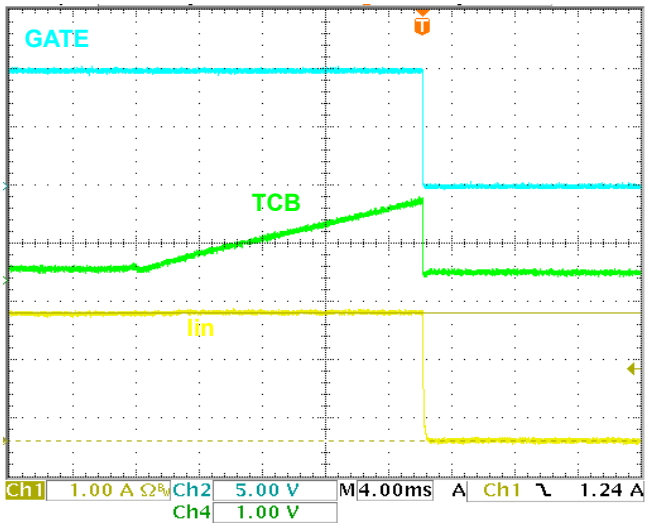


FIGURE 18. SLOW RAMPING TO 2.2A OC CIRCUIT BREAKER OPERATION

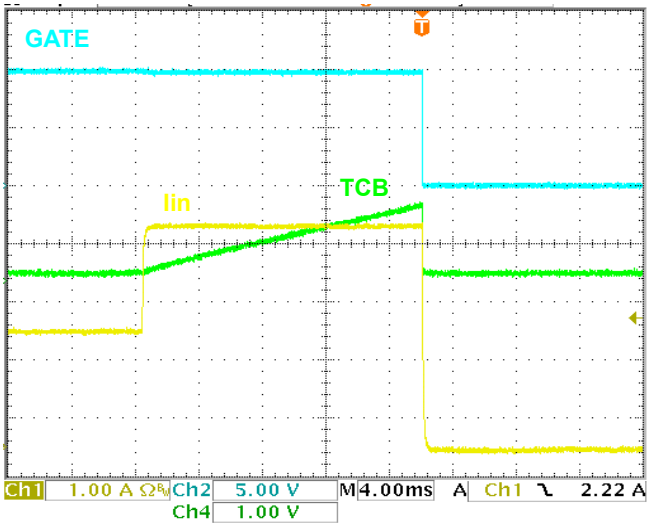


FIGURE 19. TRANSIENT TO 3.9A OC CIRCUIT BREAKER OPERATION

The way to confirm WOC mode, is by looking at the TCB pin waveform. If no ramping is seen prior to GATE turn off, then WOC is active. The following waveform in Figure 20 shows WOC operation:

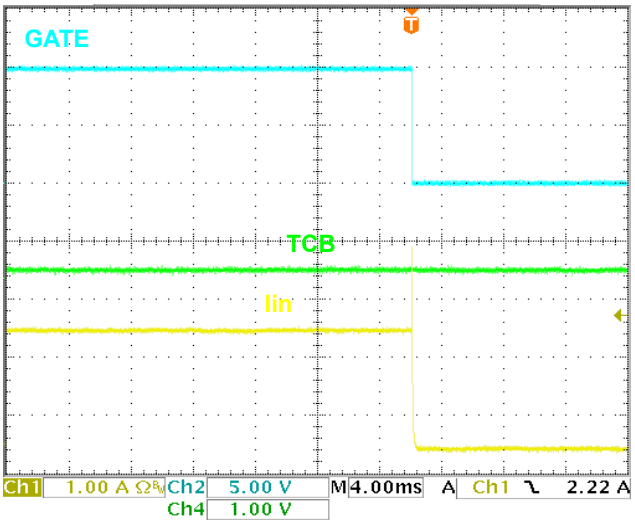


FIGURE 20. WOC CIRCUIT BREAKER OPERATION

Figure 21 is a 200X zoom of a WOC turn-off event and clearly illustrates the lack of any TCB ramping during this WOC event.

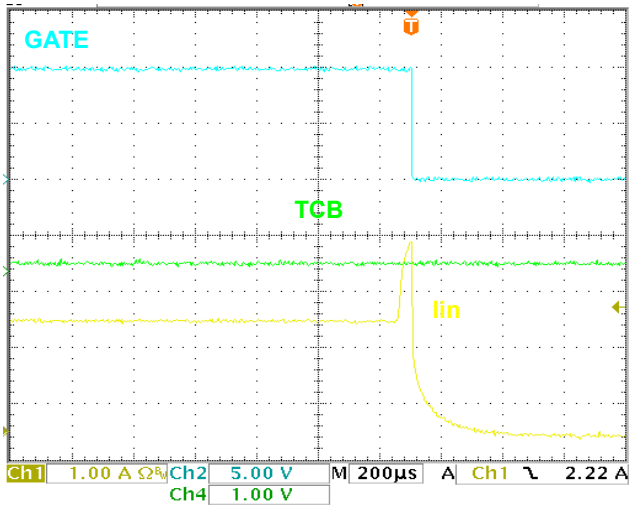


FIGURE 21. WOC CIRCUIT BREAKER OPERATION ZOOM

Figure 22 illustrates the GATE response time to an output short. The time from the input current > 2.2A (I_{CB}) to the FET gate being pulled down is ~0.6µs.

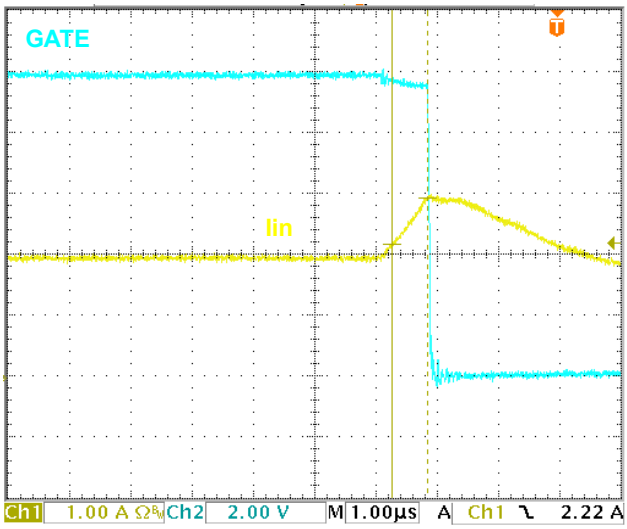


FIGURE 22. SHORTED OUTPUT GATE RESPONSE

The previous scope shots illustrate the performance with a ~18ms circuit breaker delay, t_{CB} as determined by the 10.5µF cap on TCB pin. Figure 23 shows the performance with an open TCB pin for the same amplitude of OC event as shown in Figure 19. Once again, see the TCB pin ramp duration and t_{CB} of ~3µs, the intrinsic delay of the IC OC response.

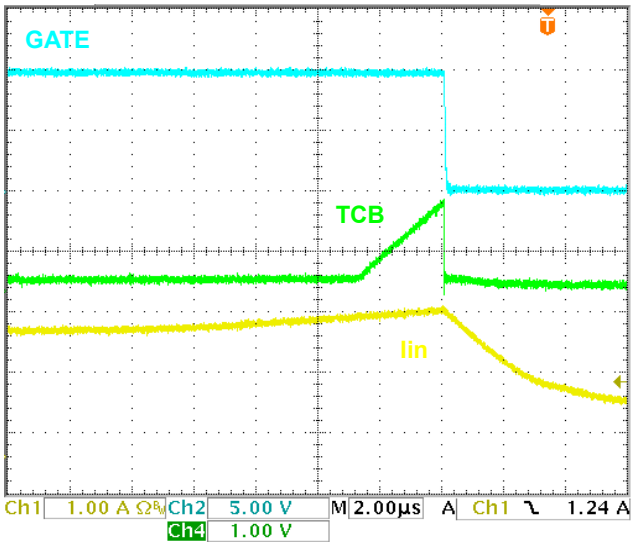


FIGURE 23. TRANSIENT TO 3.9A OC CIRCUIT BREAKER OPERATION with TCB OPEN

Dual Voltage Tracking During Turn-on

The ISL6174 Dual Circuit Breaker is also designed to provide either concurrent or ratiometric tracking of the two output voltages during turn-on. This capability is critical in providing power to many high value loads.

The two channels can be forced to track each other by simply tying their SS pins together and using a common SS capacitor, C_{SS}. In addition, their $\overline{EN}$ pins also must be tied together. Typical Start-up waveforms in this mode are shown in Figure 24, where the common C_{SS} value is 0.066µF.

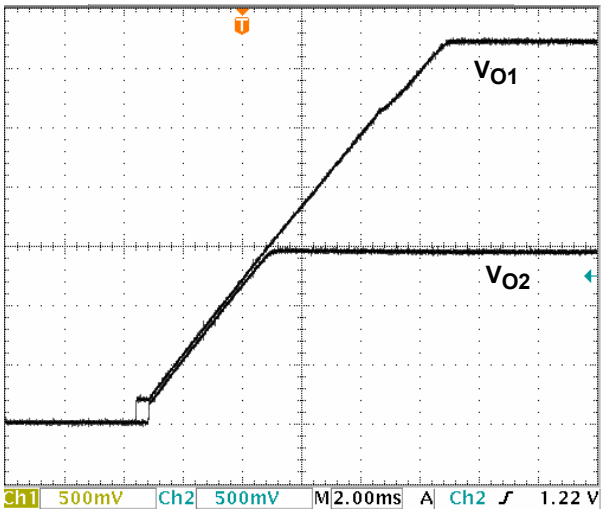


FIGURE 24. CONCURRENT TRACKING MODE

If one channel experiences a CB event and turns off, the other one will too.

To achieve ratiometric tracking, the ratio of the two C_{SS} must match the ratio of the two voltages being handled. In the illustrated case in Figure 25, the 1.5V to 3.3V ratio of 1:2.2 is

reflected in the choices of C_{SS} cap values of 0.033µF and 0.072µF. These cap values result in the performance demonstrated, the variance from a perfect match being the effect of variance in capacitor values, V_{SS} and I_{SS}.

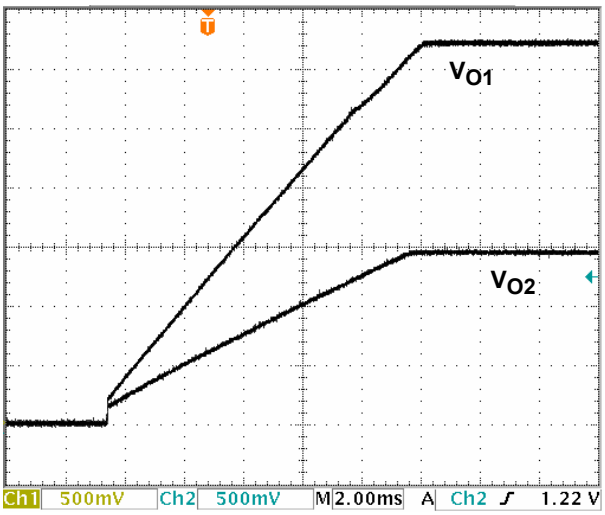
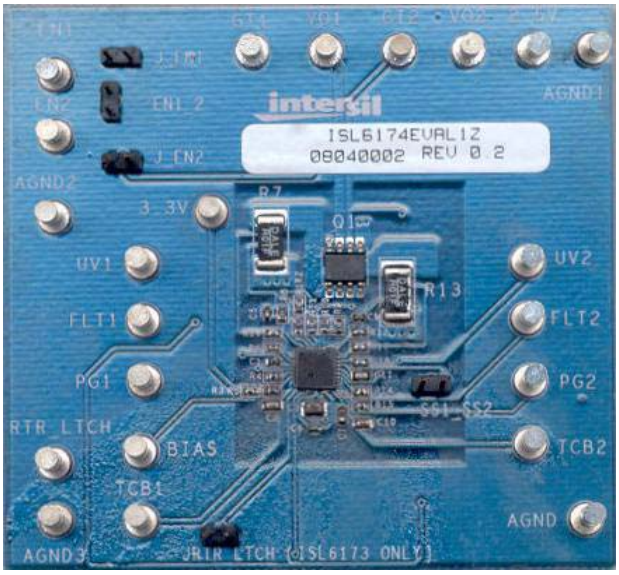


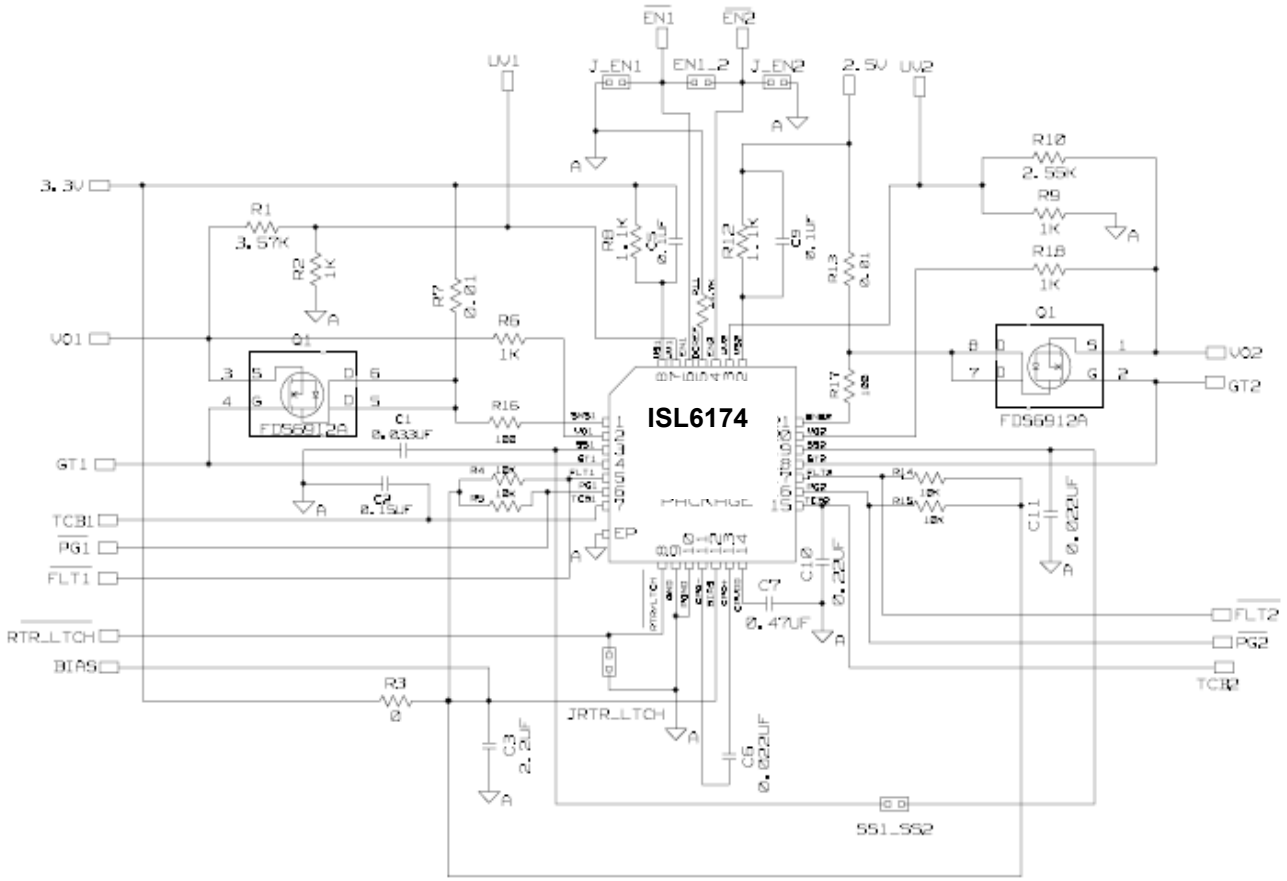
FIGURE 25. RATIOMETRIC TRACKING MODE

ISL617XEVAL1Z Photograph



BOM for ISL617XEVAL1Z Board and Schematic

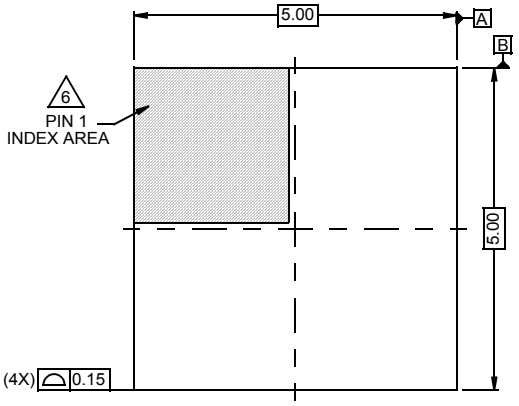
REFERENCE	PART	PKG	MFG P/N	MANUFACTURER
U1	Circuit Breaker IC	28 Ld 5X5 QFN	ISL6174DRZ	Intersil
Q1	FDS6912A	SO8	FDS6912A or equivalent	Various
C1	0.033µF	0402		Any
C2	0.15µF	0402		Any
C7	0.47µF			Any
C3	2.2µF			Any
C5, C9	0.1µF			Any
C6, C11	0.022µF	0402		Any
C10	0.22µF	0402		Any
R7, R13	0.01	2512		Any
R1	3.57k	0402		Any
R16	2.55k	0402		Any
R10	14.7k	0402		Any
R3	0	0402		Any
R4, R5, R14, R15	10k	0402		Any
R8, R12	1.1k	0402		Any
R2, R6, R17, R18	1k	0402		Any
J_EN1, EN1-2, J_EN2, JRTR_LTCH, SS1_SS2	Jumper	2 PIN, 0.1”		Any



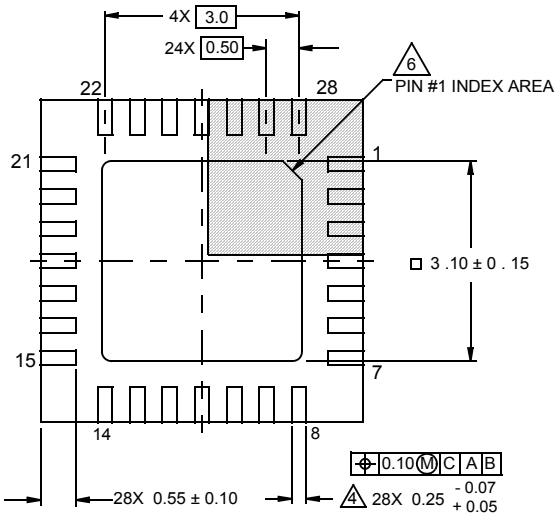
Package Outline Drawing

L28.5x5

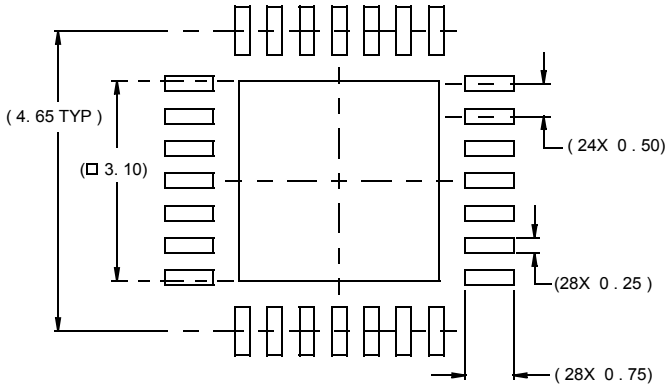
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/07



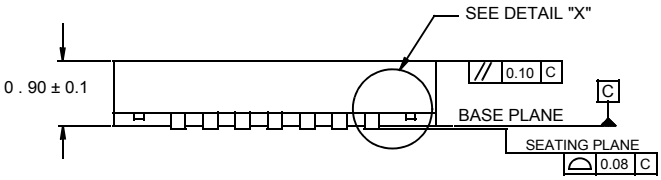
TOP VIEW



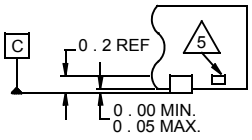
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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