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REVISION HISTORY

7/11—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

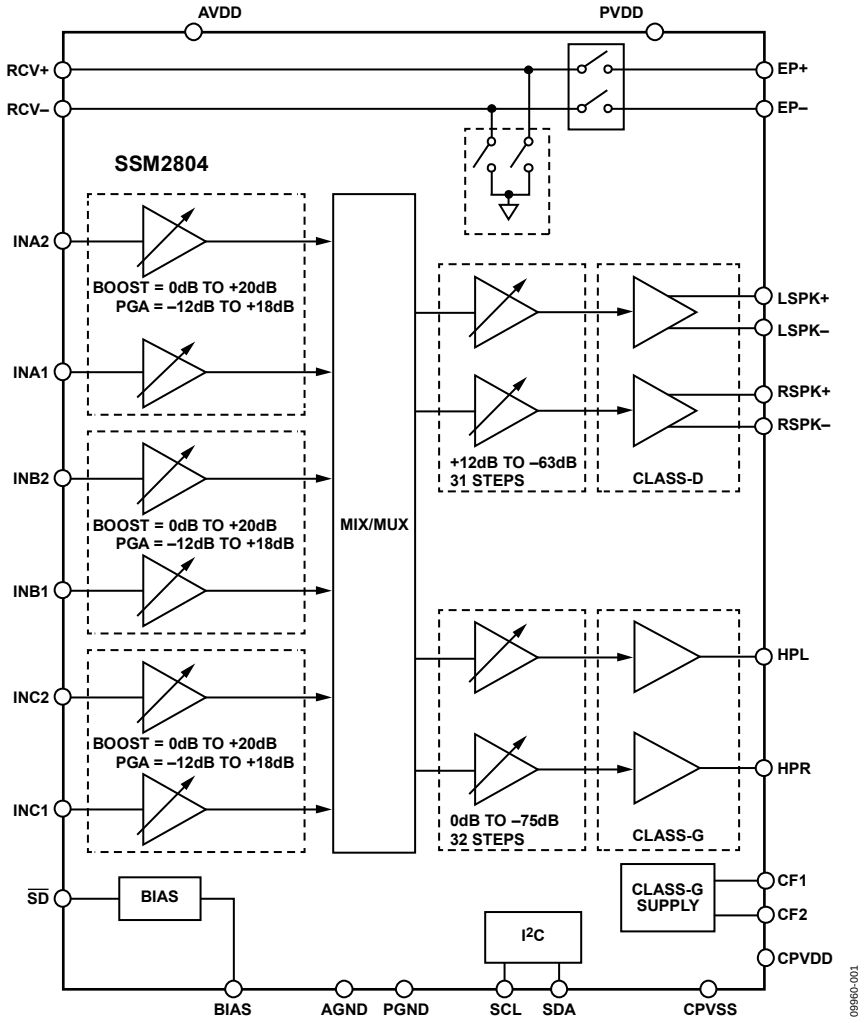

Figure 1.

SPECIFICATIONS

T_A = 25°C, AVDD = 3.3 V, PVDD = 3.6 V, gain = 0 dB, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
Analog Voltage Supply (AVDD)	2.5	3.3	3.6	V	
Speaker Voltage Supply (PVDD)	2.7	3.6	5.5	V	
Total Quiescent Current (I_{DD})		3.5		mA	HP mode only
		6.0		mA	Stereo Class-D mode only
		9.8		mA	HP and Class-D modes
		400		µA	Receiver path mode
Power-Down Current (I_{SD})		1		µA	$\overline{SD}$ pin low
INPUT CHARACTERISTICS					
Turn-On Time		10		ms	$\overline{SD}$ rising edge from AGND to AVDD
PGA Mode Operation					
Input Impedance	38	54		kΩ	Minimum gain setting
	4.5	6.5		kΩ	Maximum gain setting
Gain Range	−12		+18	dB	INAx, INBx, INCx inputs, 31 steps
Boost Mode Operation					
Input Impedance		20		kΩ	
Gain Range	0		20	dB	INAx, INBx, INCx inputs, 3 steps
CLASS-D AMPLIFIER					
Output Offset Voltage (V_{OS})		2.3		mV	Output muted
		12		mV	Output unmuted
Output Power (P_{OUT})					f = 1 kHz, mono operation
		310		mW	PVDD = 2.7 V, R_L = 8 Ω + 33 µH, THD + N = 1%
		700		mW	PVDD = 3.6 V, R_L = 8 Ω + 33 µH, THD + N = 1%
		1.0		W	PVDD = 4.2 V, R_L = 8 Ω + 33 µH, THD + N = 1%
		1.4		W	PVDD = 5.0 V, R_L = 8 Ω + 33 µH, THD + N = 1%
		700		mW	PVDD = 2.7 V, R_L = 4 Ω + 15 µH, THD + N = 1%
		1.5		W	PVDD = 3.6 V, R_L = 4 Ω + 15 µH, THD + N = 1%
		2.0		W	PVDD = 4.2 V, R_L = 4 Ω + 15 µH, THD + N = 1%
		2.9		W	PVDD = 5.0 V, R_L = 4 Ω + 15 µH, THD + N = 1%
		400		mW	PVDD = 2.7 V, R_L = 8 Ω + 33 µH, THD + N = 10%
		860		mW	PVDD = 3.6 V, R_L = 8 Ω + 33 µH, THD + N = 10%
		1.2		W	PVDD = 4.2 V, R_L = 8 Ω + 33 µH, THD + N = 10%
		1.7		W	PVDD = 5.0 V, R_L = 8 Ω + 33 µH, THD + N = 10%
		900		mW	PVDD = 2.7 V, R_L = 4 Ω + 15 µH, THD + N = 10%
		1.8		W	PVDD = 3.6 V, R_L = 4 Ω + 15 µH, THD + N = 10%
		2.5		W	PVDD = 4.2 V, R_L = 4 Ω + 15 µH, THD + N = 10%
		3.6		W	PVDD = 5.0 V, R_L = 4 Ω + 15 µH, THD + N = 10%
Total Harmonic Distortion Plus Noise (THD + N)		0.01		%	R_L = 8 Ω + 33 µH, P_{OUT} = 250 mW
Output Noise (V_n)		40		µV	20 Hz to 20 kHz, A-weighted
Signal-to-Noise Ratio (SNR)		94		dB	2.0 V rms output, A-weighted, PVDD = 5 V
Power Supply Rejection Ratio (PSRR)		80		dB	217 Hz, 200 mV p-p ripple
		80		dB	1 kHz, 200 mV p-p ripple
Common-Mode Rejection Ratio (CMRR)		55		dB	Differential input mode, 1 kHz, 10 mV rms
Efficiency		89		%	P_{OUT} = 700 mW
Minimum Load Resistance (R_{LOAD})	4			Ω	
Average Switching Frequency (f_{SW})		400		kHz	
Volume Control Gain Range	−63		+12	dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HEADPHONE OUTPUT					
Output Offset Voltage (V_{OS})		2		mV	Headphone only
		8		mV	INAx, INBx, INCx inputs
Output Power (P_{OUT})		20		mW	R_L = 32 Ω, THD + N = 1%
		40		mW	R_L = 16 Ω, THD + N = 1%, 1 µF charge pump capacitor
Total Harmonic Distortion Plus Noise (THD + N)		0.012		%	R_L = 32 Ω, P_{OUT} = 15 mW
		0.02		%	R_L = 16 Ω, P_{OUT} = 10 mW
Output Noise (V_n)		16		µV	20 Hz to 20 kHz, A-weighted
Signal-to-Noise Ratio (SNR)		96		dB	800 mV rms output, A-weighted
Power Supply Rejection Ratio (PSRR)		95		dB	217 Hz, 200 mV p-p ripple
		85		dB	1 kHz, 200 mV p-p ripple
Crosstalk		90		dB	1 kHz, P_{OUT} = 12 mW
Minimum Load Resistance (R_{LOAD})	16			Ω	
Maximum Capacitive Load (C_{LOAD})			500	pF	
Gain Range	−75		0	dB	
ESD Protection		±8		kV	
RECEIVER PATH (BYPASS SWITCH)					
Path Impedance (R_{ON}), Receiver Inputs to Speaker Outputs		1.5		Ω	RCV+ to EP+ and RCV− to EP−
Signal Path THD + N		0.1		%	P_{OUT} = 70 mW, R_L = 32 Ω or P_{OUT} = 17.5 mW, R_L = 8 Ω
Output Noise		10		µV	20 Hz to 20 kHz, A-weighted
Off Channel Isolation		90		dB	217 Hz, 200 mV p-p ripple
Input Common Mode			PVDD/2	V	

Table 2. Digital Logic Levels (CMOS Levels)

Parameter	Min	Typ	Max	Unit
Input Low Level (V_{IL})			0.35	V
Input High Level (V_{IH})	1.35			V
Output Low Level (V_{OL})			0.1 × AVDD	V
Output High Level (V_{OH})	0.9 × AVDD			V

I²C TIMING CHARACTERISTICS

Table 3.

Parameter	Limit		Unit	Description
	t_{MIN}	t_{MAX}		
t_{SCS}	600		ns	Start condition setup time
t_{SCH}	600		ns	Start condition hold time
t_{PH}	600		ns	SCL pulse width high
t_{PL}	1.3		µs	SCL pulse width low
f_{SCL}	0	526	kHz	SCL frequency
t_{DS}	100		ns	Data setup time
t_{DH}		900	ns	Data hold time
t_{RT}		300	ns	SDA and SCL rise time
t_{FT}		300	ns	SDA and SCL fall time
t_{HCS}	600		ns	Stop condition setup time

Timing Diagram

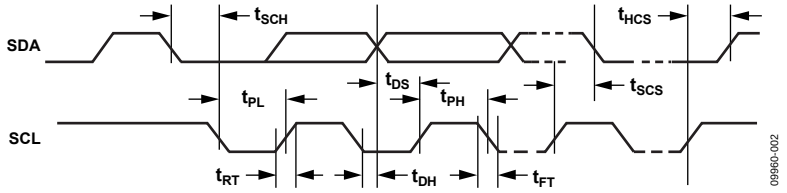

Figure 2. I²C Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
Analog Supply Voltage (AVDD)	−0.3 V to +3.6 V
Speaker Supply Voltage (PVDD)	−0.3 V to +3.6 V
Input Voltage	V_{DD}
$\overline{SD}$, SCL, SDA, RCV+, RCV−	−0.3 V to +6.0 V
INA1, INA2, INB1, INB2, INC1, INC2	−0.3 V to AVDD + 0.3 V
ESD (HBM) on Headphone Output	8 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
30-Ball, 2.5 mm × 3.0 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

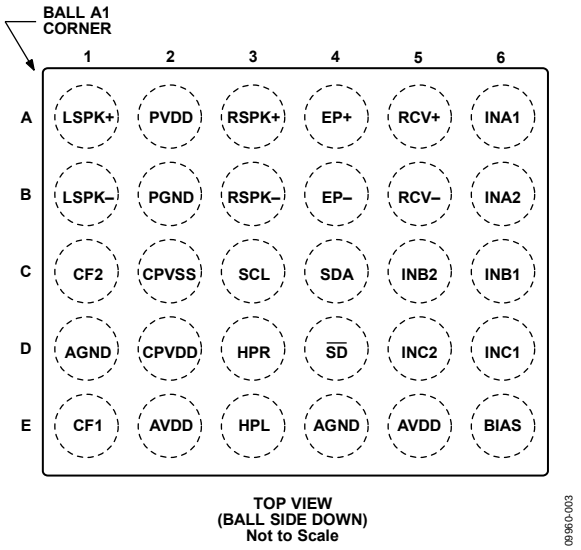

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	LSPK+	Class-D Loudspeaker Output Left +
B1	LSPK–	Class-D Loudspeaker Output Left –
C1	CF2	Charge Pump Flyback Capacitor, Terminal 2
D1	AGND	Analog Ground
E1	CF1	Charge Pump Flyback Capacitor, Terminal 1
A2	PVDD	Speaker Power Supply
B2	PGND	Speaker Ground
C2	CPVSS	Charge Pump Negative Supply for Class-G
D2	CPVDD	Charge Pump Positive Supply for Class-G
E2	AVDD	Analog Power Supply
A3	RSPK+	Class-D Loudspeaker Output Right +
B3	RSPK–	Class-D Loudspeaker Output Right –
C3	SCL	2-Wire I^2C Control Interface Clock Input
D3	HPR	Class-G Headphone Output, Right Channel
E3	HPL	Class-G Headphone Output, Left Channel
A4	EP+	Integrated Switch Output +
B4	EP–	Integrated Switch Output –
C4	SDA	2-Wire I^2C Control Interface Data Input/Output
D4	$\overline{SD}$	Shutdown Control, Active Low (Optional Limiter Threshold Voltage)
E4	AGND	Analog Ground
A5	RCV+	Baseband Receiver (Voice) Input +
B5	RCV–	Baseband Receiver (Voice) Input –
C5	INB2	Configurable Input B2 (Single-Ended Input B– or Stereo Input B, Left Channel)
D5	INC2	Configurable Input C2 (Single-Ended Input C– or Stereo Input C, Left Channel)
E5	AVDD	Analog Power Supply
A6	INA1	Configurable Input A1 (Single-Ended Input A+ or Stereo Input A, Right Channel)
B6	INA2	Configurable Input A2 (Single-Ended Input A– or Stereo Input A, Left Channel)
C6	INB1	Configurable Input B1 (Single-Ended Input B+ or Stereo Input B, Right Channel)
D6	INC1	Configurable Input C1 (Single-Ended Input C+ or Stereo Input C, Right Channel)
E6	BIAS	Device Bias Pin

TYPICAL PERFORMANCE CHARACTERISTICS

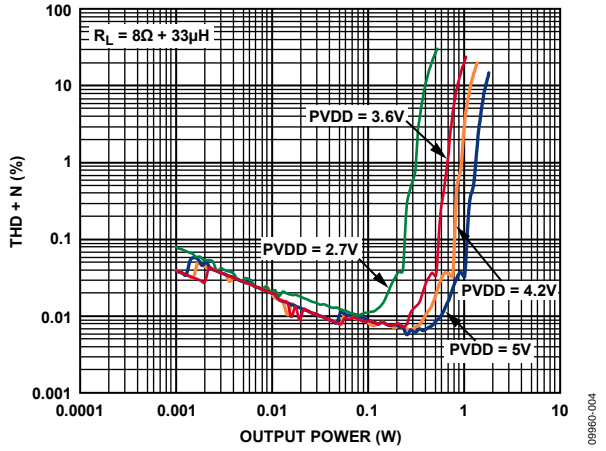

Figure 4. THD + N vs. Output Power into 8 Ω, Class-D Amplifier, Mono Operation

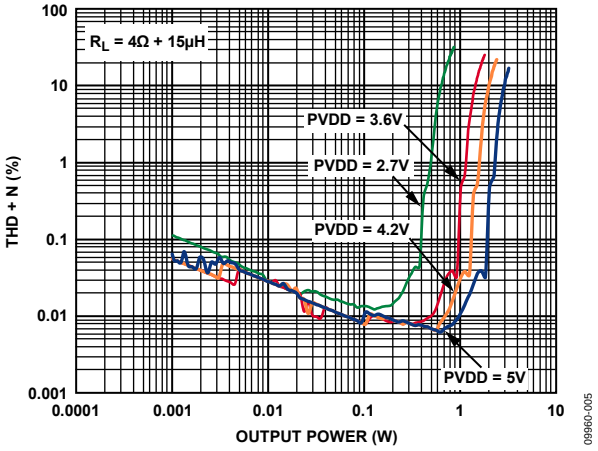

Figure 7. THD + N vs. Output Power into 4 Ω, Class-D Amplifier, Mono Operation

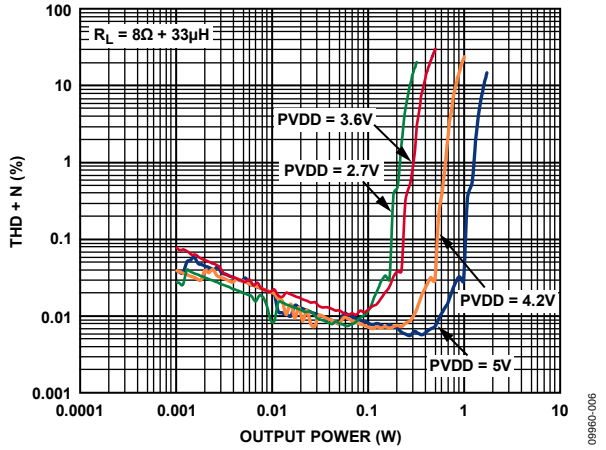

Figure 5. THD + N vs. Output Power into 8 Ω, Class-D Amplifier, Stereo Operation

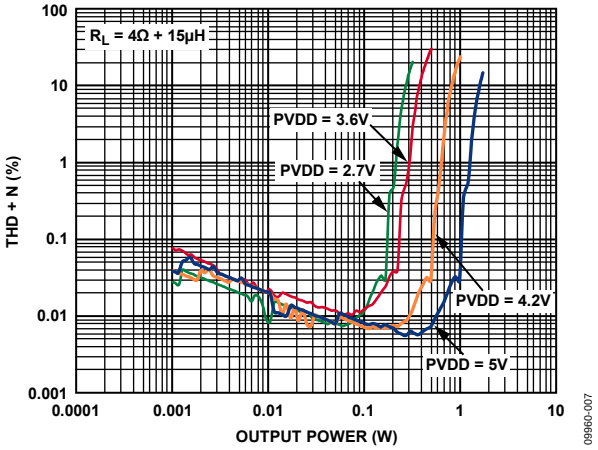

Figure 8. THD + N vs. Output Power into 4 Ω, Class-D Amplifier, Stereo Operation

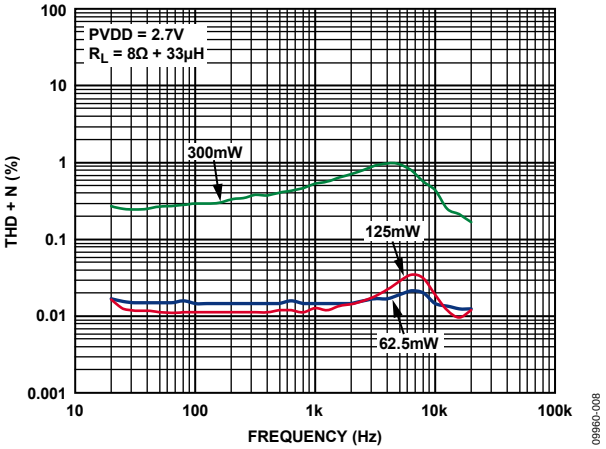

Figure 6. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 8 Ω, PVDD = 2.7 V

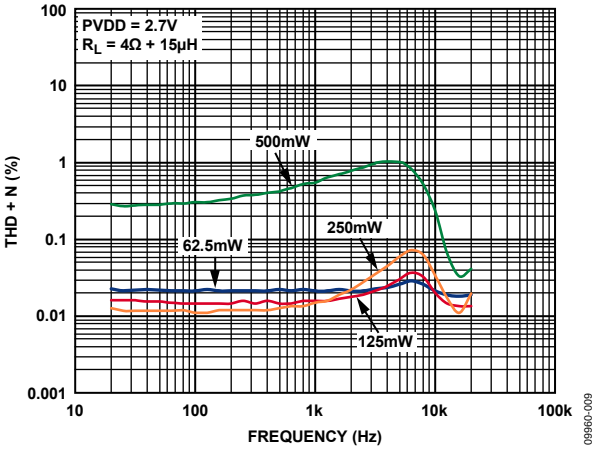

Figure 9. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 4 Ω, PVDD = 2.7 V

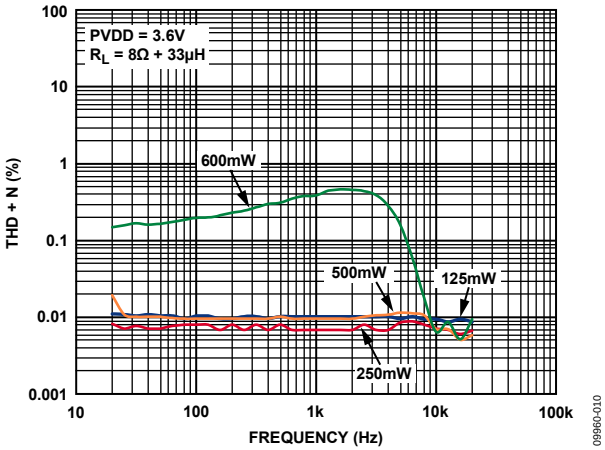

Figure 10. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 8 Ω, PVDD = 3.6 V

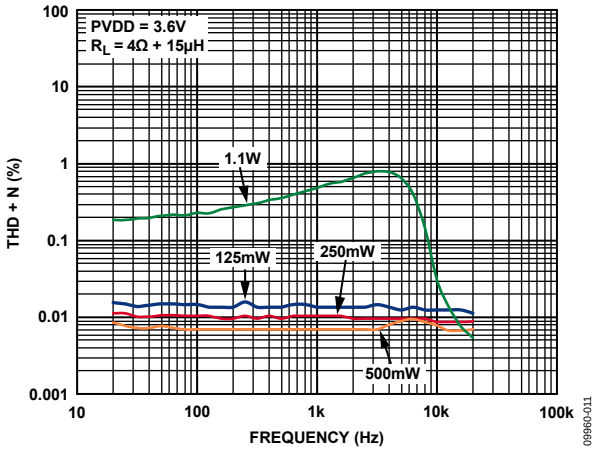

Figure 13. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 4 Ω, PVDD = 3.6 V

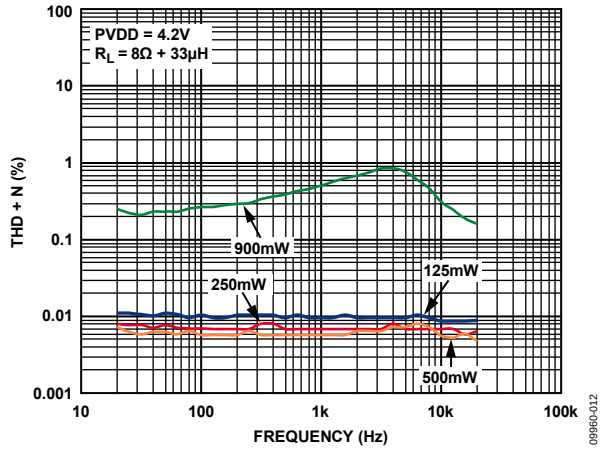

Figure 11. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 8 Ω, PVDD = 4.2 V

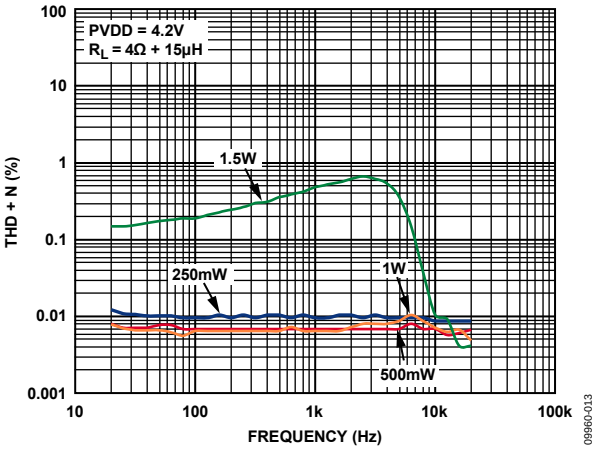

Figure 14. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 4 Ω, PVDD = 4.2 V

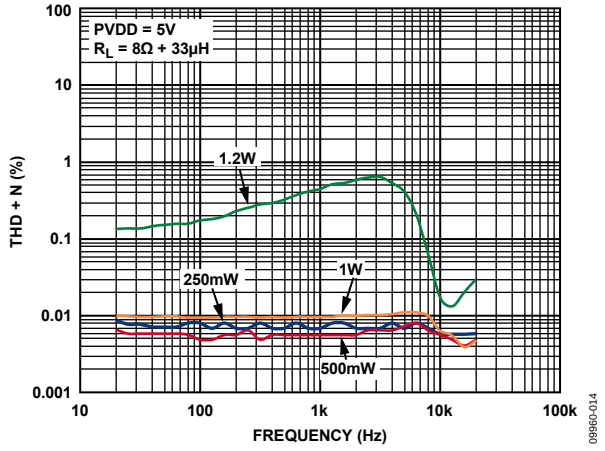

Figure 12. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 8 Ω, PVDD = 5.0 V

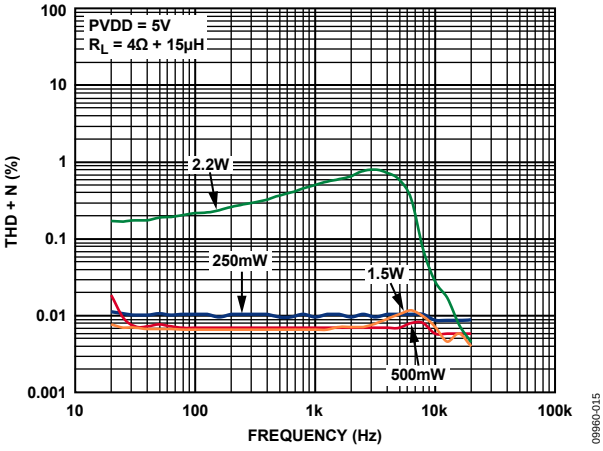

Figure 15. THD + N vs. Frequency, Class-D Amplifier, Mono Operation, R_L = 4 Ω, PVDD = 5.0 V

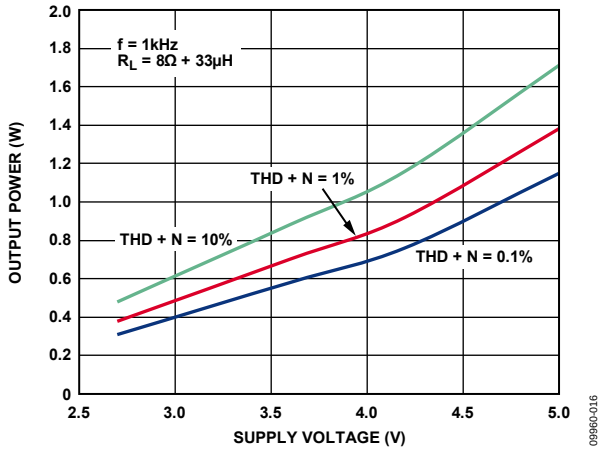

Figure 16. Output Power vs. Supply Voltage, Class-D Amplifier, R_L = 8 Ω

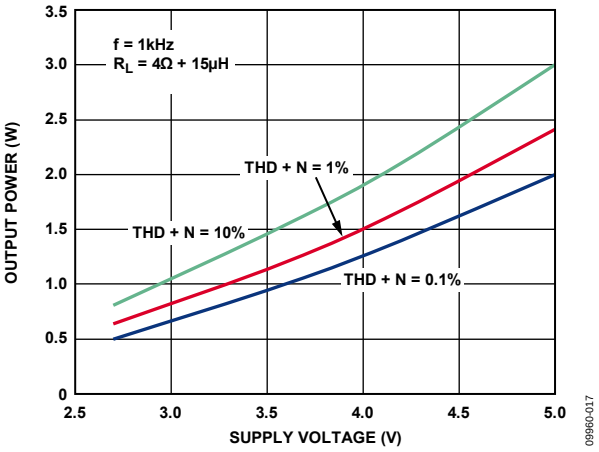

Figure 19. Output Power vs. Supply Voltage, Class-D Amplifier, R_L = 4 Ω

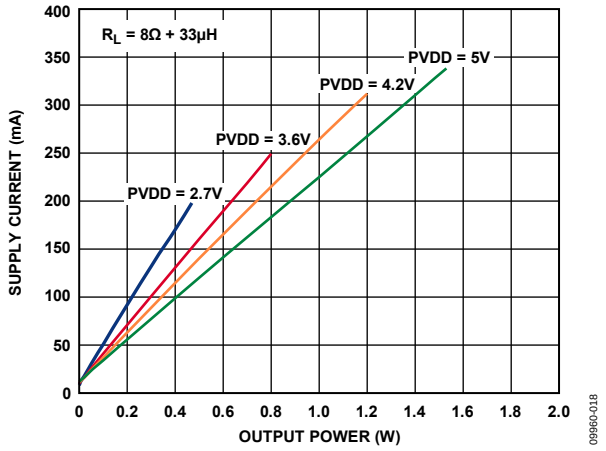

Figure 17. Supply Current vs. Output Power into 8 Ω, Class-D Amplifier

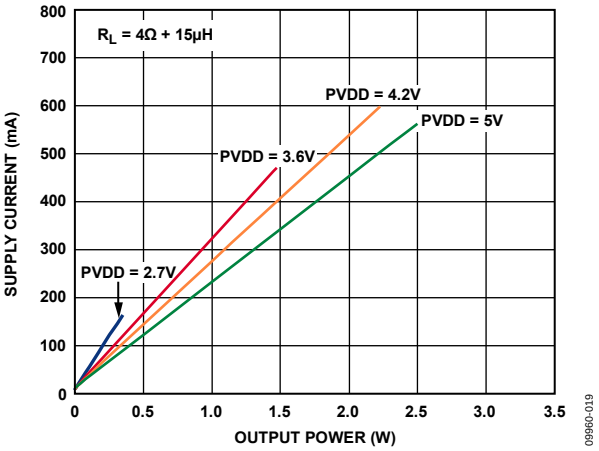

Figure 20. Supply Current vs. Output Power into 4 Ω, Class-D Amplifier

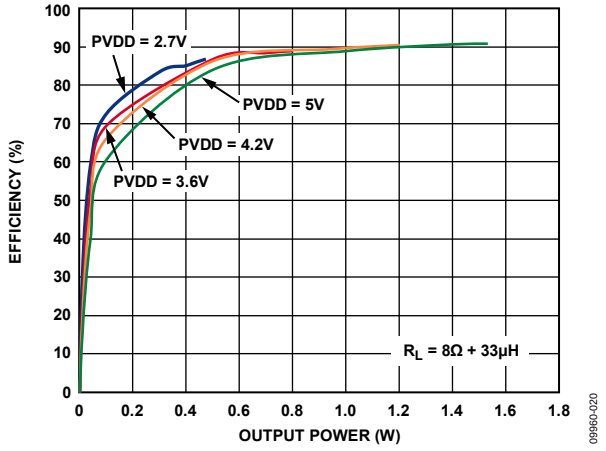

Figure 18. Efficiency vs. Output Power into 8 Ω, Class-D Amplifier

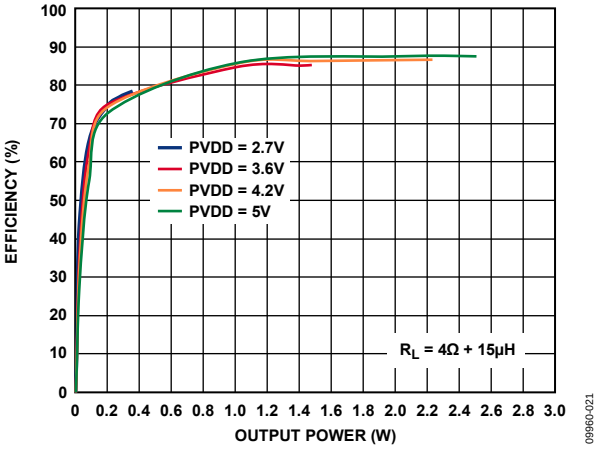

Figure 21. Efficiency vs. Output Power into 4 Ω, Class-D Amplifier

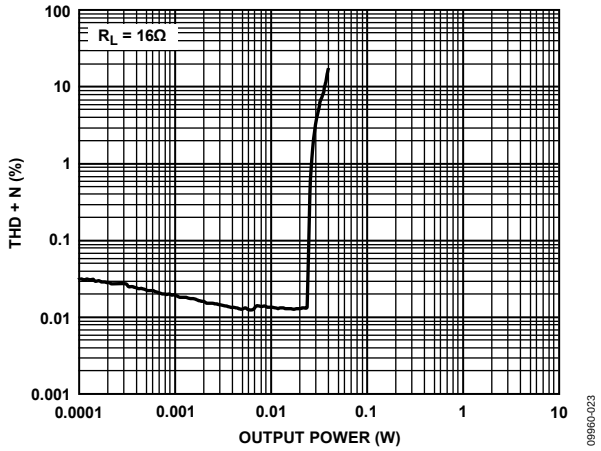

Figure 22. THD + N vs. Output Power into 16 Ω, Headphone Amplifier, Stereo Operation

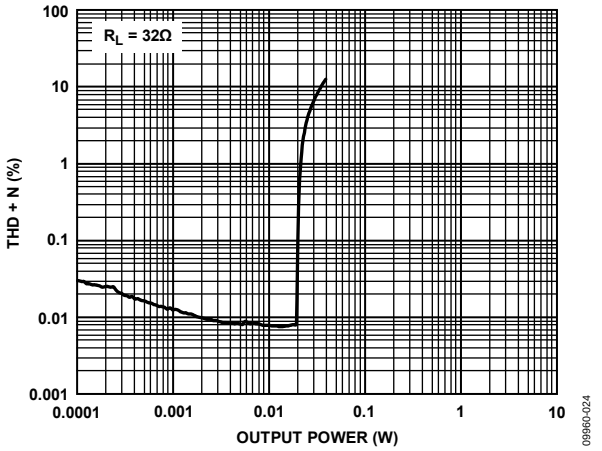

Figure 25. THD + N vs. Output Power into 32 Ω, Headphone Amplifier, Stereo Operation

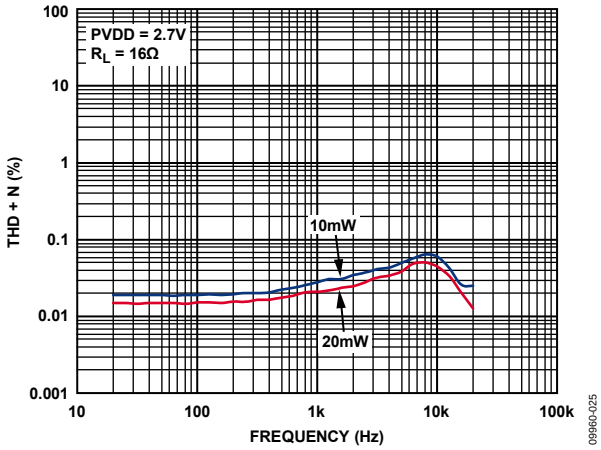

Figure 23. THD + N vs. Frequency, Headphone Amplifier, R_L = 16 Ω, PVDD = 2.7 V

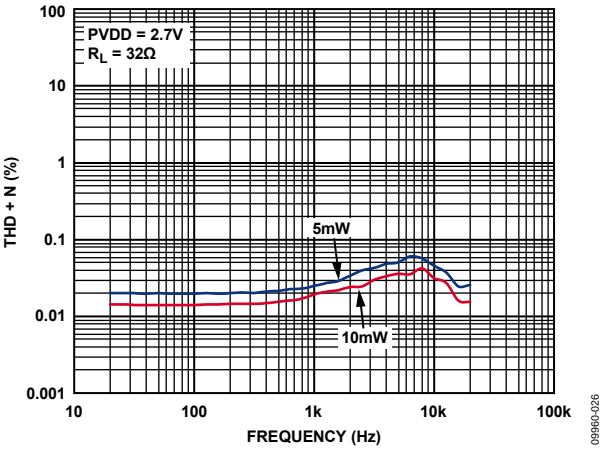

Figure 26. THD + N vs. Frequency, Headphone Amplifier, R_L = 32 Ω, PVDD = 2.7 V

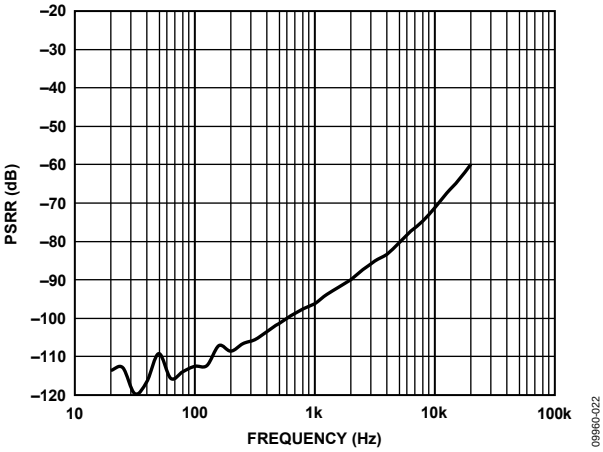

Figure 24. Power Supply Rejection Ratio (PSRR) vs. Frequency, Class-D Amplifier

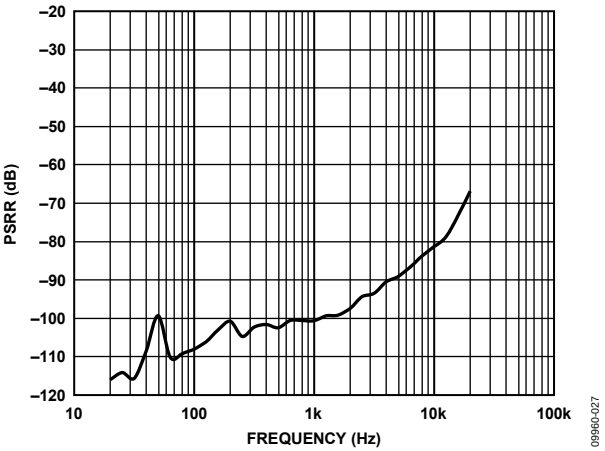

Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency, Headphone Amplifier

THEORY OF OPERATION

The SSM2804 audio subsystem features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing system cost. The SSM2804 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2804 uses Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits.

- Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do.
- Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emissions that might otherwise be radiated by speakers and long cable traces.
- The SSM2804 does not require external EMI filtering for twisted speaker cable lengths shorter than 10 cm. If longer speaker cables are used, the SSM2804 has emission limiting circuitry that allows significantly longer speaker cable.
- Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for modulator synchronization is eliminated for designs that incorporate multiple SSM2804 amplifiers.

Using the I²C control interface, the gain of the SSM2804 can be selected from a range of +12 dB to −63 dB in 32 steps. Other features accessed from the I²C interface include the following:

- Independent left/right channel shutdown
- Variable ultralow EMI emission limiting circuitry
- Automatic level control (ALC) for high quality speaker protection
- Stereo-to-mono mixing operation

The SSM2804 also offers protection circuits for overcurrent and overtemperature protection.

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients may be generated when the amplifier system changes its operating mode. For example, the following may be sources of audible transients: system power-up and power-down, mute and unmute, input source change, and sample rate change.

The SSM2804 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM2804 uses three-level, Σ-Δ output modulation. Each output can swing from GND to V_{DD} and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to the constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUT+ and OUT−) is generated to follow the input voltage. The differential pulse density (V_{OUT}) is increased by raising the input signal level. Figure 28 depicts three-level, Σ-Δ output modulation with and without input stimulus.

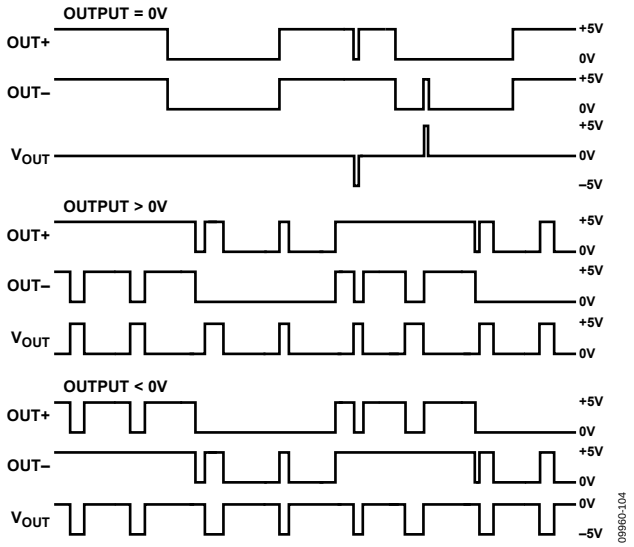

Figure 28. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

HARDWARE-BASED HEADPHONE LIMITER

To provide fail-safe headphone level limiting independent of the register values sent to the amplifier over the I²C bus, the SSM2804 incorporates an optional hardware-based headphone limiter feature. The user controls the limiter level by supplying a voltage at the $\overline{SD}$ pin (see Table 7). The hardware limiter is activated by setting the LIM_MODE bit to 0 in the additional control register (Bit D3 of Register 0x0E). After the desired limiter value is set, the user can lock the limiter setting by setting the LIMLOCK bit (Bit D7 of Register 0x0E).

Table 7. Hardware Limiter Options

Limiter Level	Power into 32 Ω (mW)	Power into 16 Ω (mW)	$\overline{SD}$ Pin Voltage
Shutdown	N/A	N/A	<0.87 V
±0.40 V	2.5	5	0.87 V < $V_{\overline{SD}}$ < 1.08 V
±8 V	10	20	1.08 V < $V_{\overline{SD}}$ < 1.29 V
±1.13 V	20	40	$V_{\overline{SD}}$ > 1.29 V

Note that after the hardware limiter lock bit is set, the locked levels cannot be reset until the SSM2804 is powered down, the $\overline{SD}$ pin is strobed low, or all eight bits of the software reset register (Register 0x10) are set to 0.

In addition to the hardware-based limiter, several other limiter levels can be selected using the I²C-based limiter function (set the HPLIM bits of Register 0x0E; see Table 44). The effect of the limiter function on the headphone output is shown in Figure 29.

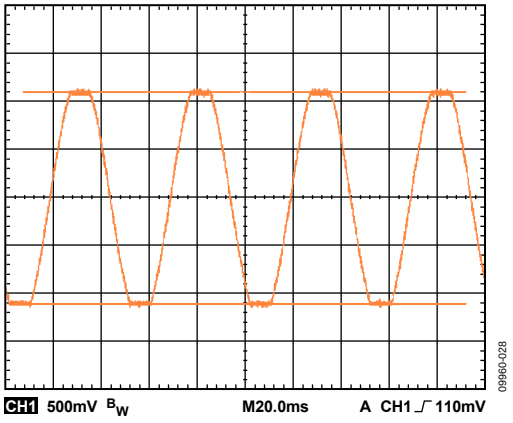

Figure 29. Limited Headphone Signal

ACTIVATING OR DEACTIVATING THE EMISSION LIMITING CIRCUITRY

To activate or deactivate the emission limiting circuitry, change the value of the EDGE bits in the additional control register (Bits[D1:D0] of Register 0x0E). Four levels of emission control are available, allowing the user to determine the best trade-off between efficiency and EMI reduction.

In the default (fastest edge) mode, the user can pass FCC Class-B emission testing with 10 cm twisted pair speaker wire for loudspeaker connection. If longer speaker wire is desired, change the EDGE setting to a slower edge rate mode. The trade-off is slightly lower efficiency and noise performance. The penalty for using the emission control circuitry is far less than the decreased performance observed when using a ferrite bead based EMI filter for emission limiting purposes.

AUTOMATIC LEVEL CONTROL (ALC)

Automatic level control (ALC) is a function that automatically adjusts amplifier gain to generate the desired output amplitude with reference to a particular input stimulus. The primary use for the ALC is to protect an audio power amplifier or speaker load from the damaging effects of clipping or current overloading. This is accomplished by limiting the output amplitude of the amplifier upon reaching a preset threshold voltage. Another benefit of the ALC is that it makes sound sources with a wide dynamic range more intelligible by boosting low level signals and limiting very high level signals.

Before activating the ALC by setting the ALCEN bit (Bit D7 of Register 0x0B), the user has full control of the left and right channel PGA gain. After the ALC is activated (ALCEN = 1), the user has no control over the gain settings; the left channel PGA gain is locked into the device and controls the gain for both the left and right channels. To change the gain, the user must reset the ALCEN bit to 0 and then load the new gain settings.

Figure 30 shows the response of the SSM2804 to a linearly increasing input signal. When the output reaches the current threshold value, the amplifier gain decreases by 0.5 dB so that the output voltage remains under the threshold. As more attenuation is added to the system, the threshold increases according to a profile determined by the compressor setting bits in the ALC Control 2 register (Bits[D6:D5] of Register 0x0B), causing a rounded "knee" as the output voltage approaches the output limiter level. The effect of this compression curve is shown in Figure 30.

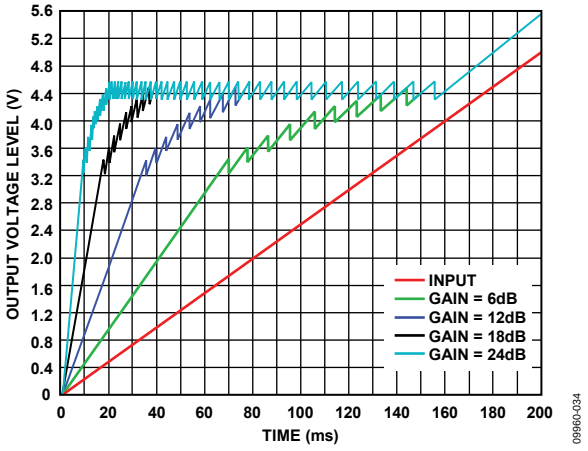

Figure 30. Output Response to Linearly Increasing Input Ramp Signal

When the input level is small and the output voltage is smaller than the ALC threshold value, the gain of the amplifier stays at the preset gain setting. When the input exceeds the ALC threshold value, the ALC gradually reduces the gain from the preset gain setting down to 1 dB.

ALC Compression and Limiter Modes

The ALC implemented on the SSM2804 has two operation modes: compression mode and limiter mode. When the ALC is triggered for medium-level input signals, the ALC is in compression mode. In this mode, an increase of the output signal is one-third the increase of the input signal. For example, if the input signal increases by 3 dB, the ALC reduces the amplifier gain by 2 dB and, thus, the output signal increases by only 1 dB.

As the input signal becomes very large, the ALC transitions to limiter mode. In this mode, the output stays at a given threshold level, V_{TH}, even if the input signal grows larger. As an example of limiter mode operation, when a large input signal increases by 3 dB, the ALC reduces the amplifier gain by 3 dB and, thus, the output increases by 0 dB. When the amplifier gain is reduced to 1 dB, the ALC cannot reduce the gain further, and the output increases again. This is because the total range of the ALC operation has bottomed out due to extreme input voltage at high gain. To avoid potential speaker damage, the maximum input amplitude should not be large enough to exceed the maximum attenuation (to a level of 1 dB) of the limiter mode.

Attack Time, Hold Time, and Release Time

When the amplifier input signal exceeds a preset threshold, the ALC reduces amplifier gain rapidly until the output voltage settles to a target level. This target level is maintained for a certain period. If the input voltage does not exceed the threshold again, the ALC increases the gain gradually.

The attack time is the time taken to reduce the gain from maximum to minimum. The hold time is the time that the reduced gain is maintained. The release time is the time taken to increase the gain from minimum to maximum. These times are shown in Table 8. The attack time and the release time can be set using the ALC 1 control register (Address 0x0A).

Table 8. ALC Attack, Hold, and Release Times

Time[1]	Duration
Attack Time	32 µs to 4 ms (per 0.5 dB step)
Hold Time	90 ms to 120 ms
Release Time	4 ms to 512 ms (per 0.5 dB step)

[1] The attack time and release time can be adjusted using the I²C interface. The hold time cannot be adjusted.

Soft-Knee Compression

Often performed using sophisticated DSP algorithms, soft-knee compression provides maximum sound quality with effective speaker protection. Instead of using a fixed compression setting prior to limiting, the SSM2804 allows for a much more subtle transition into limiting mode, preserving the original sound quality of the source audio. Figure 31 to Figure 33 show the various soft-knee compression settings that can be selected using the COMP bit settings (Bits[D6:D5] of Register 0x0B).

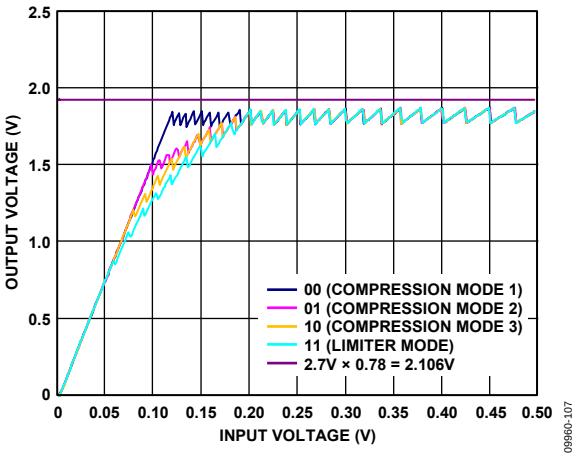

Figure 31. Adjustable Compression Settings, PVDD = 2.7 V, ALC Threshold Level = 78%

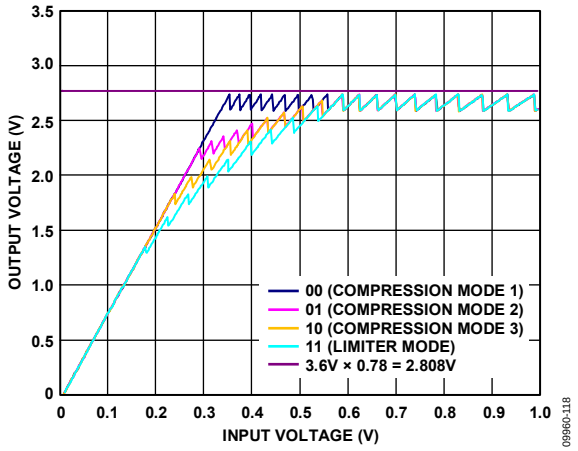

Figure 32. Adjustable Compression Settings, PVDD = 3.6 V, ALC Threshold Level = 78%

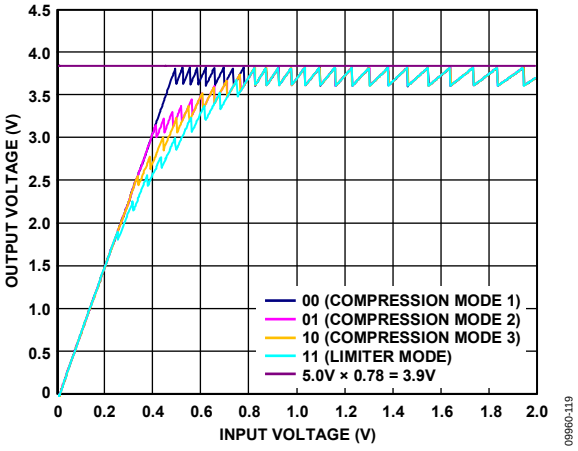

Figure 33. Adjustable Compression Settings, PVDD = 5.0 V, ALC Threshold Level = 78%

ALC Soft Transition

The ALC operation of the SSM2804 incorporates techniques to reduce the audible artifacts associated with gain change transitions. First, the gain is changed in small increments of 0.5 dB. In addition to this small step size, the rate of gain change is reduced, proportional to the attack time setting. This feature drastically reduces and virtually eliminates the presence of zipper noise and other artifacts associated with gain transitions during ALC operation. Figure 34 shows the soft transition operation.

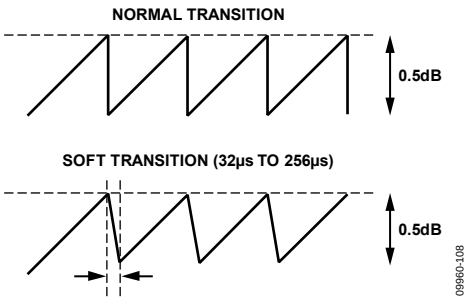

Figure 34. Soft Transition

TYPICAL APPLICATION CIRCUITS

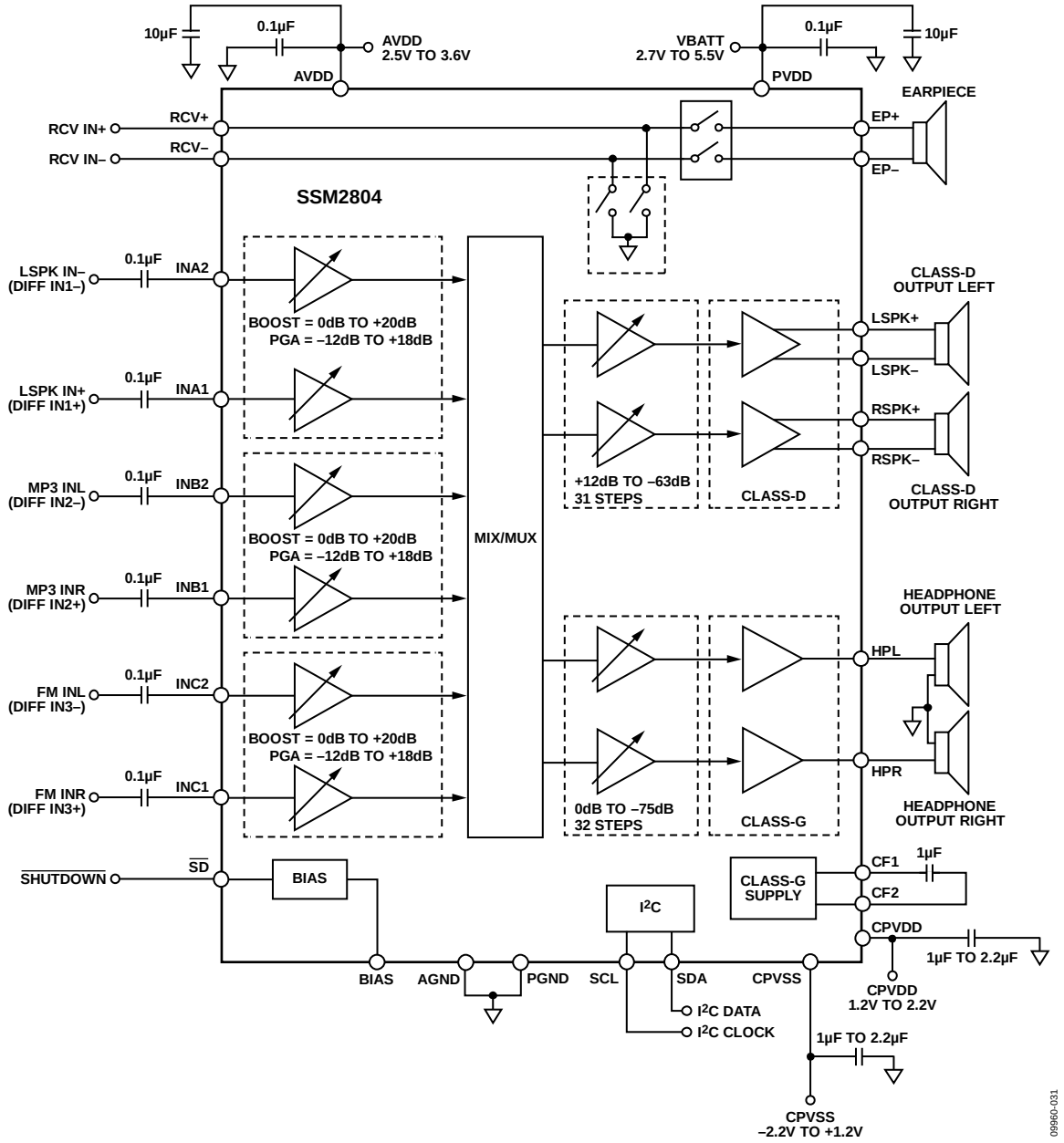

Figure 35. Application Circuit with External Components

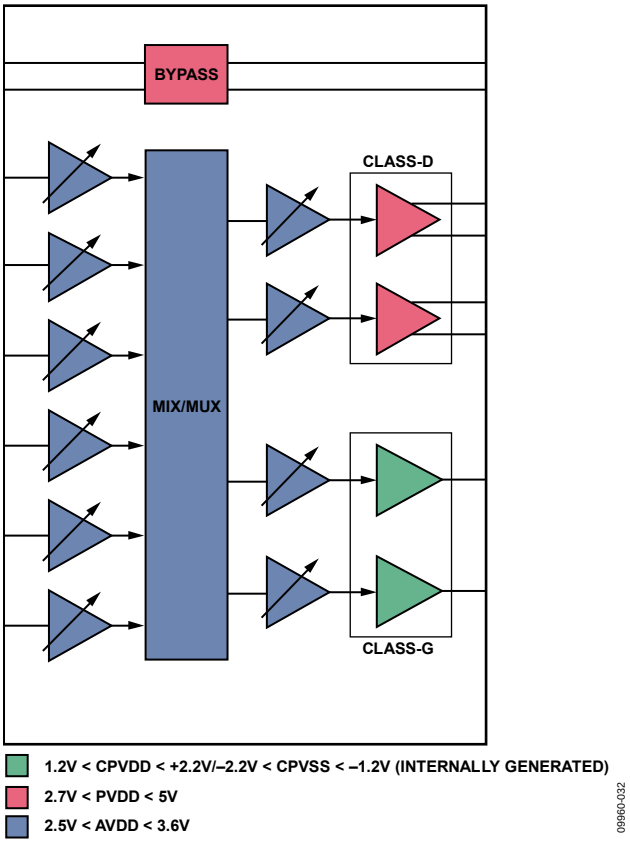

Figure 36. Power Supply Domains

I²C SOFTWARE CONTROL INTERFACE

The I²C interface provides access to the user-selectable control registers and operates with a 2-wire interface.

Each control register consists of 16 bits, MSB first. Bits[B15:B9] are the register map address, and Bits[B8:B0] are the register data for the associated register map.

SDA generates the serial control data-word, and SCL clocks the serial data. The I²C bus address (Bits[A7:A1]) is 0x3B (01110110 for write and 01110111 for read). Bit A0 is the designated read/write bit.

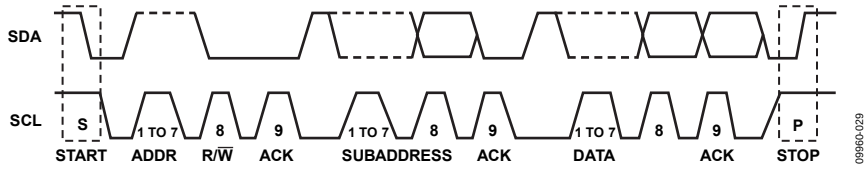

Figure 37. 2-Wire I²C Generalized Clocking Diagram

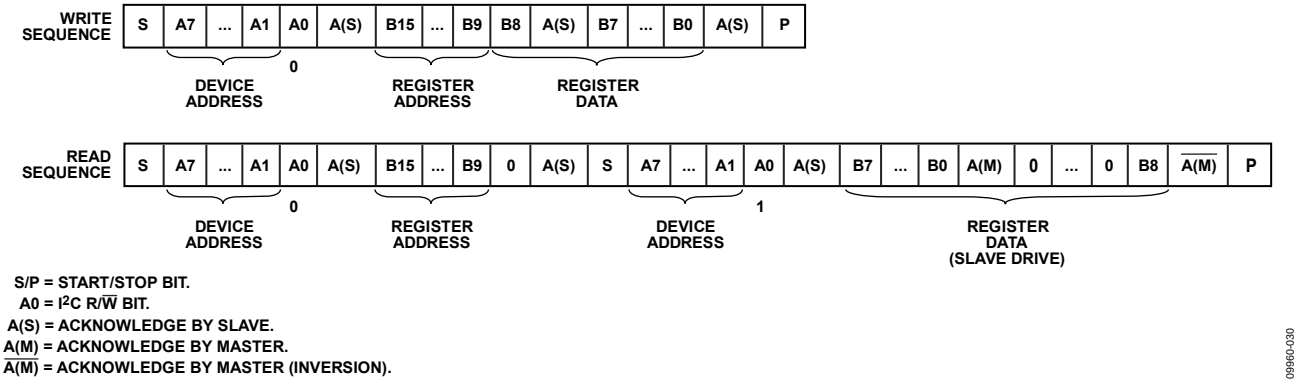

Figure 38. I²C Write and Read Sequences

REGISTER MAP

The 7-bit I²C address of the SSM2804 is 0x3B (0111011).

Table 9. Register Map

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00	Input mode	0	ZCD	GAINMOD[2:0]			INMOD[2:0]			0x00
0x01	INA volume	0	0	0	INAVOL[4:0]					0x00
0x02	INB volume	0	0	0	INBVOL[4:0]					0x00
0x03	INC volume	0	0	0	INCVOL[4:0]					0x00
0x04	Class-D left volume	0	0	0	LCDVOL[4:0]					0x00
0x05	Class-D right volume	0	0	0	RCDVOL[4:0]					0x00
0x06	LHP volume	0	0	0	LHPVOL[4:0]					0x00
0x07	RHP volume	0	0	0	RHPVOL[4:0]					0x00
0x08	HP input mixer	POPTIME[1:0]		RHPMOD[2:0]			LHPMOD[2:0]			0x00
0x09	Class-D input mixer	CDSM[1:0]		RCDMOD[2:0]			LCDMOD[2:0]			0x00
0x0A	ALC Control 1	0	0	RECTIME[2:0]			ATTIME[2:0]			0x2B
0x0B	ALC Control 2	ALCEN	COMP[1:0]		ALCLV_FIX	ALCLV[3:0]				0x4B
0x0C	ALC Control 3	0	LCDBOOST	RCDBOOST	SOFTSTART	SOFTCLIPEN	NGEN	NGATE[1:0]		0x00
0x0D	Power-down control	PASSPDB	INCPDB	INBPDB	INAPDB	RCDPDB	LCDPDB	HPPDB	PWDB	0x00
0x0E	Additional control	LIMLOCK	HPLIM[2:0]			LIM_MOD	TO	EDGE[1:0]		0x00
0x0F	Chip status[1]	0	0	0	0	OCCD	OCHP	OW	OT	0x00
0x10	Software reset[2]	SOFTRESET								0x00

[1] This byte is read-only.
[2] This byte is write-only.

REGISTER MAP DETAILS

INPUT CHANNEL MODE CONTROL, ADDRESS 0x00

Table 10. Input Channel Mode Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	ZCD	GAINMOD[2:0]			INMOD[2:0]		

Table 11. Input Channel Mode Control Register Bit Descriptions

Bit Name	Description	Settings
ZCD	Zero cross-detector enable	0 = disable (default) 1 = enable
GAINMOD[2:0]	Input amplifier gain mode	xx0 = Input A PGA mode xx1 = Input A boost mode x0x = Input B PGA mode x1x = Input B boost mode 0xx = Input C PGA mode 1xx = Input C boost mode
INMOD[2:0]	Input mode control	xx0 = Input A stereo mode (INA1, INA2 > INAL, INAR) xx1 = Input A differential mode (INA1, INA2 > INA+, INA−) x0x = Input B stereo mode (INB1, INB2 > INBL, INBR) x1x = Input B differential mode (INB1, INB2 > INB+, INB−) 0xx = Input C stereo mode (INC1, INC2 > INCL, INCR) 1xx = Input C differential mode (INC1, INC2 > INC+, INC−) See Table 12 for complete information about the naming table

Table 12. Input Mode Naming Table

INMOD[2:0]	INA1 Pin	INA2 Pin	INB1 Pin	INB2 Pin	INC1 Pin	INC2 Pin
000	INAL	INAR	INBL	INBR	INCL	INCR
001	INAL	INAR	INBL	INBR	INC+	INC−
010	INAL	INAR	INB+	INB−	INCL	INCR
011	INAL	INAR	INB+	INB−	INC+	INC−
100	INA+	INA−	INBL	INBR	INCL	INCR
101	INA+	INA−	INBL	INBR	INC+	INC−
110	INA+	INA−	INB+	INB−	INCL	INCR
111	INA+	INA−	INB+	INB−	INC+	INC−

CHANNEL A LINE INPUT VOLUME, ADDRESS 0x01

Table 13. Channel A Line Input Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	INAVOL[4:0]				

Table 14. Channel A Line Input Volume Register Bit Descriptions

Bit Name	Description	Settings
INAVOL[4:0]	Analog Channel A input volume control	See Table 15

Table 15. Descriptions of Channel A Volume Register Bits

INAVOL[4:0]	PGA Mode (dB)	Boost Mode (dB)
00000	Mute	Mute
00001	−12	0
00010	−11	0
00011	−10	0
00100	−9	0
00101	−8	0
00110	−7	0
00111	−6	0
01000	−5	0
01001	−4	0
01010	−3	0
01011	−2	0
01100	−1	0
01101	0	0
01110	1	9
01111	2	9
10000	3	9
10001	4	9
10010	5	9
10011	6	9
10100	7	20
10101	8	20
10110	9	20
10111	10	20
11000	11	20
11001	12	20
11010	13	20
11011	14	20
11100	15	20
11101	16	20
11110	17	20
11111	18	20

CHANNEL B LINE INPUT VOLUME, ADDRESS 0x02

Table 16. Channel B Line Input Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	INBVOL[4:0]				

Table 17. Channel B Line Input Volume Register Bit Descriptions

Bit Name	Description	Settings
INBVOL[4:0]	Analog Channel B input volume control	See Table 18

Table 18. Descriptions of Channel B Input Volume Register Bits

INBVOL[4:0]	PGA Mode (dB)	Boost Mode (dB)
00000	Mute	Mute
00001	−12	0
00010	−11	0
00011	−10	0
00100	−9	0
00101	−8	0
00110	−7	0
00111	−6	0
01000	−5	0
01001	−4	0
01010	−3	0
01011	−2	0
01100	−1	0
01101	0	0
01110	1	9
01111	2	9
10000	3	9
10001	4	9
10010	5	9
10011	6	9
10100	7	20
10101	8	20
10110	9	20
10111	10	20
11000	11	20
11001	12	20
11010	13	20
11011	14	20
11100	15	20
11101	16	20
11110	17	20
11111	18	20

CHANNEL C LINE INPUT VOLUME, ADDRESS 0x03

Table 19. Channel C Line Input Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	INCVOL[4:0]				

Table 20. Channel C Line Input Volume Register Bit Descriptions

Bit Name	Description	Settings
INCVOL[4:0]	Analog Channel C input volume control	See Table 21

Table 21. Descriptions of Channel C Input Volume Register Bits

INCVOL[4:0]	PGA Mode (dB)	Boost Mode (dB)
00000	Mute	Mute
00001	−12	0
00010	−11	0
00011	−10	0
00100	−9	0
00101	−8	0
00110	−7	0
00111	−6	0
01000	−5	0
01001	−4	0
01010	−3	0
01011	−2	0
01100	−1	0
01101	0	0
01110	1	9
01111	2	9
10000	3	9
10001	4	9
10010	5	9
10011	6	9
10100	7	20
10101	8	20
10110	9	20
10111	10	20
11000	11	20
11001	12	20
11010	13	20
11011	14	20
11100	15	20
11101	16	20
11110	17	20
11111	18	20

CLASS-D LEFT LOUDSPEAKER OUTPUT VOLUME, ADDRESS 0x04

Table 22. Class-D Left Loudspeaker Output Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LCDVOL[4:0]				

Table 23. Class-D Left Loudspeaker Output Volume Register Bit Descriptions

Bit Name	Description	Settings
LCDVOL[4:0]	Left channel Class-D volume control	00000 = mute (default) 00001 = −75 dB 00010 = −71 dB 00011 = −67 dB 00100 = −63 dB 00101 = −59 dB 00110 = −55 dB 00111 = −51 dB 01000 = −47 dB 01001 = −44 dB 01010 = −41 dB 01011 = −38 dB 01100 = −35 dB 01101 = −32 dB 01110 = −29 dB 01111 = −26 dB 10000 = −23 dB 10001 = −21 dB 10010 = −19 dB 10011 = −17 dB 10100 = −15 dB 10101 = −13 dB 10110 = −11 dB 10111 = −9 dB 11000 = −7 dB 11001 = −6 dB 11010 = −5 dB 11011 = −4 dB 11100 = −3 dB 11101 = −2 dB 11110 = −1 dB 11111 = 0 dB

CLASS-D RIGHT LOUDSPEAKER OUTPUT VOLUME, ADDRESS 0x05

Table 24. Class-D Right Loudspeaker Output Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	RCDVOL[4:0]				

Table 25. Class-D Right Loudspeaker Output Volume Register Bit Descriptions

Bit Name	Description	Settings
RCDVOL[4:0]	Right channel Class-D volume control	00000 = mute (default) 00001 = −75 dB 00010 = −71 dB 00011 = −67 dB 00100 = −63 dB 00101 = −59 dB 00110 = −55 dB 00111 = −51 dB 01000 = −47 dB 01001 = −44 dB 01010 = −41 dB 01011 = −38 dB 01100 = −35 dB 01101 = −32 dB 01110 = −29 dB 01111 = −26 dB 10000 = −23 dB 10001 = −21 dB 10010 = −19 dB 10011 = −17 dB 10100 = −15 dB 10101 = −13 dB 10110 = −11 dB 10111 = −9 dB 11000 = −7 dB 11001 = −6 dB 11010 = −5 dB 11011 = −4 dB 11100 = −3 dB 11101 = −2 dB 11110 = −1 dB 11111 = 0 dB

LEFT HEADPHONE OUTPUT VOLUME, ADDRESS 0x06

Table 26. Left Headphone Output Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LHPVOL[4:0]				

Table 27. Left Headphone Output Volume Register Bit Descriptions

Bit Name	Description	Settings
LHPVOL[4:0]	Left headphone output volume control	00000 = mute (default) 00001 = −75 dB 00010 = −71 dB 00011 = −67 dB 00100 = −63 dB 00101 = −59 dB 00110 = −55 dB 00111 = −51 dB 01000 = −47 dB 01001 = −44 dB 01010 = −41 dB 01011 = −38 dB 01100 = −35 dB 01101 = −32 dB 01110 = −29 dB 01111 = −26 dB 10000 = −23 dB 10001 = −21 dB 10010 = −19 dB 10011 = −17 dB 10100 = −15 dB 10101 = −13 dB 10110 = −11 dB 10111 = −9 dB 11000 = −7 dB 11001 = −6 dB 11010 = −5 dB 11011 = −4 dB 11100 = −3 dB 11101 = −2 dB 11110 = −1 dB 11111 = 0 dB

RIGHT HEADPHONE OUTPUT VOLUME, ADDRESS 0x07

Table 28. Right Headphone Output Volume Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	RHPVOL[4:0]				

Table 29. Right Headphone Output Volume Register Bit Descriptions

Bit Name	Description	Settings
RHPVOL[4:0]	Right headphone output volume control	00000 = mute (default) 00001 = −75 dB 00010 = −71 dB 00011 = −67 dB 00100 = −63 dB 00101 = −59 dB 00110 = −55 dB 00111 = −51 dB 01000 = −47 dB 01001 = −44 dB 01010 = −41 dB 01011 = −38 dB 01100 = −35 dB 01101 = −32 dB 01110 = −29 dB 01111 = −26 dB 10000 = −23 dB 10001 = −21 dB 10010 = −19 dB 10011 = −17 dB 10100 = −15 dB 10101 = −13 dB 10110 = −11 dB 10111 = −9 dB 11000 = −7 dB 11001 = −6 dB 11010 = −5 dB 11011 = −4 dB 11100 = −3 dB 11101 = −2 dB 11110 = −1 dB 11111 = 0 dB

HEADPHONE INPUT MIXER CONTROL, ADDRESS 0x08

Table 30. Headphone Input Mixer Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
POPTIME[1:0]		RHPMOD[2:0]			LHPMOD[2:0]		

Table 31. Headphone Input Mixer Control Register Bit Descriptions

Bit Name	Description	Settings
POPTIME[1:0]	Headphone turn-on time constant setting	00 = 10 ms (default) 01 = 20 ms 10 = 40 ms 11 = 80 ms (smallest pop-and-click)
RHPMOD[2:0]	Right headphone input mixer	xx0 = Analog Input A disabled (default) xx1 = Analog Input A enabled x0x = Analog Input B disabled (default) x1x = Analog Input B enabled 0xx = Analog Input C disabled (default) 1xx = Analog Input C enabled
LHPMOD[2:0]	Left headphone input mixer	xx0 = Analog Input A disabled (default) xx1 = Analog Input A enabled x0x = Analog Input B disabled (default) x1x = Analog Input B enabled 0xx = Analog Input C disabled (default) 1xx = Analog Input C enabled

CLASS-D INPUT MIXER CONTROL, ADDRESS 0x09

Table 32. Class-D Input Mixer Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
CDSM[1:0]		RCDMOD[2:0]			LCDMOD[2:0]		

Table 33. Class-D Input Mixer Control Register Bit Descriptions

Bit Name	Description	Settings
CDSM[1:0]	Class-D stereo/mono mode control	x0 = left channel disabled (default) x1 = left channel enabled (left and right) 0x = right channel disabled (default) 1x = right channel enabled (left and right)
RCDMOD[2:0]	Right Class-D input mixer	xx0 = Analog Input A disabled (default) xx1 = Analog Input A enabled x0x = Analog Input B disabled (default) x1x = Analog Input B enabled 0xx = Analog Input C disabled (default) 1xx = Analog Input C enabled
LCDMOD[2:0]	Left Class-D input mixer	xx0 = Analog Input A disabled (default) xx1 = Analog Input A enabled x0x = Analog Input B disabled (default) x1x = Analog Input B enabled 0xx = Analog Input C disabled (default) 1xx = Analog Input C enabled

ALC CONTROL 1, ADDRESS 0x0A

Table 34. ALC Control 1 Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	RECTIME[2:0]			ATTIME[2:0]		

Table 35. ALC Control 1 Register Bit Descriptions

Bit Name	Description	Settings
RECTIME[2:0]	ALC release rate	000 = 4 ms per 0.5 dB step (6 dB/48 ms) 001 = 8 ms 010 = 16 ms 011 = 32 ms 100 = 64 ms 101 = 128 ms (default) 110 = 256 ms 111 = 512 ms
ATTIME[2:0]	ALC attack rate	000 = 32 µs per 0.5 dB step (6 dB/384 µs) 001 = 64 µs 010 = 128 µs 011 = 256 µs (default) 100 = 512 µs 101 = 1 ms 110 = 2 ms 111 = 4 ms

ALC CONTROL 2, ADDRESS 0x0B

Table 36. ALC Control 2 Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
ALCEN	COMP[1:0]		ALCLV_FIX	ALCLV[3:0]			

Table 37. ALC Control 2 Register Bit Descriptions

Bit Name	Description	Settings
ALCEN	ALC enable	0 = ALC disabled (default) 1 = ALC enabled
COMP[1:0]	Compressor setting (see the Soft-Knee Compression section for more information)	00 = Compression Mode 1 (1:4 to 1:∞) 01 = Compression Mode 2 (1:1.7 to 1:4 to 1:∞) 10 = Compression Mode 3 (1:1.3 to 1:2.5 to 1:∞) 11 = Limiter mode (1:∞)
ALCLV_FIX	ALC threshold mode setting	0 = supply tracking (threshold is a constant fraction of supply voltage) 1 = fixed power (threshold is a fixed voltage)
ALCLV[3:0]	ALC threshold level setting	See Table 38

Table 38. ALC Threshold Levels

ALCLV[3:0] Value	Supply Tracking Threshold (% of PVDD) (ALCLV_FIX = 0)	Fixed Power Threshold (V) (ALCLV_FIX = 1)
0000	65	2.74
0001	67	2.89
0010	69	3.04
0011	72	3.19
0100	75	3.34
0101	78	3.50
0110	81	3.65
0111	85	3.80
1000	88	3.95
1001	93	4.10
1010	97	4.25
1011	102	4.40
1100	108	4.56
1101	114	4.71
1110	122	4.86
1111	130	5.01

ALC CONTROL 3, ADDRESS 0x0C

Table 39. ALC Control 3 Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	LCDBOOST	RCDBOOST	SOFTSTART	SOFTCLIPEN	NGEN	NGATE[1:0]	

Table 40. ALC Control 3 Register Bit Descriptions

Bit Name	Description	Settings
LCDBOOST	Left channel Class-D gain boost	0 = 0 dB (default) 1 = +6 dB boost
RCDBOOST	Right channel Class-D gain boost	0 = 0 dB (default) 1 = +6 dB boost
SOFTSTART	Soft start enable	0 = soft start disabled (default) 1 = soft start enabled
SOFTCLIPEN	Soft clip enable	0 = soft clip disabled (default) 1 = soft clip enabled
NGEN	Noise gate enable	0 = noise gate disabled (default) 1 = noise gate enabled
NGATE[1:0]	Noise gate level	00 = 2 mV (default) 01 = 4 mV 10 = 8 mV 11 = 16 mV

POWER-DOWN CONTROL, ADDRESS 0x0D

Table 41. Power-Down Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
PASSPDB	INCPDB	INBPDB	INAPDB	RCDPDB	LCDPDB	HPPDB	PWDB

Table 42. Power-Down Control Register Bit Descriptions

Bit Name	Description	Settings
PASSPDB	Passive switch power-down	0 = power down (default) 1 = power up
INCPDB	Input Channel C power-down	0 = power down (default) 1 = power up
INBPDB	Input Channel B power-down	0 = power down (default) 1 = power up
INAPDB	Input Channel A power-down	0 = power down (default) 1 = power up
RCDPDB	Class-D right channel power-down	0 = power down (default) 1 = power up
LCDPDB	Class-D left channel power-down	0 = power down (default) 1 = power up
HPPDB	Headphone power-down	0 = power down (default) 1 = power up
PWDB	System power-down	0 = power down (default) 1 = power up

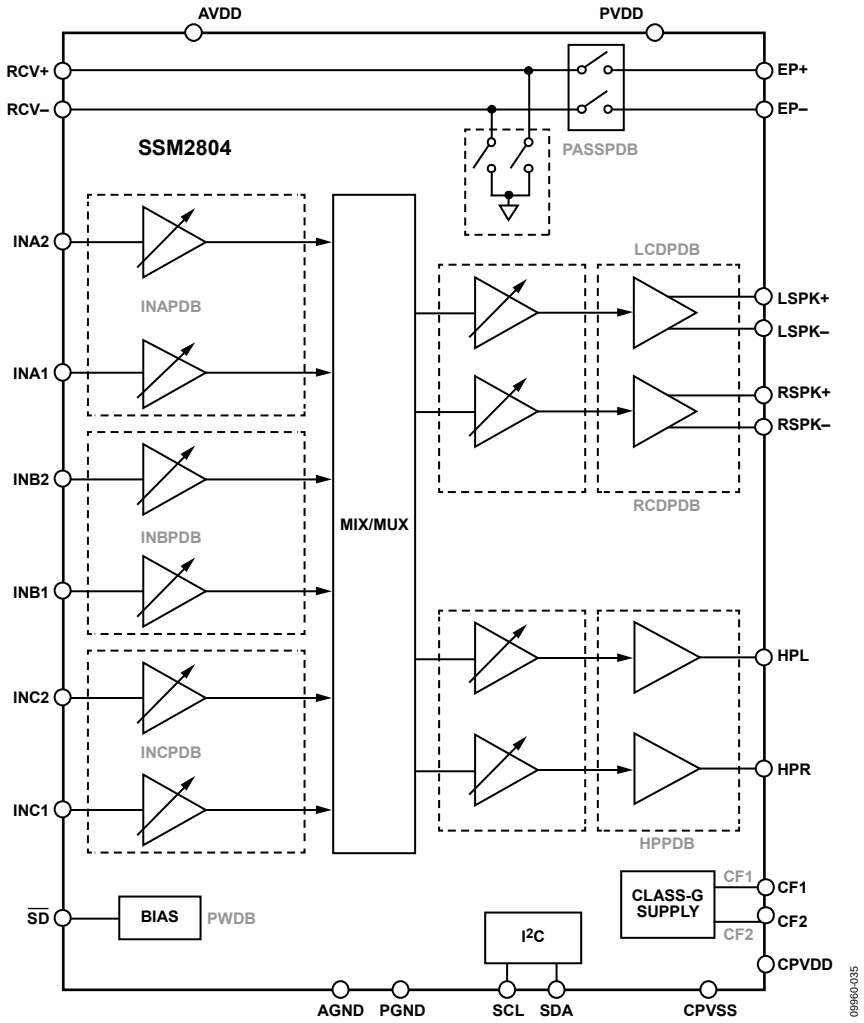

Figure 39. Power Management Control Register Blocks

ADDITIONAL CONTROL, ADDRESS 0x0E

Table 43. Additional Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
LIMLOCK	HPLIM[2:0]			LIM_MODE	TO	EDGE[1:0]	

Table 44. Additional Control Register Bit Descriptions

Bit Name	Description	Settings
LIMLOCK	Headphone limiter lock bit. After the limiter is locked, the locked levels cannot be reset until the SSM2804 is powered down, the $\overline{SD}$ pin is strobed low, or all eight bits of the software reset register (Register 0x10) are set to 0.	0 = disable (default) 1 = enable
HPLIM[2:0]	Headphone limiter level adjust.	000 = off (default) 001 = ±1.13 V 010 = ±0.98 V 011 = ±0.80 V 100 = ±0.57 V 101 = ±0.40 V 110 = ±0.28 V 111 = ±0.22 V
LIM_MODE	Headphone limiter mode selection.	0 = hardware mode (external resistor limiter via $\overline{SD}$ pin; default) 1 = software mode (I^2C adjustable limiter)
TO	Timeout control.	0 = 30 ms (default) 1 = 60 ms
EDGE[1:0]	Class-D output stage edge control.	00 = normal mode (default) 01 = slow edge 10 = slower edge (PVDD > 3.0 V recommended) 11 = slowest edge (PVDD > 4.0 V recommended)

CHIP STATUS REGISTER, ADDRESS 0x0F

This register is read-only.

Table 45. Chip Status Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	OCCD	OCHP	OW	OT

Table 46. Chip Status Register Bit Descriptions

Bit Name	Description	Settings
OCCD	Overcurrent for Class-D	0 = normal 1 = overcurrent
OCHP	Overcurrent for headphone	0 = normal 1 = overcurrent
OW	Overtemperature warning	0 = normal 1 = overtemperature warning
OT	Overtemperature error (thermal shutdown)	0 = normal 1 = overtemperature shutdown

SOFTWARE RESET REGISTER, ADDRESS 0x10

This register is write-only.

Table 47. Software Reset Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
SOFTRESET							

Table 48. Software Reset Register Bit Descriptions

Bit Name	Description	Settings
SOFTRESET	Software reset	00000000 = software reset

OUTLINE DIMENSIONS

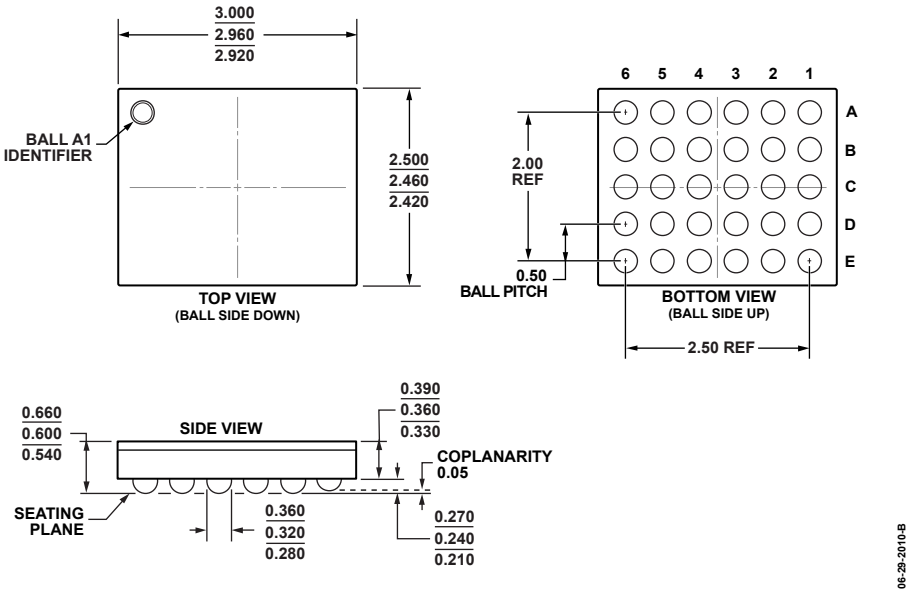

Figure 40. 30-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-30-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2804CBZ-RL	−40°C to +85°C	30-Ball Wafer Level Chip Scale Package [WLCSP]	CB-30-4
SSM2804CBZ-R7	−40°C to +85°C	30-Ball Wafer Level Chip Scale Package [WLCSP]	CB-30-4
EVAL-SSM2804Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D09960-0-7/11(0)

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