CK408 (66/100/133/200 MHz) spread spectrum differential system clock generator

PCK2023

FEATURES

- 3.3 V operation
- Three differential CPU clock pairs
- Ten PCI clocks at 3.3 V
- Six 66 MHz clocks at 3.3 V
- Two 48 MHz clocks at 3.3 V
- One 14.318 MHz reference clock
- 66,100, 133 or 200 MHz operation
- Power management control pins
- CPU clock skew less than 200 ps cycle-to-cycle
- CPU clock skew less than 150 ps pin-to-pin
- 1.5 ns to 3.5 ns delay on PCI pins
- Spread Spectrum capability

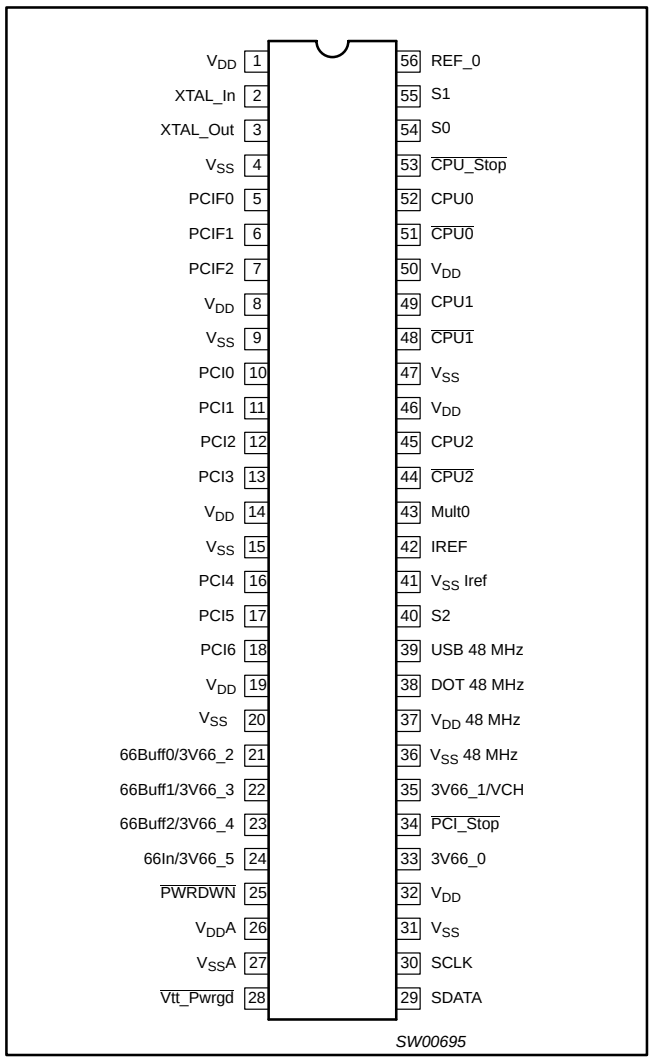
DESCRIPTION

The PCK2023 is a clock synthesizer/driver for a Pentium IV and other similar processors.

The PCK2023 has three differential pair CPU current source outputs. There are ten PCI clock outputs running at 33 MHz and two 48 MHz clocks. There are six 3V66 outputs. Finally, there is one 3.3 V reference clock at 14.318 MHz. All clock outputs meet Intel's drive strength, rise/fall times, jitter, accuracy, and skew requirements.

The part possesses a dedicated power-down input pin for power management control. This input is synchronized on-chip and ensures glitch-free output transitions.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic SSOP	0 to +70 °C	PCK2023DL	SOT371-1
56-Pin Plastic TSSOP	0 to +70 °C	PCK2023DGG	SOT364-1

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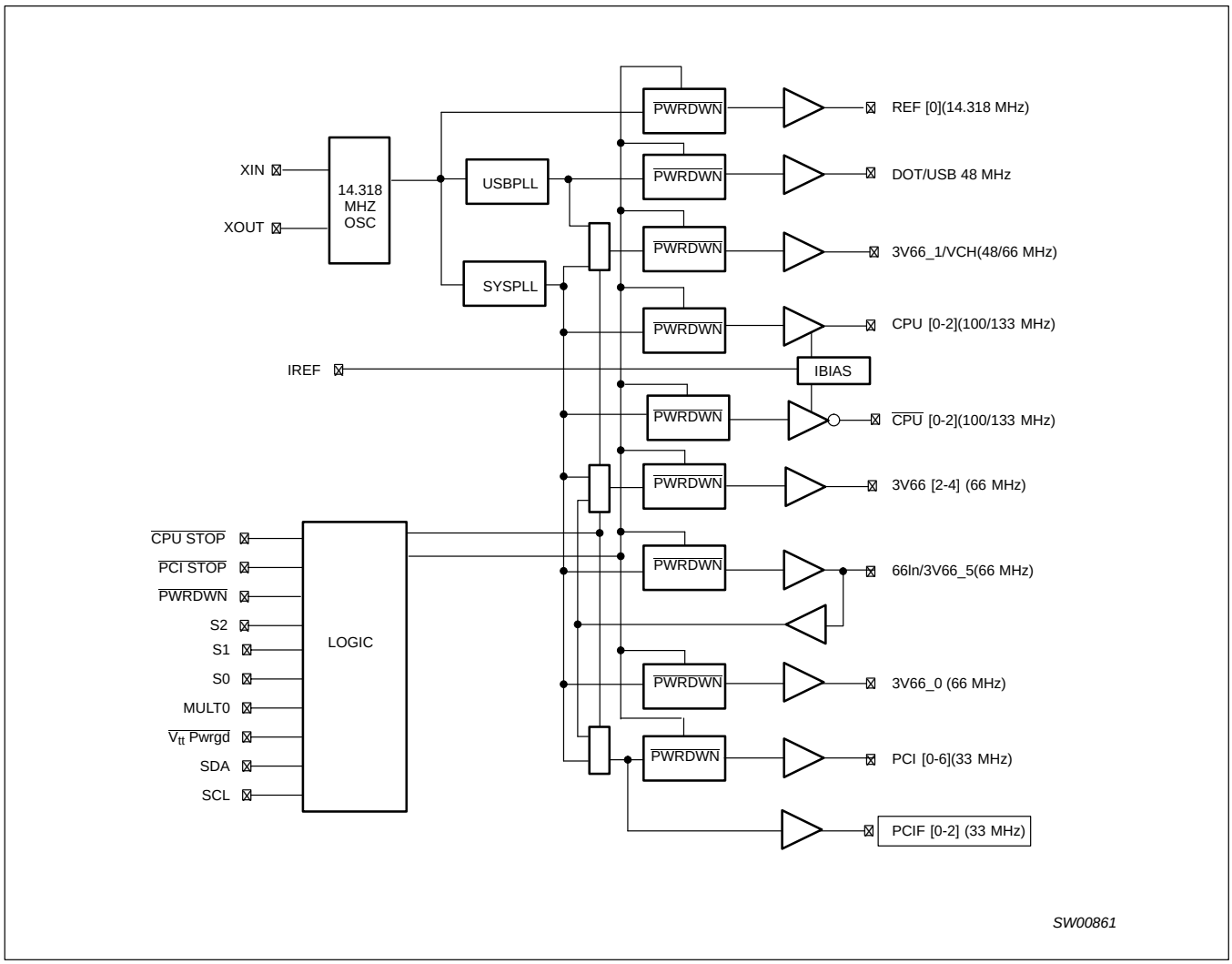
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
56	ref	3.3 V 14.318 MHz clock output.
2	XTAL_In	14.318 MHz crystal input.
3	XTAL_Out	14.318 MHz crystal output.
44, 45, 48, 49, 51, 52	CPU & $\overline{\text{CPU}}$ [2:0]	Differential CPU clock outputs.
33	3V66_0	3.3 V 66 MHz clock output.
35	3V66_1/VCH	3.3 V selectable through I^2C to be 66 MHz or 48 MHz
24	66In/3V66_5	66 MHz input to buffered 66Buff and PCI or 66 MHz clock from internal VCO.
21, 22, 23	66Buff [2:0] / 3V66 [4:2]	66 MHz buffered outputs from 66 input or 66 MHz clocks from internal VCO.
5, 6, 7	PCIF [2:0]	33 MHz clocks divided down from 66 input or divided down from 3V66.
10, 11, 12, 13, 16, 17, 18	PCI [6:0]	PCI clock outputs divided down from 66 input or divided down from 3V66.
39	USB	Fixed 48 MHz clock output.
38	DOT	Fixed 48 MHz clock output.
40	S2	Special 3.3 V 3 level input for mode selection.
54, 55	S1, S0	3.3 V LVTTL inputs for CPU frequency selection.
42	I_{ref}	A precision resistor is attached to this pin which is connected to the internal current reference.
43	Mult0	3.3 V LVTTL input for selecting the current multiplier for the CPU outputs.
25	$\overline{\text{PWRDWN}}$	3.3 V LVTTL input for $\overline{\text{PowerDown}}$ active low.
34	$\overline{\text{PCI\_Stop}}$	3.3 V LVTTL input for $\overline{\text{PCI\_Stop}}$ active low.
53	$\overline{\text{CPU\_Stop}}$	3.3 V LVTTL input for $\overline{\text{CPU\_Stop}}$ active low.
28	$\overline{\text{Vtt\_Pwrgd}}$	3.3 V LVTTL input is a level sensitive strobe used to determine when S [2:0] and Mult0 inputs are valid and ok to be sampled (active low).
29	SDATA	I^2C compatible SDATA.
30	SCLOCK	I^2C compatible SCLOCK.
1, 8, 14, 19, 32, 37, 46, 50	V_{DD}	3.3 V power supply for outputs.
26	$V_{DD}A$	3.3 V power supply for PLL.
4, 9, 15, 20, 31, 36, 41, 47	V_{SS}	Ground for outputs.
27	$V_{SS}A$	Ground for PLL.

BLOCK DIAGRAM



FREQUENCY SELECT/FUNCTION TABLE

S2	S1	S0	CPU	3V66	66BUFF/ 3V66	66In/ 3V66_5	PCIF/PCI	REF 0	USB/DOT	3V66_1/ VCH
1	0	0	66 MHz	66 MHz	66 In	66 input	66 In/2	14.318 MHz	48 MHz	66/48 MHz
1	0	1	100 MHz	66 MHz	66 In	66 input	66 In/2	14.318 MHz	48 MHz	66/48 MHz
1	1	0	200 MHz	66 MHz	66 In	66 input	66 In/2	14.318 MHz	48 MHz	66/48 MHz
1	1	1	133 MHz	66 MHz	66 In	66 input	66 In/2	14.318 MHz	48 MHz	66/48 MHz
0	0	0	66 MHz	66 MHz	66 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz	66/48 MHz
0	0	1	100 MHz	66 MHz	66 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz	66/48 MHz
0	1	0	200 MHz	66 MHz	66 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz	66/48 MHz
0	1	1	133 MHz	66 MHz	66 MHz	66 MHz	33 MHz	14.318 MHz	48 MHz	66/48 MHz
Mid	0	0	Low	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi Z	Hi-Z
Mid	0	1	Tclk/2	Tclk/4	Tclk/4	Tclk/4	Tclk/8	Tclk	Tclk/2	Tclk/4

NOTE:
1. Mid is defined as a voltage level between 1.0 V and 1.8 V for 3 level input functionality. LOW is below 0.8 V. HIGH is above 2.0 V.
2. 3V66_1/VCH output frequency is set by the I^2C.
3. Frequency of the 48 MHz outputs must be +167 ppm to match USB default.
4. Rref output min = 14.316 MHz, nominal = 14.31818, max = 14.32 MHz.
5. Tclk is a test clock over-driven on the XTAL_In input during test mode.

POWER DOWN MODE

$\overline{\text{PWRDWN}}$	CPU	$\overline{\text{CPU}}$	3V66	66BUFF/ 3V66	66In/ 3V66_5	PCIF/PCI	REF 0	USB/DOT	3V66_1/ VCH
1	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal
0	I_{ref}*2	Float	LOW	LOW	LOW	LOW	LOW	LOW	LOW

HOST SWING SELECT FUNCTIONS - CK408

MULT 0	BOARD IMPEDANCE	I_{ref}	I_{OH}	V_{OH} @ 50 W
0	50 Ω	R_{ref} = 221.1% I_{ref} = 5.00 mA	$I_{OH} = 4*I_{ref}$	1.0 V
1	50 Ω	R_{ref} = 475.1% I_{ref} = 2.32 mA	$I_{OH} = 6*I_{ref}$	0.7 V

	CONDITIONS	CONFIGURATION	LOAD	MIN.	MAX.
I_{OUT}	V_{DD} = 3.3 V	All combinations, see Table above	Nominal test load for given configuration	-7% of I_{OH} See Table above	+7% of I_{OH} See Table above
I_{OUT}	V_{DD} = 3.3 V ±5%	All combinations, see Table above	Nominal test load for given configuration	-12% of I_{OH} See Table above	+12% of I_{OH} See Table above

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3 V supply		-0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$	—	-50	mA
V_I	DC input voltage	Note 2	—	—	V
I_{OK}	DC output diode current	$V_O > V_{DD}$ or $V_O < 0$	—	±50	mA
V_O	DC output voltage	Note 2	-0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{DD}	—	±50	mA
T_{stg}	Storage temperature range		-65	+150	°C
P_{tot}	Power dissipation per package plastic medium-shrink (SSOP)	For temperature range: -40 to +125°C above +55°C derate linearly with 11.3 mW/K	—	850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT	NOTES
			MIN	MAX		
V_{DD3}	DC 3.3 V supply voltage		3.135	3.465	V	
AV_{DD}	DC 3.3 V analog supply voltage		3.135	3.465	V	
V_{IH}	3.3 V HIGH-level input voltage		2.0	V_{DD} + 0.3	V	
V_{IL}	3.3 V HIGH-level input voltage		V_{SS} - 0.3	0.8	V	
V_{OL3}	3.3 V LOW-level input voltage	I_{OL} = 1.0 mA	—	0.4	V	
V_{OH3}	3.3 V HIGH-level input voltage	I_{OH} = 1.0 mA	2.4	—	V	
I_{LI}	Input leakage current	$0 < V_{IN} < V_{DD}$	-5	+5	µA	1
f_{ref}	reference frequency, oscillator normal value		14.31818	14.31818	MHz	
C_{IN}	Input pin capacitance		—	5	pF	2
C_{XTAL}	Xtal pin capacitance		13.5	22.5	pF	3
C_{OUT}	Output pin capacitance		—	6	pF	2
L_{PIN}	Pin inductance		—	7	nH	2
T_{amb}	Operating ambient temperature range in free air		0	+70	°C	

NOTES:
1. Input leakage current does not include inputs with pull up or pull down resistors.
2. This is a recommendation, not an absolute requirement.
3. As seen by the crystal. Device is intended to be used with a 17-20 pF AT crystal.

POWER MANAGEMENT

CONDITION	MAXIMUM 3.3 V SUPPLY CONSUMPTION MAXIMUM DISCRETE CAP LOADS, V_{DDL}= 3.465 V ALL STATIC INPUTS = V_{DD3} OR V_{SS}
Power-down mode ($\overline{PWRDWN}$ = 0)	25 mA @ I_{ref} = 2.32 mA 46 mA @ I_{ref} = 5.0 mA
Full active	280 mA

CPU STOP FUNCTIONALITY

$\overline{CPU\_STOP}$	CPU	$\overline{CPU}$	3V66	66BUFF	PCIF/PCI	USB/DOT
1	Normal	Normal	66 MHz	66 input	66 input/2	48 MHz
0	I_{ref}*2	Float	66 MHz	66 input	66 input/2	48 MHz

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS T_{amb} = 0 to +70 °C			UNIT
		V_{DD} (V)	OTHER		MIN	TYP	MAX	
I_{OH}	48 MHz USB, VCH	3.135	V_{OUT} = 1.0 V	Type 3A 12-60 Ω	-29	—	—	mA
		3.465	V_{OUT} = 3.135 V		—	—	-23	
I_{OL}	48 MHz USB, VCH	3.135	V_{OUT} = 1.95 V	Type 3A 12-60 Ω	29	—	—	mA
		3.465	V_{OUT} = 0.4 V		—	—	27	
I_{OH}	48 MHz DOT	3.135	V_{OUT} = 1.0 V	Type 3B 12-60 Ω	-29	—	—	mA
		3.465	V_{OUT} = 3.135 V		—	—	-23	
I_{OL}	48 MHz DOT	3.135	V_{OUT} = 1.95 V	Type 3B 12-60 Ω	29	—	—	mA
		3.465	V_{OUT} = 0.4 V		—	—	27	
I_{OH}	REF, PCI, PCIF, 3V66, 66BUFF	3.135	V_{OUT} = 1.0 V	Type 5 12-55 Ω	-33	—	—	mA
		3.465	V_{OUT} = 3.135 V		—	—	-33	
I_{OL}	REF, PCI, PCIF, 3V66, 66BUFF	3.135	V_{OUT} = 1.95 V	Type 5 12-55 Ω	30	—	—	mA
		3.465	V_{OUT} = 0.4 V		—	—	38	
V_{OL}	CPU/$\overline{CPU}$	V_{SS} = 0.0	R_S = 33.2 Ω R_P= 49.9 Ω	Type X1	0.0	—	0.05	V
$\pm I_I$	Input leakage current	3.365	0 < V_{IN} < V_{DD3}	—	-5	—	5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{DD} or GND	I_O = 0	—	—	10	µA

NOTE:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC characteristics section.

AC CHARACTERISTICS

V_{DD3} = 3.3 V -5%; $f_{crystal}$ = 14.31818 MHz

3V66 66 MHz TIMING REQUIREMENTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0 to +70 °C		UNIT	NOTES
		MIN	MAX		
T_{PERIOD}	period	15.0	15.3	ns	8, 13
t_{HIGH}	HIGH time	4.95	N/A	ns	9
t_{LOW}	LOW time	4.55	N/A	ns	10
t_{RISE}	rise time	0.5	2.0	ns	12
t_{FALL}	fall time	0.5	2.0	ns	12
t_{JITTER}	cycle-to-cycle jitter	—	250	ps	
Edge rate	rising edge rate	1.0	4.0	V/ns	12
Edge rate	falling edge rate	1.0	4.0	V/ns	12
t_{SKEW}	pin-to-pin skew 3V66 [1:0]	0.0	250	ps	
t_{SKEW}	pin-to-pin skew 3V66 [5:2]	0.0	250	ps	
t_{SKEW}	pin-to-pin skew 3V66 [5:0]	0.0	450	ps	

66 MHz BUFFERED TIMING REQUIREMENTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0 to +70 °C		UNITS	NOTES
		MIN	MAX		
t_{RISE}	rise time	0.5	2.0	ns	12
t_{FALL}	fall time	0.5	2.0	ns	12
t_{PD}	propagation delay from 66In to 66BUFF [2:0]	2.5	4.5	ns	
Edge rate	rising edge rate	1.0	4.0	V/ns	12
Edge rate	falling edge rate	1.0	4.0	V/ns	12
t_{SKEW}	66 MHz buffered pin-to-pin skew	0.0	175	ps	

PCIF/PCI AC TIMING REQUIREMENTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0 to +70 °C		UNITS	NOTES
		MIN	MAX		
T_{PERIOD}	period	30.0	N/A	ns	8, 13
t_{HIGH}	HIGH time	12.0	N/A	ns	9
t_{LOW}	LOW time	12.0	N/A	ns	10
t_{RISE}	rise time	0.5	2.0	ns	12
t_{FALL}	fall time	0.5	2.0	ns	12
t_{JITTER}	cycle-to-cycle jitter	—	—	ps	
Edge rate	rising edge rate	1.0	4.0	V/ns	12
Edge rate	falling edge rate	1.0	4.0	V/ns	12
t_{SKEW}	pin-to-pin skew	0.0	500	ps	
t_{PCI}	3V66 [5:0] leads 33 MHz PCI	1.5	3.5	ns	

USB 48 MHz AC TIMING REQUIREMENTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0 to +70 °C		UNITS	NOTES
		MIN	MAX		
T_{PERIOD} (average)	period	nominal = 20.829		ns	
t_{HIGH}	HIGH time	8.094	10.036	ns	
t_{LOW}	LOW time	7.694	9.836	ns	
f	frequency	48.000	48.008	MHz	8
t_{RISE}	rise time	1.0	2.0	ns	12
t_{FALL}	fall time	1.0	2.0	ns	12
t_{JITTER}	cycle-to-cycle jitter	0	350	ps	
Edge rate	rising edge rate	1.0	2.0	V/ns	
Edge rate	falling edge rate	1.0	2.0	V/ns	

DOT 48 MHz AC TIMING REQUIREMENTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0 to +70 °C		UNITS	NOTES
		MIN	MAX		
T_{PERIOD} (average)	period	nominal = 20.829		ns	
t_{HIGH}	HIGH time	8.094	10.036	ns	
t_{LOW}	LOW time	7.694	9.836	ns	
f	frequency	48.000	48.008	MHz	8
t_{RISE}	rise time	0.5	1.0	ns	12
t_{FALL}	fall time	0.5	1.0	ns	12
t_{JITTER}	cycle-to-cycle jitter	—	350	ps	
Edge rate	rising edge rate	2.0	4.0	V/ns	
Edge rate	falling edge rate	2.0	4.0	V/ns	
t_{SKEW}	USB to DOT	—	1000	ps	

CPU 0.7 V AC TIMING REQUIREMENTS

SYMBOL	PARAMETER	CPU 200 MHz		CPU 133 MHz		CPU 100 MHz		CPU 66 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
T_{PERIOD}	average period	5.0	5.1	7.5	7.65	10.0	10.2	15.0	15.3	ns	1, 7
t_{ABSMIN}	absolute minimum host clock period	4.8	—	7.3	—	9.8	—	14.8	—	ns	1, 7
t_{RISE}	rise time	175	600	175	600	175	600	175	600	ps	2, 7, 14
t_{FALL}	fall time	175	600	175	600	175	600	175	600	ps	2, 7, 14
Δt_{RISE}	rise time variation	—	150	—	150	—	150	—	150	ps	2, 7
Δt_{FALL}	fall time variation	—	150	—	150	—	150	—	150	ps	2, 7
V_{CROSS}	absolute crossing point voltages	280	430	280	430	280	430	280	430	mV	7
ΔV_{CROSS}	total variation of V_{CROSS} for rising edge of host	—	90	—	90	—	90	—	90	mV	3, 7
Total ΔV_{CROSS}	total variation of V_{CROSS} over all edges	—	110	—	110	—	110	—	110	mV	4, 7
$t_{CCJITTER}$	cycle-to-cycle jitter	—	150	—	150	—	150	—	150	ps	7, 15
Duty Cycle		45	55	45	55	45	55	45	55	%	7
Overshoot	maximum voltage allowed at output	—	850	—	850	—	850	—	850	mV	7
Undershoot	minimum voltage allowed at output	—	-150	—	-150	—	-150	—	-150	mV	7
t_{SKEW}	pin-to-pin	—	150	—	150	—	150	—	150	ps	

CPU 1.0 V AC TIMING REQUIREMENTS

SYMBOL	PARAMETER	CPU 200 MHz		CPU 133 MHz		CPU 100 MHz		CPU 66 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
T_{PERIOD}	average period	5.0	5.1	7.5	7.65	10.0	10.2	15.0	15.3	ns	1, 15
t_{ABSMIN}	absolute minimum host clock period	4.85	—	7.35	—	9.85	—	14.85	—	ns	1, 15
Diff-t_{RISE}	rise time	175	467	175	467	300	467	300	467	ps	15, 16
Diff-t_{FALL}	fall time	175	467	175	467	175	467	175	467	ps	15, 16
SE Δ_{SKEW}	Absolute single-ended rise/fall waveform symmetry	—	325	—	325	—	325	—	325	ps	17, 18
V_{CROSS}	absolute crossing point voltages	0.51	0.76	0.51	76	0.51	76	—	—	V	18
$t_{CCJITTER}$	cycle-to-cycle jitter	—	150	—	150	—	150	—	150	ps	15, 19
Duty Cycle	—	45	55	45	55	45	55	45	55	%	15
SE-V_{OH}	maximum voltage allowed at output	.92	1.45	.92	1.45	.92	1.45	.92	1.45	V	18
SE-V_{OL}	minimum voltage allowed at output	-200	350	-200	350	-200	350	-200	350	mV	18
Diff-V_{RING_RISE}	rising edge ringback	0.35	—	0.35	—	0.35	—	0.35	—	V	15
Diff-V_{RING_FALL}	falling edge ringback	—	-0.35	—	-0.35	—	-0.35	—	-0.35	V	15

ALL OUTPUTS

SYMBOL	PARAMETER	LIMITS T_{amb} = 0 to +70 °C		UNITS	NOTES
		MIN	MAX		
t_{PZL}/t_{PZH}	output enable delay (all outputs)	1.0	10.0	ns	
t_{PZL}/t_{PZH}	output disable delay (all outputs)	1.0	10.0	ns	
t_{STABLE}	all clock stabilization from power-up	—	3	ms	11

NOTES:
1. Measured at crossing points or where subtraction of CLK-$\overline{CLK}$ crosses 0 V.
2. Measured from V_{OL} = 0.175 V to V_{OH} = 0.525 V.
3. These crossing points refer to only crossing points containing a rising edge of a CPU output (as opposed to a $\overline{CPU}$ output).
4. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
5. Measured from V_{OL} = 0.2 V to V_{OH} = 0.8 V.
6. Determined as a fraction of 2* (t_{RISE}-t_{FALL})/(t_{RISE}+t_{FALL}).
7. Test load is R_S = 33.2 Ω, R_P = 49.9 Ω.
8. Period, jitter, offset and skew measured at rising edge @ 1.5 V for 3.3 V clocks.
9. T_{HIGH} is measured at 2.4 V for non-CPU outputs.
10. T_{LOW} is measured at 0.4 V for all outputs.
11. The time specified is measured from when V_{DDQ} achieves its normal operating level (typical condition V_{DDQ} = 3.3 V) until the frequency output is stable and operating within specification.
12. The 3.3 V clock t_{RISE} and t_{FALL} are measured as a transition through the threshold region V_{OL} = 0.4 V and V_{OH} = 2.4 V (1 mA) JEDEC specification.
13. The average period over any 1 μs period of time must be greater than the minimum specified period.
14. Designed for 150-420 ps (1 V/ns minimum rise time across 0.42 V).
15. Measurement taken from differential waveform.
16. Measurement taken from differential waveform from -0.35 to +0.35 V.
17. Measurements taken from common mode waveforms, measure rise/fall time from 0.41 to 0.86 V. Rise/fall time matching is defined as “the instantaneous difference between maximum CLK rise (fall) and minimum $\overline{CLK}$ fall (rise) time, or minimum CLK rise (fall) and maximum $\overline{CLK}$ fall (rise) time”. This parameter is designed for waveform symmetry.
18. Measured in absolute voltage, single ended.
19. Cycle-to-cycle jitter measurements taken with minimum capacitive loading on non-CPU outputs.

AC WAVEFORMS

V_M = 1.25 V @ V_{DDL} and 1.5 V @ V_{DD3}
$V_X = V_{OL}$ + 0.3 V
$V_Y = V_{OH}$ - 0.3 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

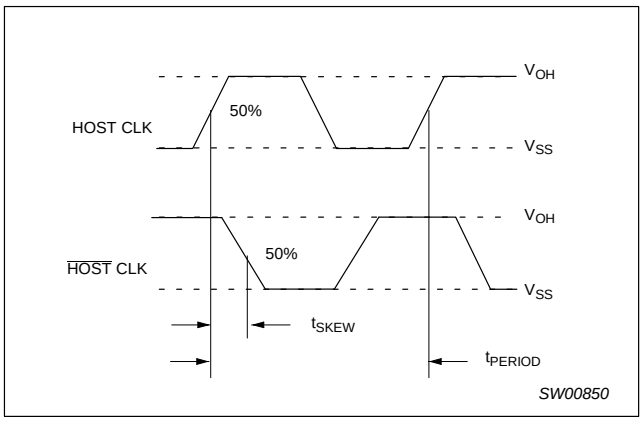


Figure 1. Host clock

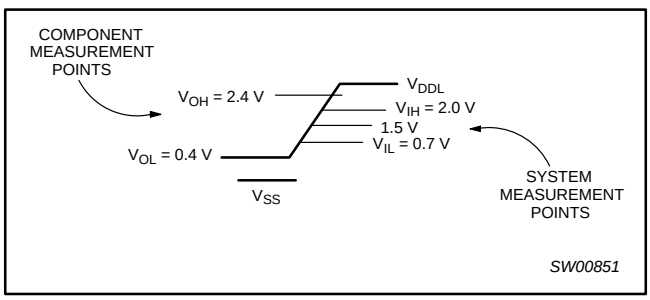


Figure 2. 3.3 V clock waveforms

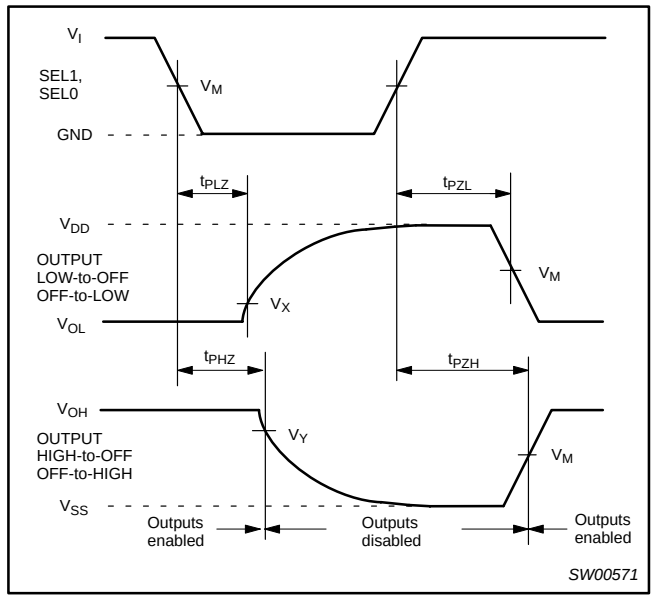


Figure 3. State enable and disable times

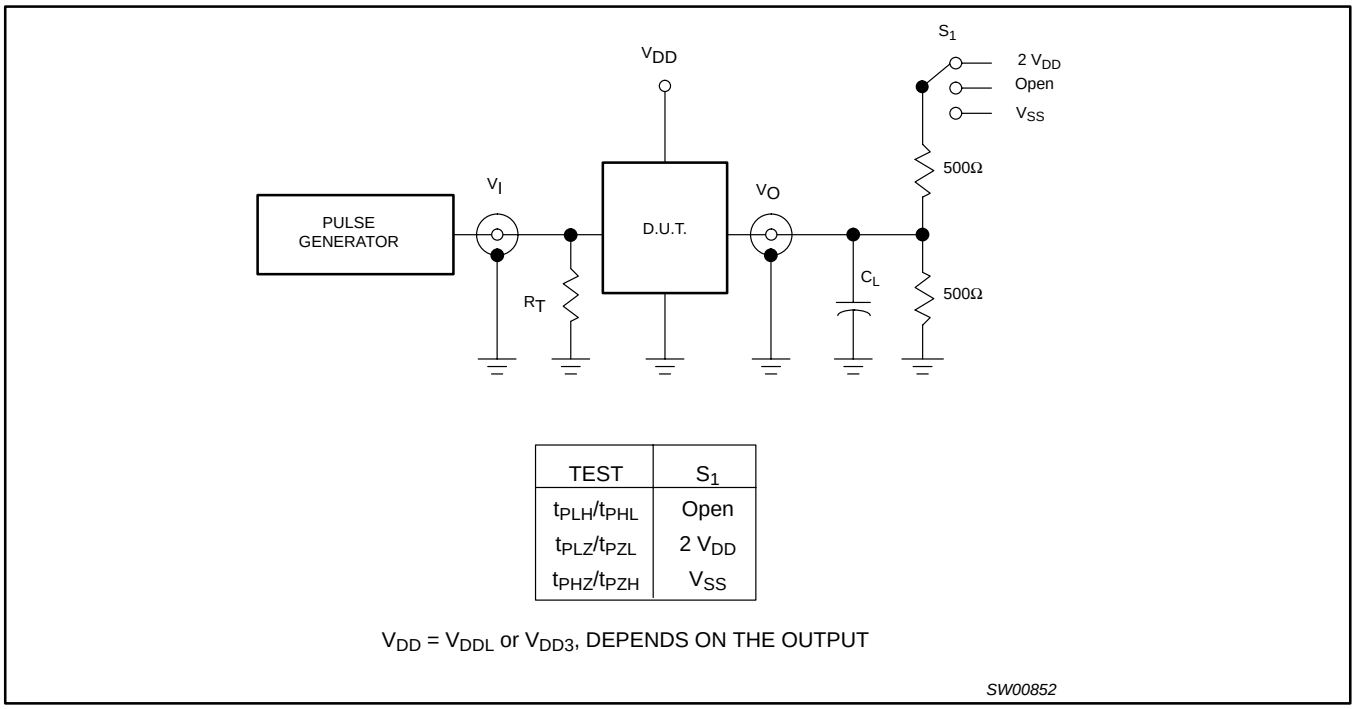


Figure 4. Load circuitry for switching times

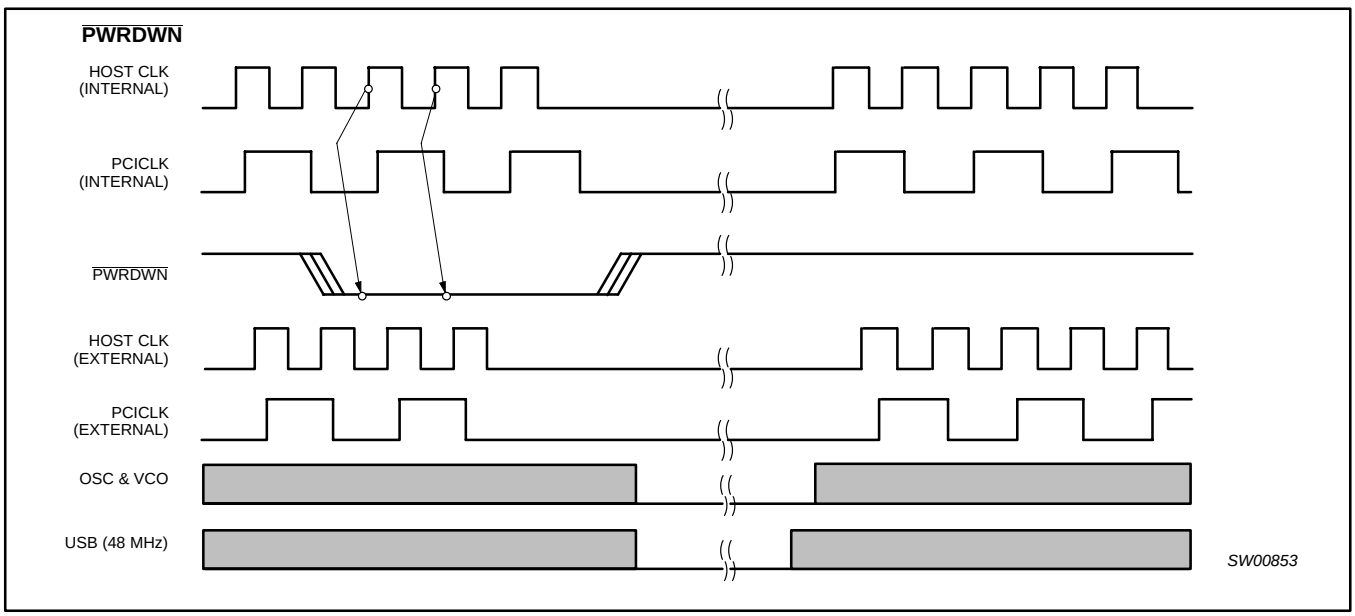


Figure 5. Power management

POWER-UP SEQUENCE

Figure 6 shows the power-up sequence for the PCK2023. Once power is applied to the device, an internal sense circuit generates a signal when the supply is above approximately 2 volts. This signal generates a series of timed signals that control the sequential event inside the device. First, the multifunction pins are latched into the device. These latched signals are then used to define the mode of operation of the device. A short time later, the PLL is enabled and begins running. After XX ms, the clock outputs are enabled and begin running

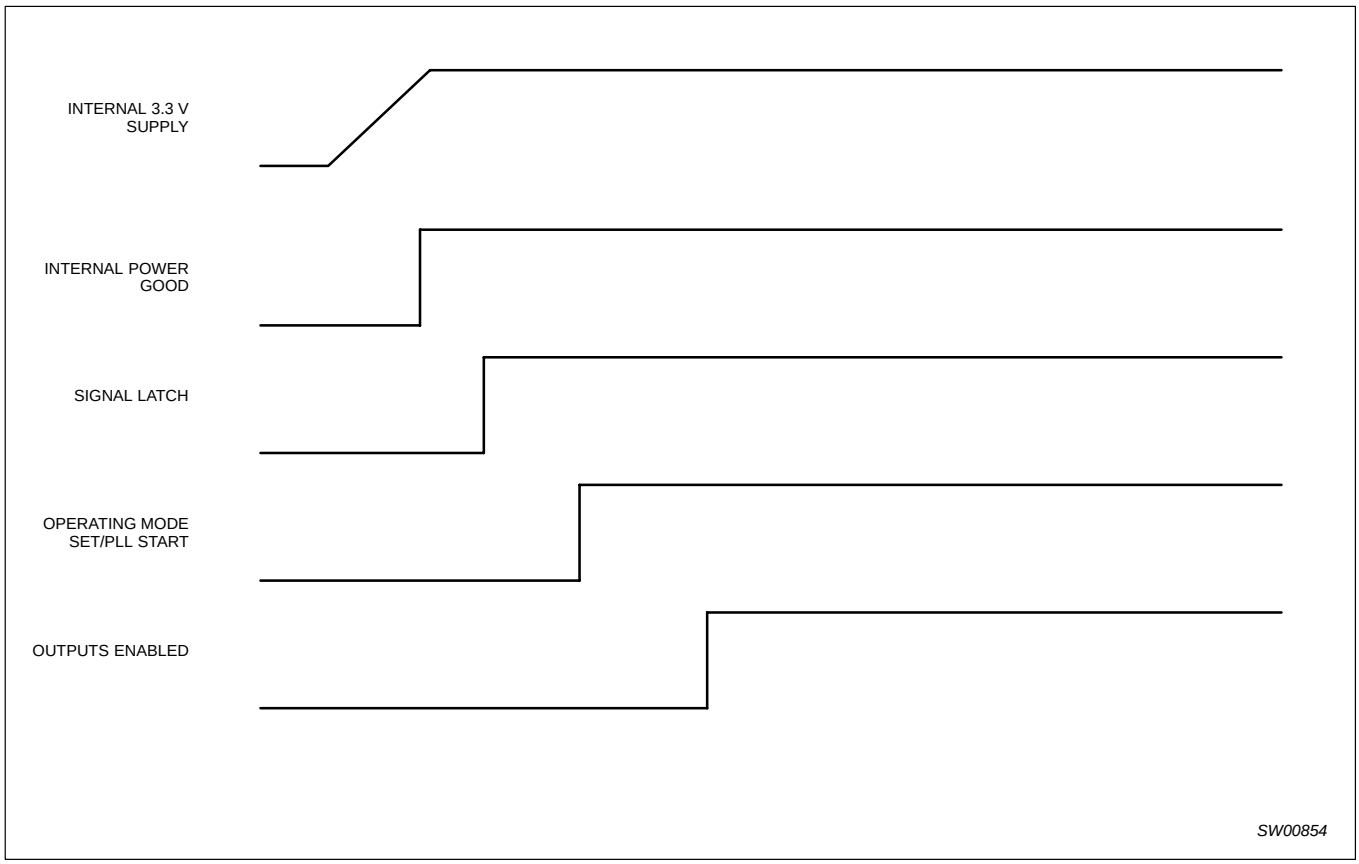


Figure 6. Power-up sequence

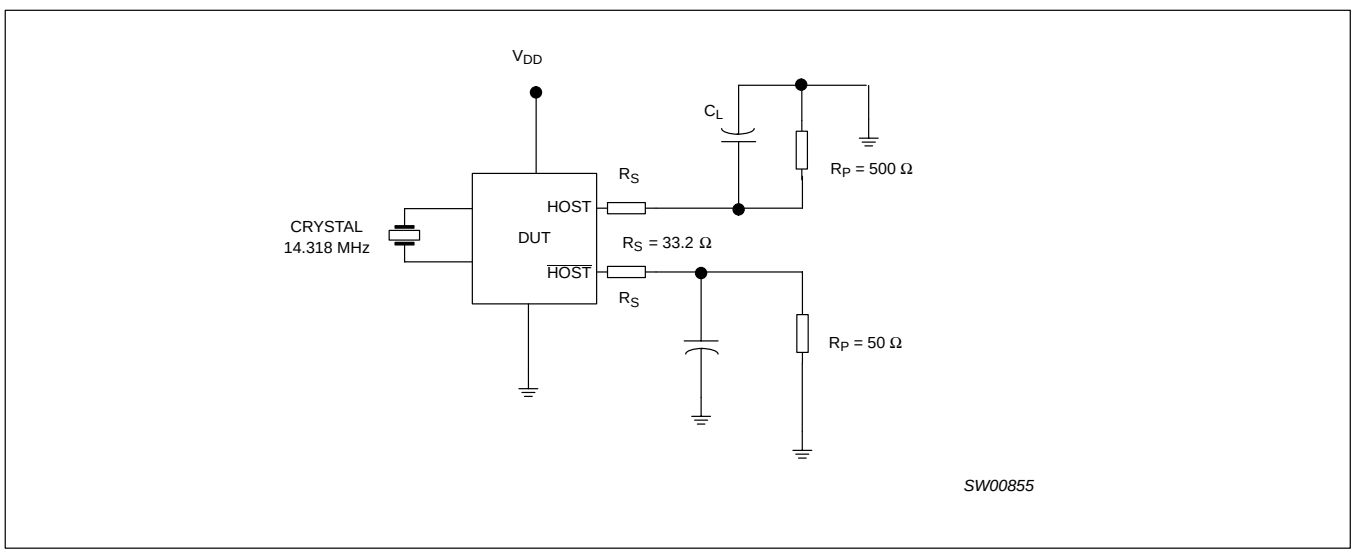


Figure 7. Host clock measurements

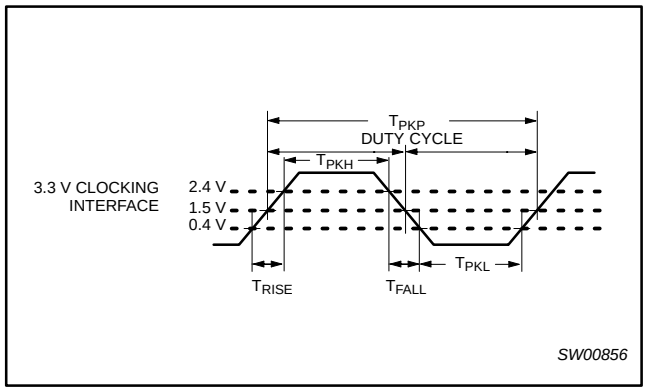


Figure 8. 3.3 V clock waveforms

I²C SPECIFICATION

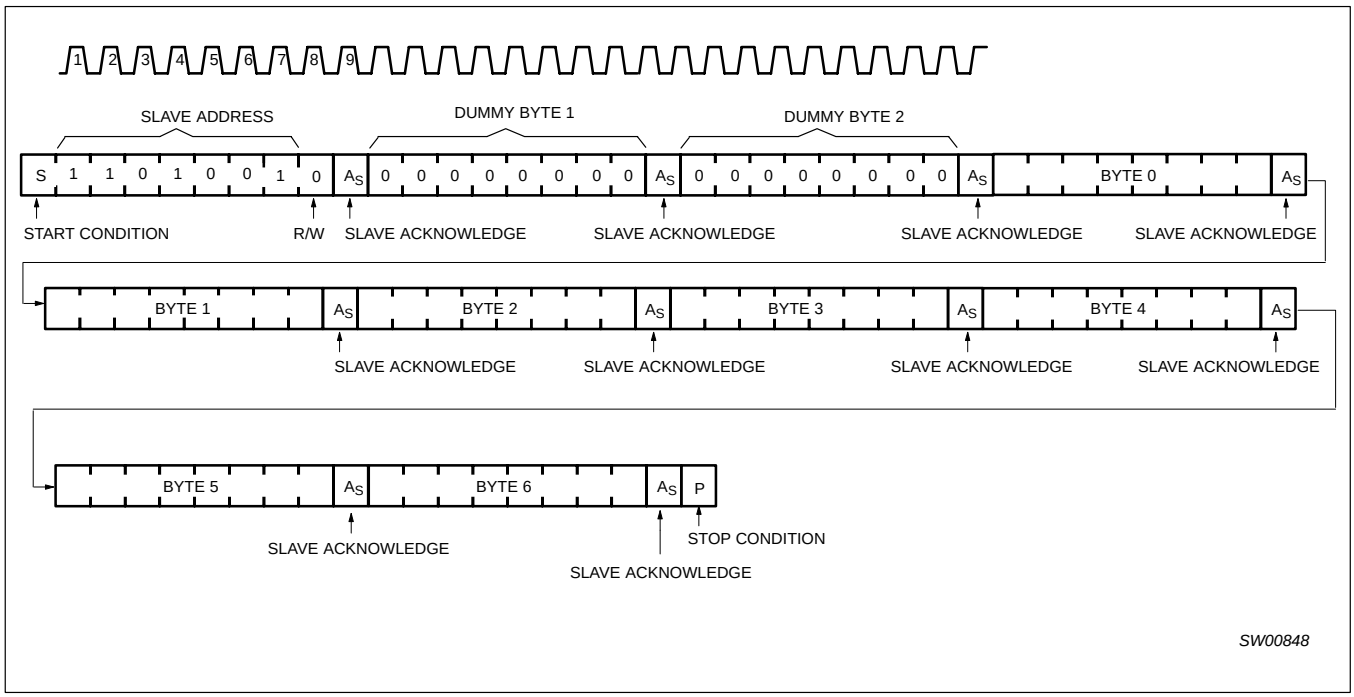


Figure 9. I²C write

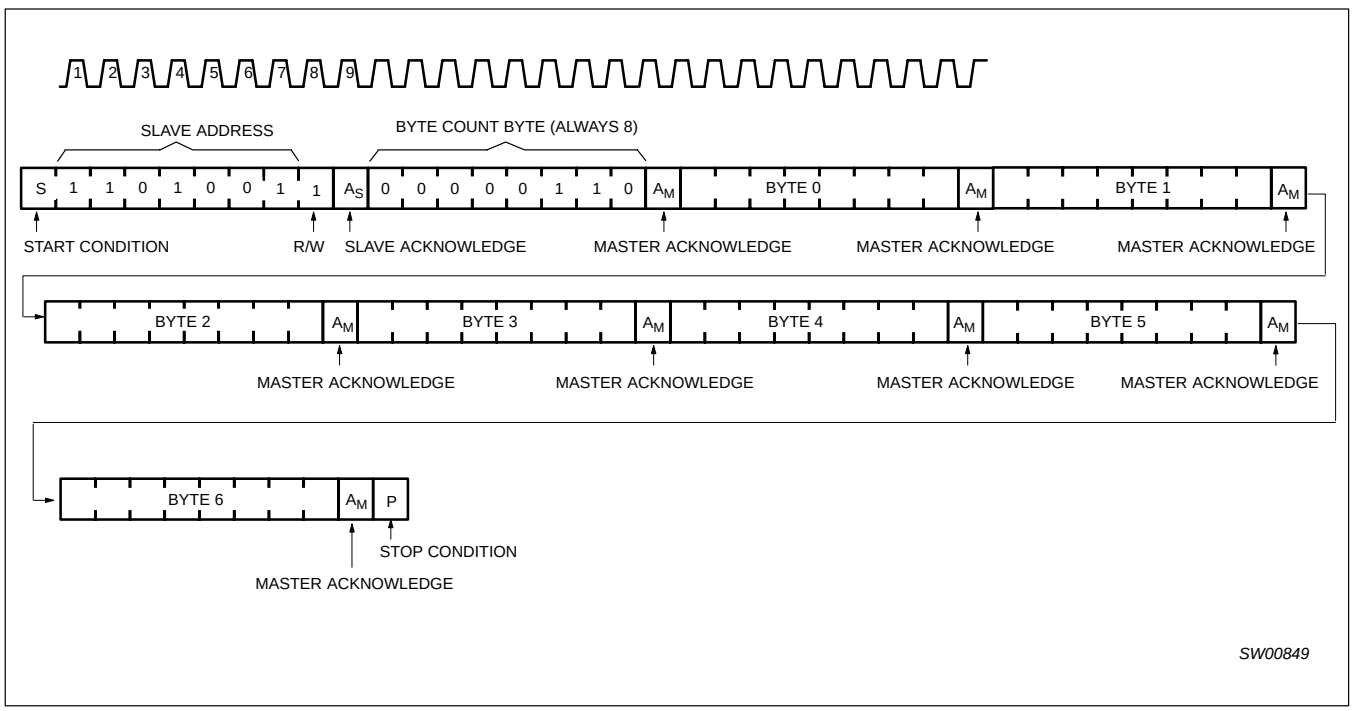


Figure 10. I²C read

BYTE 0

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN AFFECTED	SOURCE PIN
0	S0 reflects the value of the Sel_0 pin sampled on power-up	R	externally selected	N/A	N/A	54
1	S1 reflects the value of the Sel_1 pin sampled on power-up	R	externally selected	N/A	N/A	55
2	S2 reflects the value of the Sel_2 pin sampled on power-up	R	externally selected	N/A	N/A	40
3	PCI_stop. This bit is ANDed with the PCI_STOP pin for I^2C readback and control of PCI outputs	RW	externally selected	All PCI clock outputs except PCI[2:0] pins	10, 11, 12, 13, 16, 17, 18	34
4	CPU_stop reflects the current value of the external $\overline{\text{CPU\_Stop}}$ pin	R	externally selected	All CPU clock pairs	44, 45, 48, 49, 51, 52	53
5	VCH select 66 MHz/48MHz enabled	RW	0 = 66MHz enabled	3V66_1/VCH	35	N/A
6	not used	—	0	—	—	—
7	spread spectrum enabled	RW	0 = spread off	CPU[2:0], 3V66[1:0]	5, 6, 7, 10, 11, 12, 13, 16, 17, 18, 33, 35	N/A

BYTE 1

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN AFFECTED	SOURCE PIN
0	CPU0 output enable 1 = enabled 0 = disabled	RW	1 = enabled	CPU0 $\overline{\text{CPU0}}$	51, 52	N/A
1	CPU1 output enable 1 = enabled 0 = disabled	RW	1 = enabled	CPU1 $\overline{\text{CPU1}}$	48, 49	55
2	CPU2 output enable 1 = enabled 0 = disabled	RW	1 = enabled	CPU2 $\overline{\text{CPU2}}$	44, 45	40
3	allow control of CPU0 with assertion of $\overline{\text{CPU\_Stop}}$ 1 = enabled 0 = disabled	RW	0 = not free running, is affected by $\overline{\text{CPU\_Stop}}$	CPU0 $\overline{\text{CPU0}}$	51, 52	34
4	allow control of CPU1 with assertion of $\overline{\text{CPU\_Stop}}$ 1 = enabled 0 = disabled	RW	0 = not free running, is affected by $\overline{\text{CPU\_Stop}}$	CPU1 $\overline{\text{CPU1}}$	48, 49	53
5	allow control of CPU2 with assertion of CPU stop 1 = enabled 0 = disabled	RW	0 = not free running, is affected by $\overline{\text{CPU\_Stop}}$	CPU2 $\overline{\text{CPU2}}$	44, 45	N/A
6	not used	—	0	—	—	—
7	CPU Mult0 value sampled at startup	R	externally selected	N/A	N/A	43

BYTE 2

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN AFFECTED	SOURCE PIN
0	PCI0 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI0	10	N/A
1	PCI1 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI1	11	N/A
2	PCI2 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI2	12	N/A
3	PCI3 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI3	13	N/A
4	PCI4 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI4	16	N/A
5	PCI5 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI5	17	N/A
6	PCI6 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	PCI6	18	N/A
7	not used	—	0	N/A	N/A	N/A

BYTE 3

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN AFFECTED	SOURCE PIN
0	PCIF0 output enabled	RW	1 = enabled	PCIF0	5	N/A
1	PCIF1 output enabled	RW	1 = enabled	PCIF1	6	N/A
2	PCIF2 output enabled	RW	1 = enabled	PCIF2	7	N/A
3	allow control of PCIF0 with assertion of $\overline{\text{PCI\_Stop}}$ 0 = free running 1 = stopped with $\overline{\text{PCI\_Stop}}$	RW	0 = free running not affected by $\overline{\text{PCI\_Stop}}$	PCIF0	5	N/A
4	allow control of PCIF1 with assertion of $\overline{\text{PCI\_Stop}}$ 0 = free running 1 = stopped with $\overline{\text{PCI\_Stop}}$	RW	0 = free running not affected by $\overline{\text{PCI\_Stop}}$	PCIF1	6	N/A
5	allow control of PCIF2 with assertion of $\overline{\text{PCI\_Stop}}$ 0 = free running 1 = stopped with $\overline{\text{PCI\_Stop}}$	RW	0 = free running not affected by $\overline{\text{PCI\_Stop}}$	PCIF2	7	N/A
6	USB 48MHz output enabled	RW	1 = enabled	USB 48MHz	39	N/A
7	DOT 48 MHz output enabled	RW	1 = enabled	DOT 48MHz	38	N/A

BYTE 4

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN NUMBER
0	66Buff0/3V66_2 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	66Buff0/3V66_2	21
1	66Buff1/3V66_3 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	66Buff1/3V66_3	22
2	66Buff2/3V66_4 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	66Buff2/3V66_4	23
3	3V66_5 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	3V66_5	24
4	3V66_1/VCH output enabled 1 = enabled 0 = disabled	RW	1 = enabled	3V66_1/VCH	35
5	3V66_0 output enabled 1 = enabled 0 = disabled	RW	1 = enabled	3V66_0	33
6	not used	—	0	—	—
7	not used	—	0	—	—

BYTE 5

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN NUMBER
0	USB edge rate control	RW	0	USB	39
1		RW	0	USB	39
2	DOT edge rate control	RW	0	DOT	38
3		RW	0	DOT	38
4	not used	—	0	—	—
5	not used	—	0	—	—
6	not used	—	0	—	—
7	not used	—	0	—	—

BYTE 6

BIT	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	OUTPUT(S) AFFECTED	PIN NUMBER
0	vendor ID bit 0	R	1	N/A	N/A
1	vendor ID bit 1	R	1	N/A	N/A
2	vendor ID bit 2	R	1	N/A	N/A
3	vendor ID bit 3	R	0	N/A	N/A
4	revision code bit 0	R	0	N/A	N/A
5	revision code bit 1	R	0	N/A	N/A
6	revision code bit 2	R	0	N/A	N/A
7	revision code bit 3	R	0	N/A	N/A

APPLICATION NOTES

Optimum performance of the PCK2023 can only be achieved through correct implementation in the system board. This application note addresses many of the issues associated with integrating the PCK2023 on a system board. Descriptions for circuit board layout and decoupling are provided in this application note.

Circuit board layout

It is possible to generate a circuit board with the proper characteristics using four-layer configuration. Figure 11 shows the layer stack-up. It is critical to keep the clock signals on a plane next to a ground plane to ensure they are ground referenced otherwise the clock signals may experience significant distortion and added jitter. Static signals (such as $\overline{\text{SPREAD}}$, PWRDWN, etc.) can be placed on a layer next to the power plane.

The components associated with the clocks should be placed on the same layer as the PCK2023 IC. This will allow the layout to avoid the use of vias for interconnect, thereby reducing node capacitance and trace inductance. All components should be placed as close to the IC as possible.

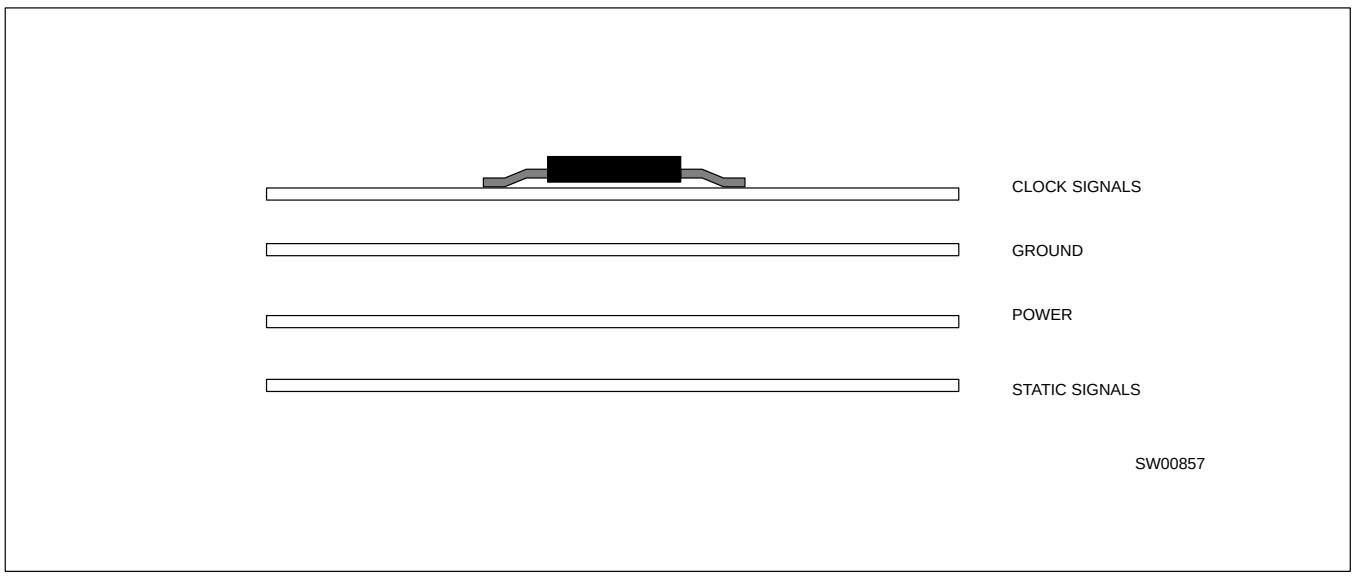


Figure 11. Optimum board layout

Component decoupling

Decoupling is another important consideration to ensure optimum operation of the PCK2023. A first pass decoupling capacitor value may be determined by applying the following equation:

$$C_{bypass} = \frac{1}{2pF_{psw}X_{max}} \text{ where}$$

$$X_{max} = \frac{\Delta V}{\Delta I}$$

$$F_{psw} = \frac{X_{max}}{2pL_{psw}}$$

ΔV is the maximum supply noise permitted (20 mV, for example)

ΔI is the maximum current draw for the clock

L_{psw} is the power supply lead inductance

F_{psw} is the frequency below which the power supply wiring is adequate

The maximum current may be determined by considering the switching of the clock outputs and the capacitive load on these outputs. The following equation may be used to determine the current per output. Once the current for each clock output is determined, they can be summed to determine the total switching current.

$$i = C_{load}\frac{dV}{dt}$$

Most of these values can be determined from the usage in the board design. For example, the IOCLK has a specified edge rate of 1.25 ns typical when slewing between 0.7 and 2.4 volts and the maximum C_{load} is 30 pF. The HOST outputs are a special case since, although the output either drives current or is off, only one drives at a time, so the current is really steered rather than switched. The act of steering the current reduces switching noise on these supplies, therefore the HOST supplies require less decoupling. As a starting point, assume the supply current for each HOST output is equal to 1/2 the programmed output current.

Decoupling capacitors should be located as close to the power pins on the IC as possible. The use of too much decoupling should be avoided since it could cause oscillations on the part because of the LC circuit (the IC leads act as inductors). Also, it is possible to cause oscillations from resonance between the board inductance and board capacitance. Two capacitors may be placed in parallel to effectively extend the capacitance range of the decoupling since the larger capacitor will have a self-resonance at a lower frequency than the smaller capacitor. When using this method, the split between values should be 100 (i.e., 0.1 μF and 0.001 μF).

Another consideration when selecting the decoupling capacitors is the dielectric material of the capacitor. This will depend on the frequency range of concern. For lower frequencies, Z5U material may be used since this type of capacitor has a self-resonance in the 1 MHz to 20 MHz range. Capacitors of NPO have a self-resonance much higher and are more for high frequency decoupling. Consult a capacitor manufacture's datasheet to determine the optimum material type to use.

Additional filtering on the Analog supplies (AV_{DD}) may be used to reduce the noise coupled from the circuit board global V_{DD} to the internal V_{DD} of the PCK2023. One way to do this is to use a PI filter. The specific values should be selected to allow proper decoupling on the pin side while rejecting the digital switching noise. A spectrum analyzer can provide considerable insight to ensure optimum values are selected. Measure the frequency content of the supply on either side of the inductor to verify the values selected reduce the noise on the component side of the filter. To provide the maximum isolation, each AV_{DD} line should have a separate filter since the internal circuitry using these lines have very different switching requirements. In general, pin 26 is strictly a static current draw and should not have any switching noise. Great care has been taken to reduce the sensitivity to supply noise, but there is a finite limit to the capability to do this, therefore added filtering on the board should enhance performance. Pin 46 is used as a supply to the internal PLLs. This node will contain some high frequency switching noise since the internal PLLs operate up to 200 MHz. Again, additional filtering will improve the performance of the part. If a single filter is used for both supplies, noise from the PLL supply (pin 46) can couple int the I_{ref} supply (pin 42) and increase the jitter of the HOST outputs.

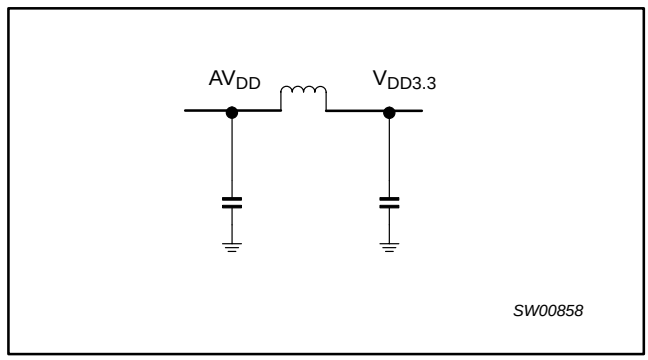


Figure 12. PI filter for all analog V_{DD} lines

I_{ref} decoupling

Filtering on the I_{ref} supply has already been discussed, but additional filtering can be added on the I_{ref} pin (pin 42) to perform additional filtering of the reference current. This reference current is critical to the performance of the HOST outputs since variation in this current is directly proportional to jitter on the HOST outputs. On-die decoupling has been included to reduce noise on this node, but additional decoupling could also be used to further reduce any noise. Care must be taken with this approach to ensure the capacitor and reference resistor share the same ground. Placing both components side by side is an optimum configuration. This external capacitor should not exceed TBD pF to ensure the current source inside the PCK2023 can supply enough charge for this node to reach reference value (1.1 volt).

Functional connection

Figure 13 shows a partial diagram of the PCK2023 in an application. The host outputs are differential current drivers, therefore the output current is converted to a voltage by using some type of load resistor (in this case, R_S and R_P). The output current is based on two, the value of R_{ref} and the setting on MULTSEL0 and MULTSEL1 pins. The I_{ref} pin is actually a reference voltage which is fixed at 1.1 volts, therefore, I_{ref} is $1.1/R_{ref}$. There are limitations on how large the current can be made. This is coupled to the termination resistors used. The maximum voltage which should be observed at the HOST or $\overline{HOST}$ pins of the PCK2023 is 1.1 volts. This value may be determined by using:

$$V_{max} = (R_s + R_P)N_{mult}\frac{1.1}{R_{ref}}$$

where R_S and R_P are the termination resistor values, N_{mult} is the current multiplier set by MULTSEL0 and MULTSEL1, and R_{ref} is the current reference resistor. V_{max} should not exceed 1.1 volts because of the internal current source configuration.

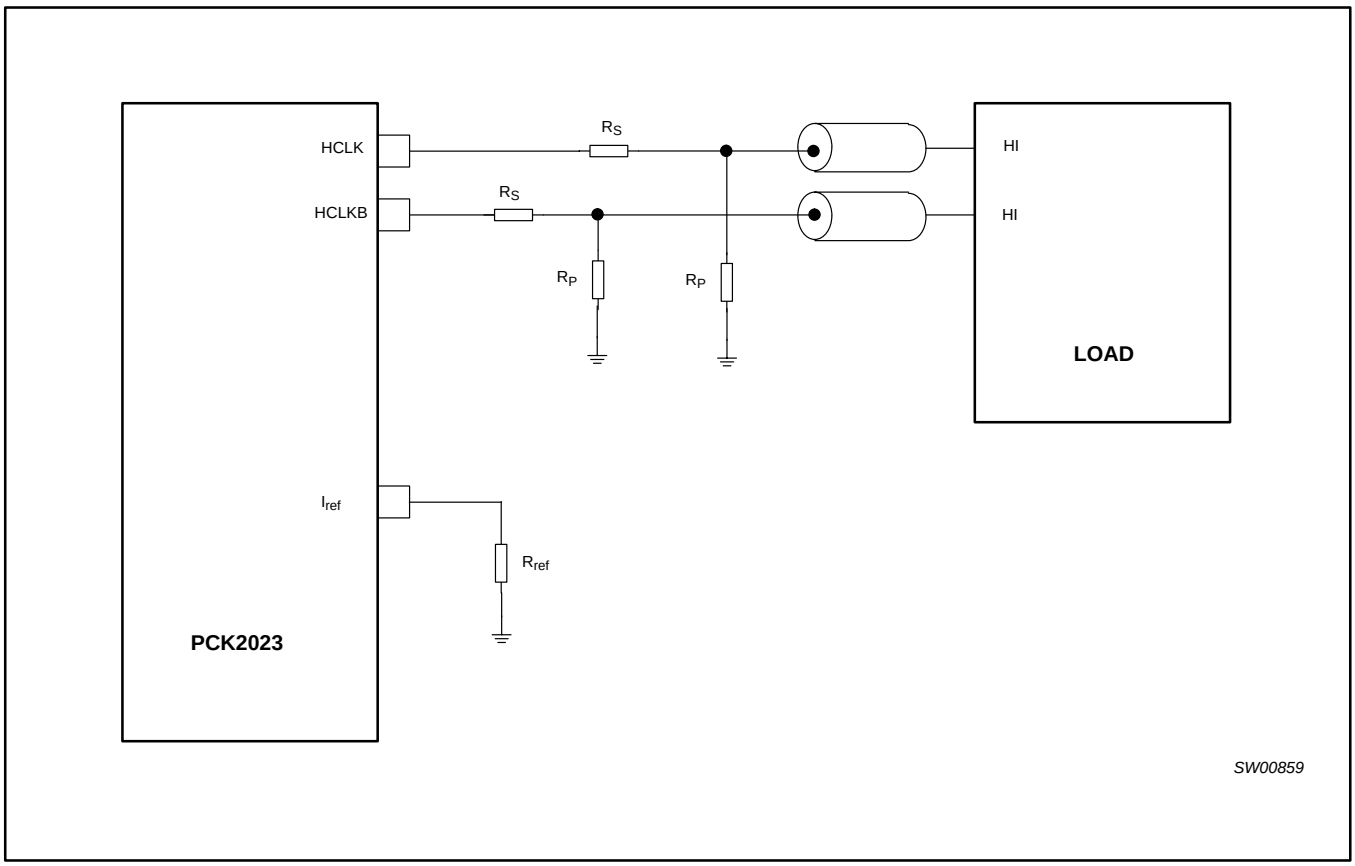


Figure 13. PCK2023 implementation in a circuit board

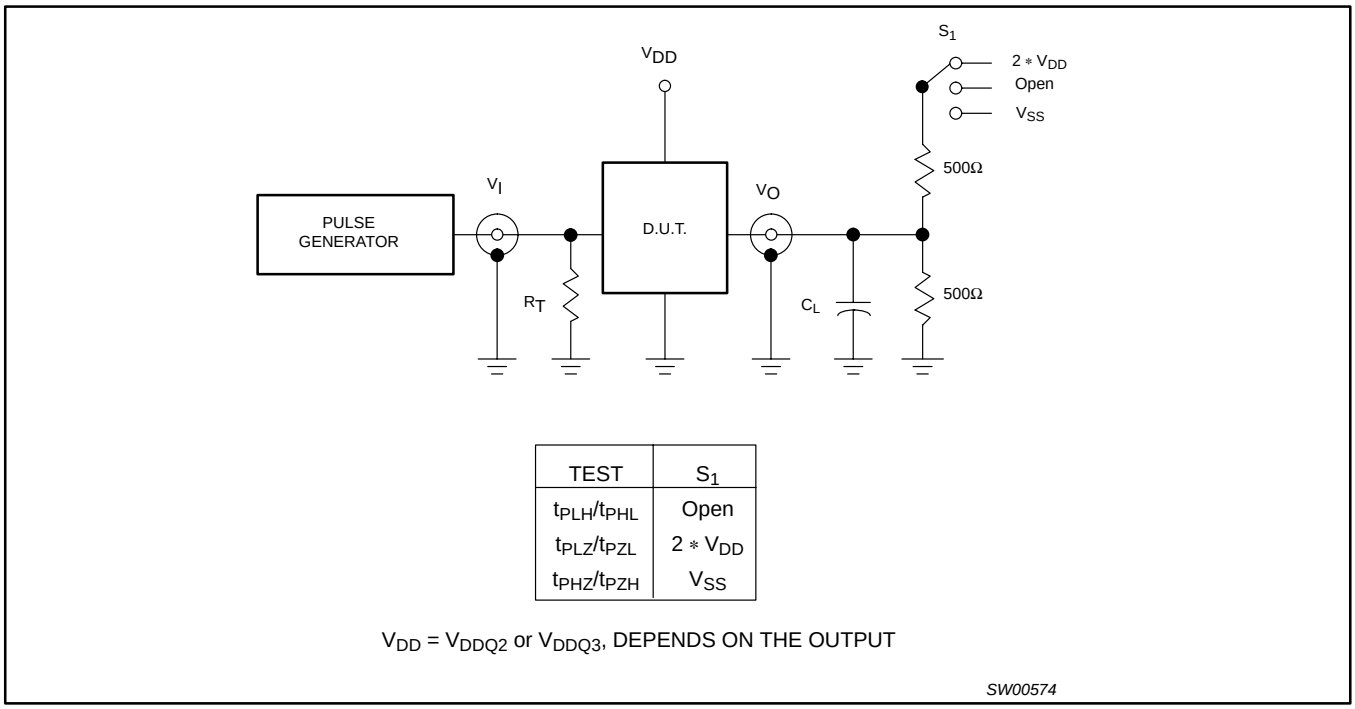


Figure 14. Host clock measurements

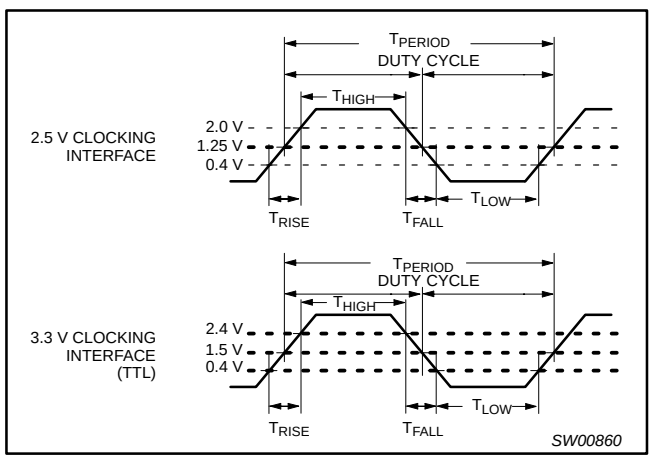


Figure 15. 2.5 V/3.3 V clock waveforms

AC WAVEFORMS

V_M = 1.25 V @ V_{DDL} and 1.5 V @ V_{DD3}
$V_X = V_{OL}$ + 0.3 V
$V_Y = V_{OH}$ - 0.3 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

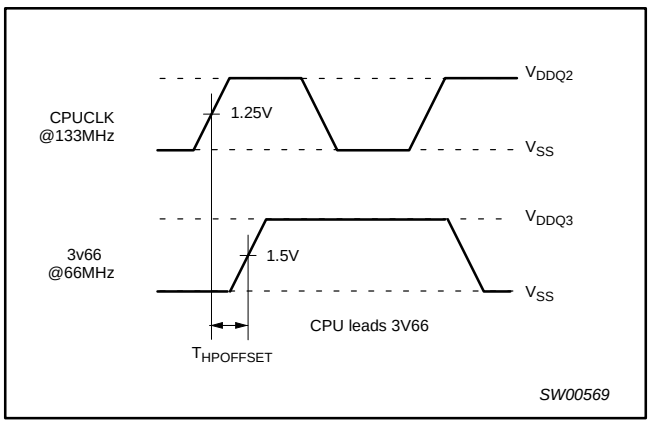


Figure 16. Host clock

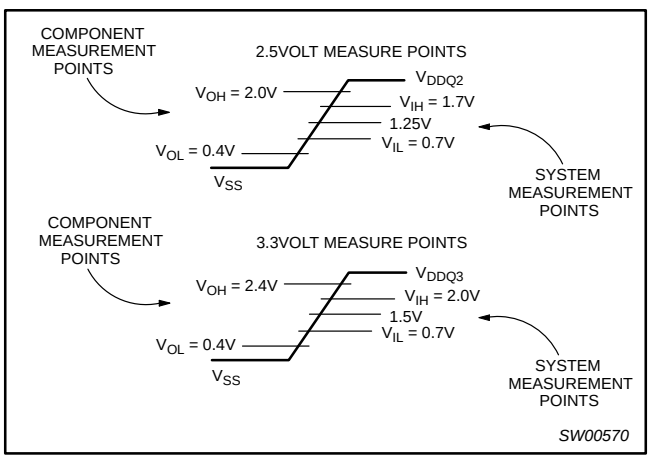


Figure 17. 3.3 V clock waveforms

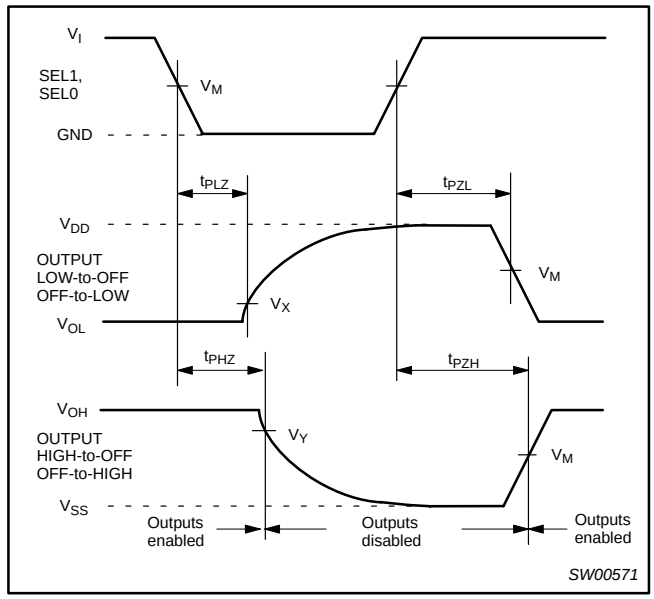


Figure 18. State enable and disable times

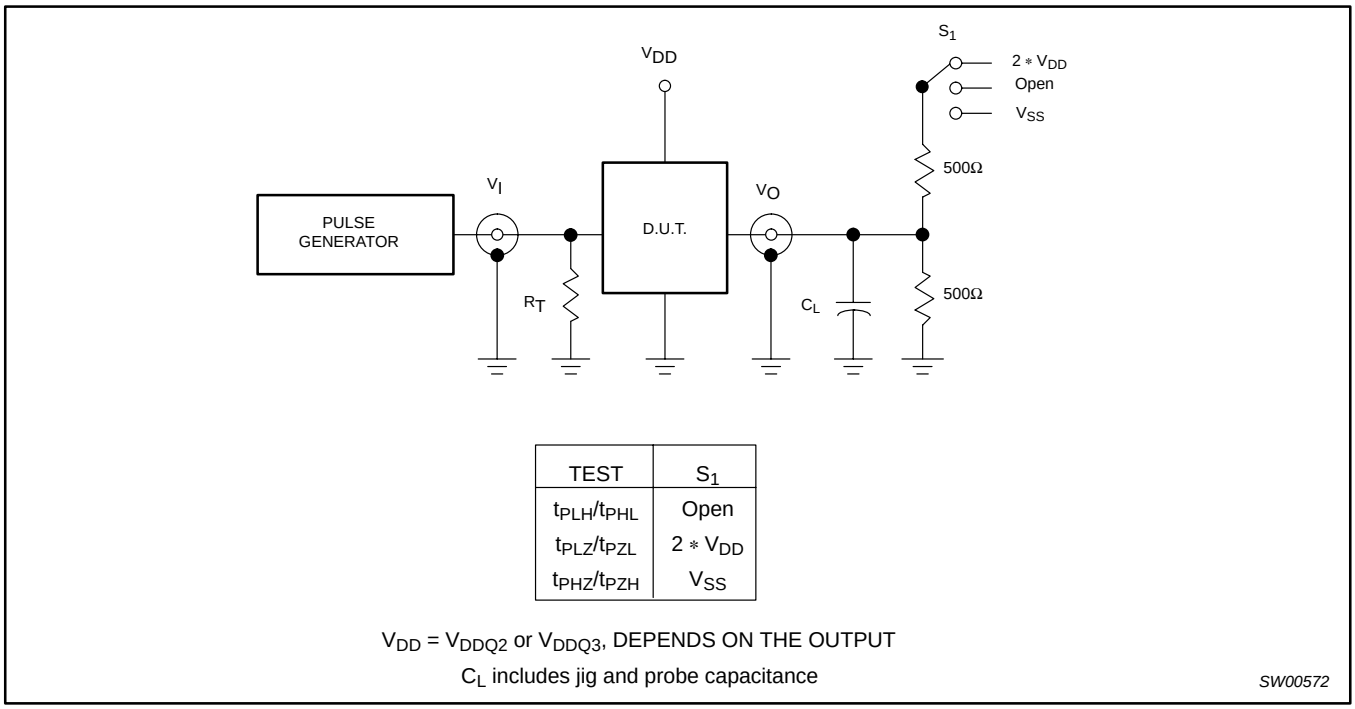


Figure 19. Load circuitry for switching times

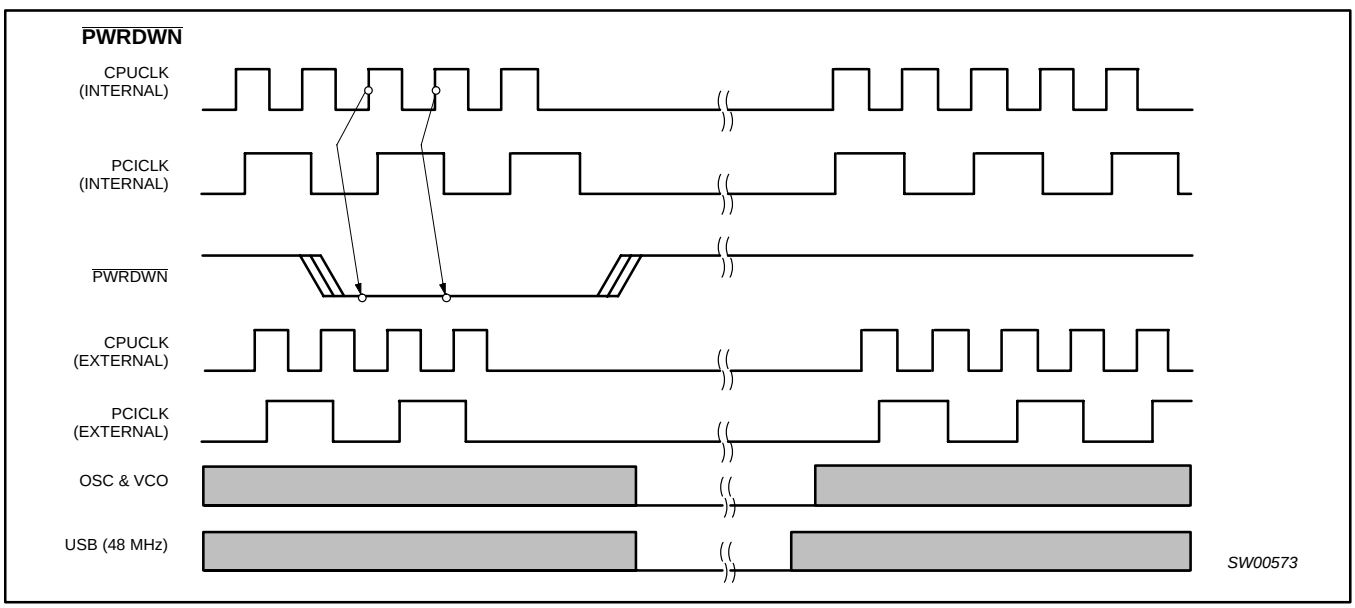
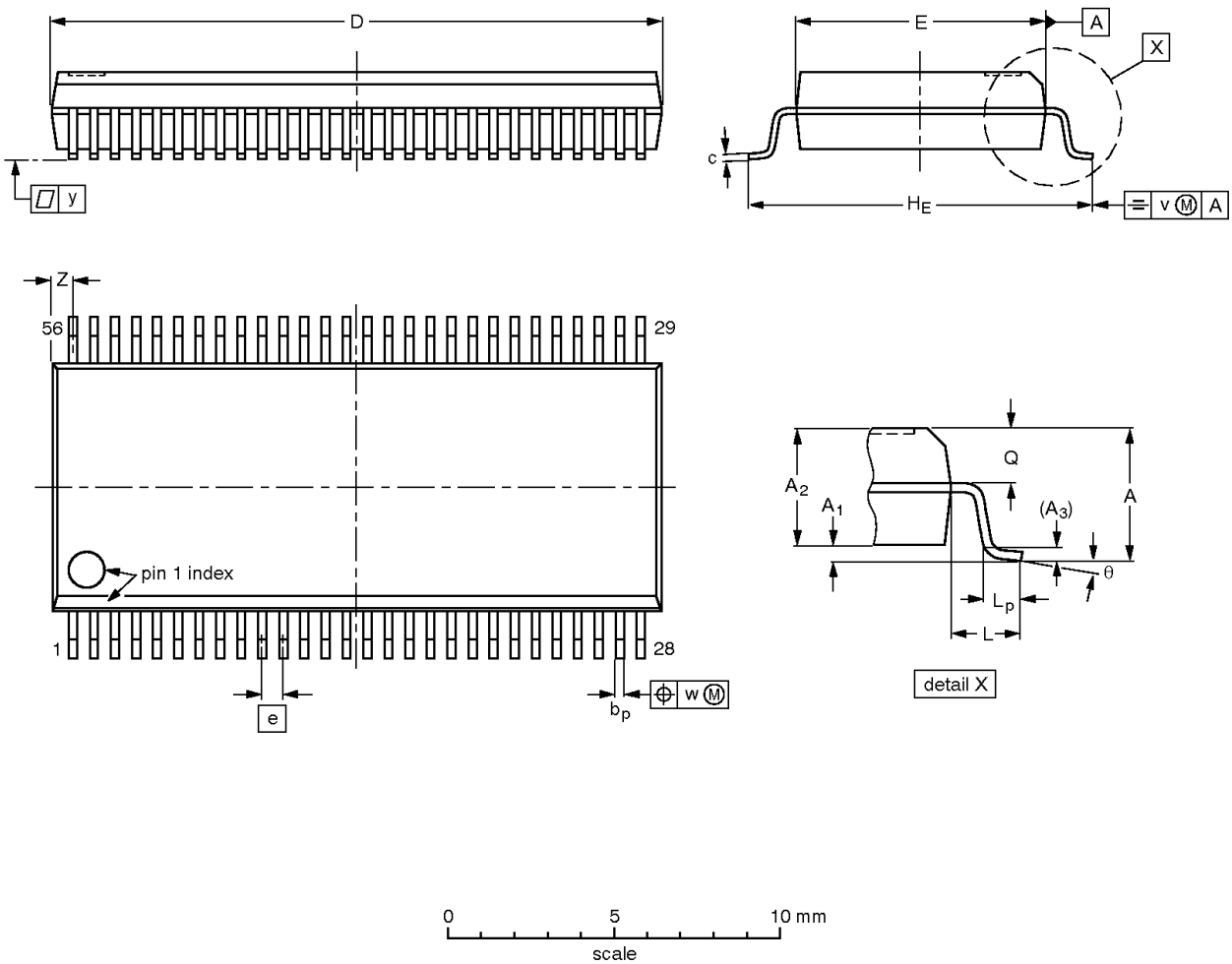


Figure 20. Power management

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

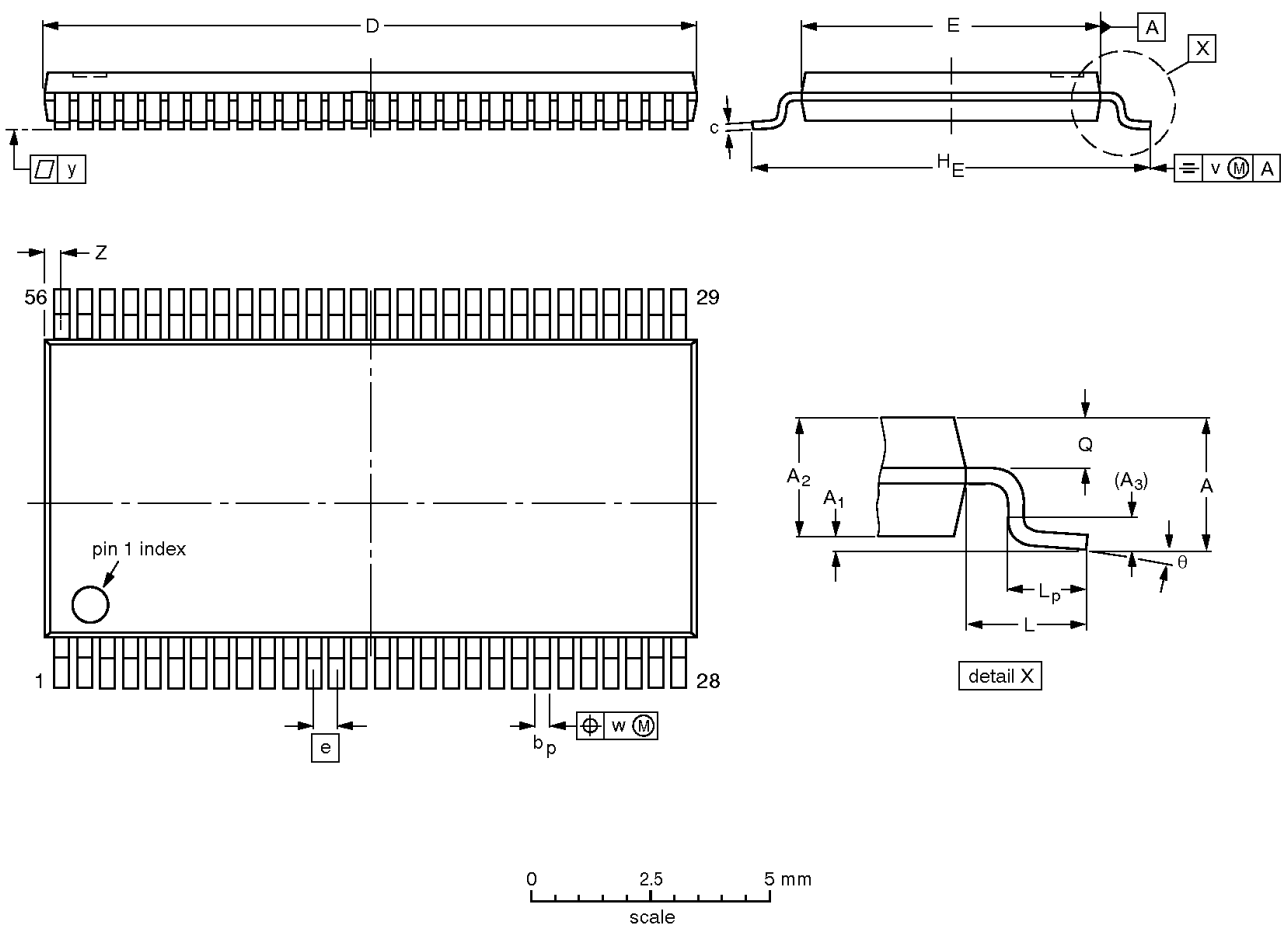
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				~~95-02-04~~ 99-12-27

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153					~~95-02-10~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_2	20030731	**Product data (9397 750 11763); ECN 853-2278 30053 dated 18 June 2003. Supersedes data of 2001 September 07 (9397 750 09142).** Modifications: • Minor changes or corrections to existing product specifications.
_1	20010907	Product data (9397 750 09142); ECN 853-2278 27052 of 07 September 2001.

CK408 (66/100/133/200 MHz) spread spectrum differential system clock generator

PCK2023

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Level	Data sheet status[1]	Product status[2] [3]	Definitions
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