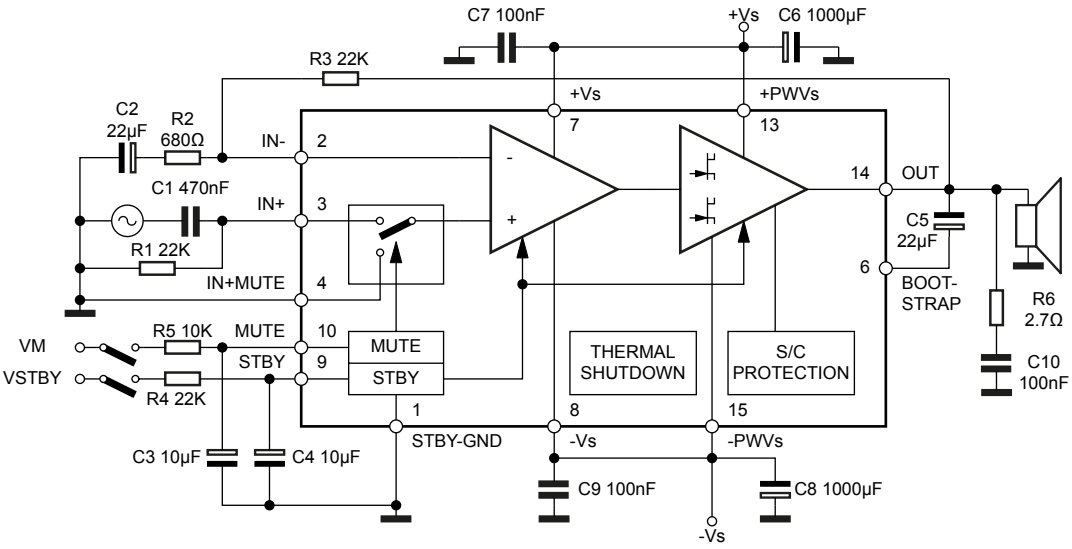
1 Typical application

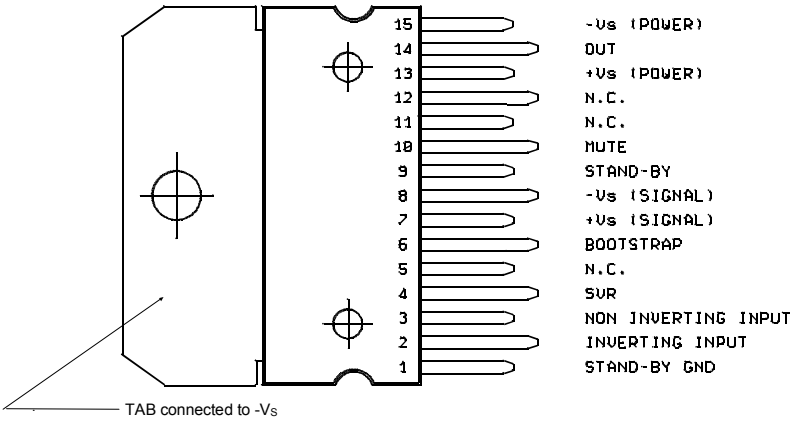
Figure 1. Typical application and test circuit



Note: The Boucherot cell R6, C10, normally not necessary for a stable operation it could be needed in presence of particular load impedances at V_S < ± 25 V.

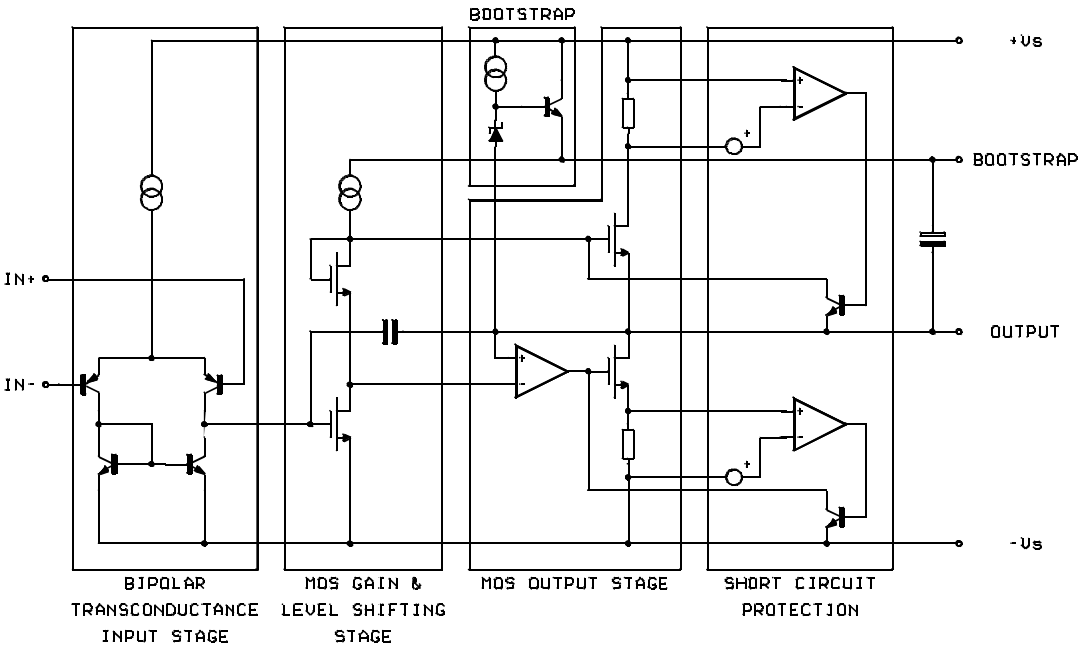
2 Pin connection

Figure 2. **Pin connection (top view)**



3 Block diagram

Figure 3. **Block diagram**



4 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply voltage (no signal)	± 50	V
I_O	Output peak current	10	A
P_{tot}	Total power dissipation (T_{case}= 70 °C)	50	W
T_{op}	Operating ambient temperature range	0 to 70	°C
T_{stg}	Storage temperature	150	°C
T_j	Junction temperature		

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\text{-}jcase}$	Thermal resistance junction-case	1.5	°C/W

5 Electrical characteristics

Refer to the test circuit V_S = ± 35 V, R_L = 8 Ω, G_V = 30 dB; R_g = 50 Ω; T_{amb} = 25 °C, f = 1 kHz; unless otherwise specified.

Table 3. Electrical characteristics

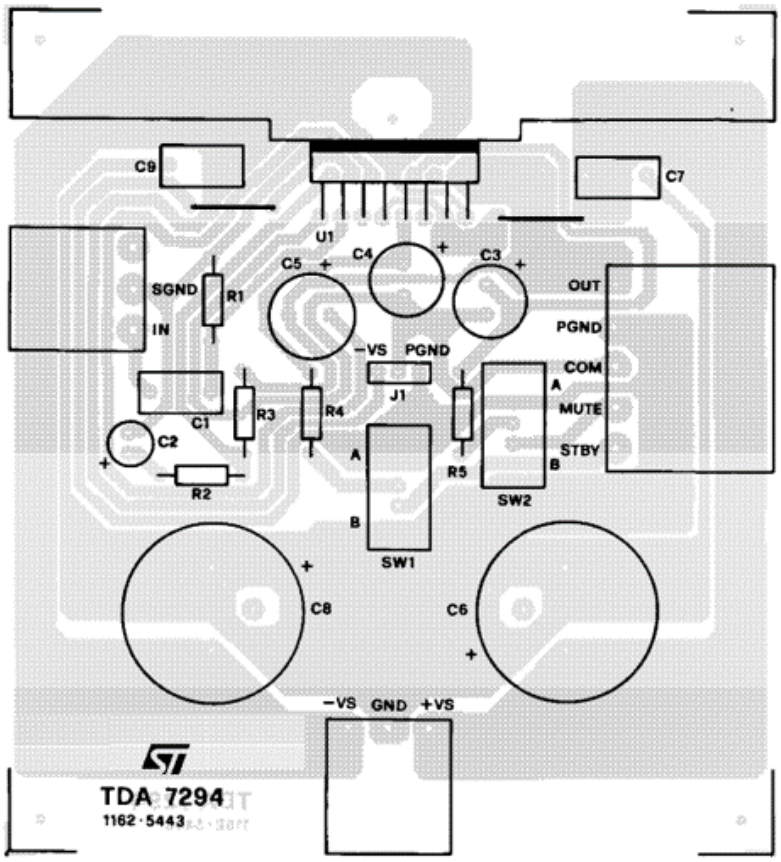
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply range		10		40	V
I_q	Quiescent current		20	30	65	mA
I_b	Input bias current				500	nA
V_{OS}	Input offset voltage				±10	mV
I_{OS}	Input offset current				±100	nA
P_O	RMS continuous output power	d = 0.5%: V_S = ± 35 V, R_L = 8 Ω V_S= ± 31 V, R_L = 6 Ω V_S = ± 27 V, R_L = 4 Ω	 60 60 60	 70 70 70		 W W W
	Music Power (RMS) IEC268.3 RULES - Δt = 1 s (1)	d = 10% R_L = 8 Ω; V_S = ± 38 V R_L = 6 ; V_S = ± 33 V R_L = 4 Ω; V_S = ± 29 V (2)		 100 100 100		 W W W
d	Total harmonic distortion (3)	P_O = 5 W; f = 1 kHz P_O = 0.1 to 50 W; f = 20 Hz to 20 kHz		0.005	 0.1	% %
		V_S = ± 27 V, R_L = 4 Ω P_O = 5 W; f = 1 kHz P_O = 0.1 to 50 W; f = 20 Hz to 20 kHz		 0.01	 0.1	 % %
SR	Slew rate		7	10		V/µs
G_V	Open loop voltage gain			80		dB
	Closed loop voltage gain		24	30	40	dB
e_N	Total input noise	A = curve f = 20 Hz to 20 kHz		1 2	 5	µV
f_L, f_H	Frequency response (-3 dB)	P_O = 1 W	20 Hz to 20 kHz			
R_i	Input resistance		100			kΩ
SVR	Supply voltage rejection	f = 100 Hz; Vripple = 0.5 Vrms	60	75		dB
T_S	Thermal shutdown			145		°C
Stand-by function (Ref: -V_S or GND)						
$V_{ST\ on}$	Stand-by on threshold				1.5	V
$V_{ST\ off}$	Stand-by off threshold		3.5			V
$ATT_{st\text{-}by}$	Stand-by attenuation		70	90		dB
Iq st-by	Quiescent current @ Stand-by			1	3	mA
Mute function (Ref: -V_S or GND)						

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{Mon}	Mute on threshold				1.5	V
V_{Moff}	Mute off threshold		3.5			V
ATT_{mute}	Mute attenuation		60	80		dB

1. *MUSIC POWER CONCEPT - MUSIC POWER is the maximal power which the amplifier is capable of producing across the rated load resistance (regardless of non linearity) 1 sec after the application of a sinusoidal input signal of frequency 1 kHz.*
2. *Limited by the max. allowable current.*
3. *Tested with optimized application board (see Figure 4).*

6 PCB and components

Figure 4. **PCB.and components layout of the circuit of figure below. (1:1 scale)**



Note: The Stand-by and Mute functions can be referred either to GND or -VS.
On the PCB is possible to set both the configuration through the jumper J1.

7 Application suggestion

The recommended values of the external components are those shown on the application circuit of Figure 1. Different values can be used; the following table can help the designer.

COMPONENTS	SUGGESTED VALUE	PURPOSE	LARGER THAN SUGGESTED	SMALLER THAN SUGGESTED
R1 (1)	22 kΩ	INPUT RESISTANCE	INCREASE INPUT IMPEDANCE	DECREASE INPUT IMPEDANCE
R2	680 Ω	CLOSED LOOP GAIN SET TO 30 dB (2)	DECREASE OF GAIN	INCREASE OF GAIN
R3 (1)	22 kΩ		INCREASE OF GAIN	DECREASE OF GAIN
R4	22 kΩ	ST-BYTIME CONSTANT	LARGERST-BY ON/OFF TIME	SMALLER ST-BY ON/OFF TIME; POP NOISE
R5	10 kΩ	MUTE TIME CONSTANT	LARGER MUTE ON/OFF TIME	SMALLER MUTE ON/OFF TIME
C1	0.47 µF	INPUT DC DECOUPLING		HIGHER LOW FREQUENCY CUTOFF
C2	22 µF	FEEDBACK DC DECOUPLING		HIGHER LOW FREQUENCY CUTOFF
C3	10 µF	MUTETIME CONSTANT	LARGER MUTE ON/OFF TIME	SMALLER MUTE ON/OFF TIME
C4	10 µF	ST-BYTIME CONSTANT	LARGERST-BY ON/OFF TIME	SMALLERST-BY ON/OFF TIME; POP NOISE
C5	22 µF	BOOT STRAPPING		SIGNAL DEGRADATION AT LOW FREQUENCY
C6, C8	1000 µF	SUPPLY VOLTAGE BYPASS		DANGER OF OSCILLATION
C7, C9	0.1 µF	SUPPLY VOLTAGE BYPASS		DANGER OF OSCILLATION

1. *R1= R3 for pop optimization.*
2. *Closed loop gain has to be 24 dB.*

8 Typical characteristics

Application circuit of fig 1 unless otherwise specified.

Figure 5. Output power vs. supply voltage (Rl = 8 Ω)

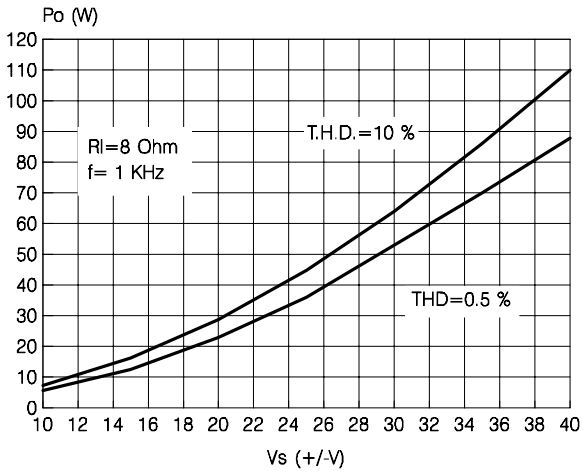


Figure 6. Distortion vs. output power (Rl = 8 Ω)

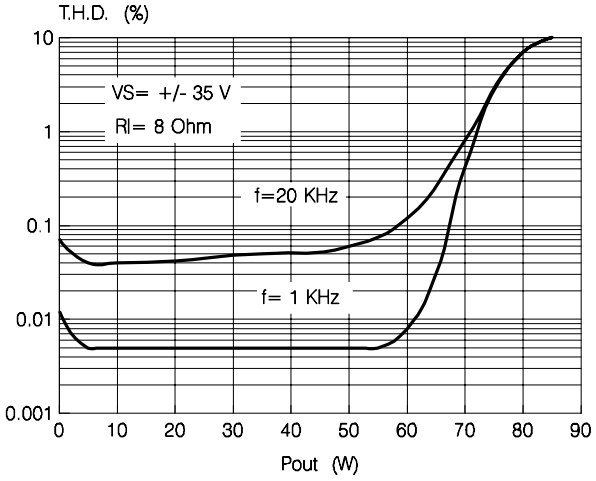


Figure 7. Output power vs. supply voltage (Rl = 4 Ω)

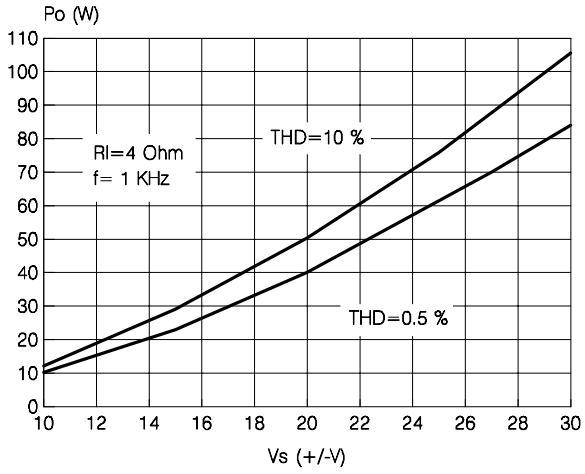


Figure 8. Distortion vs. output power (Rl = 4 Ω)

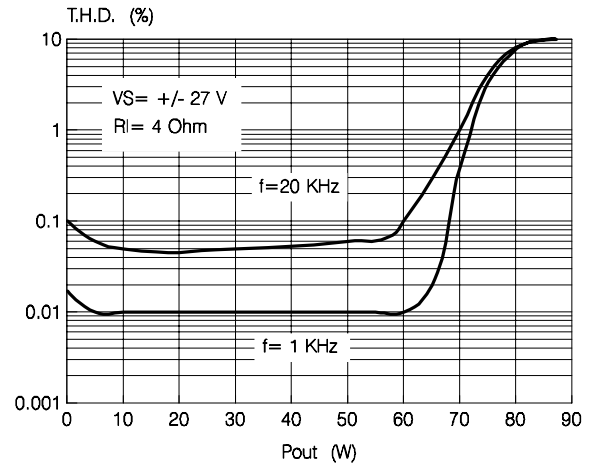


Figure 9. Distortion vs. frequency (Rl = 8 Ω)

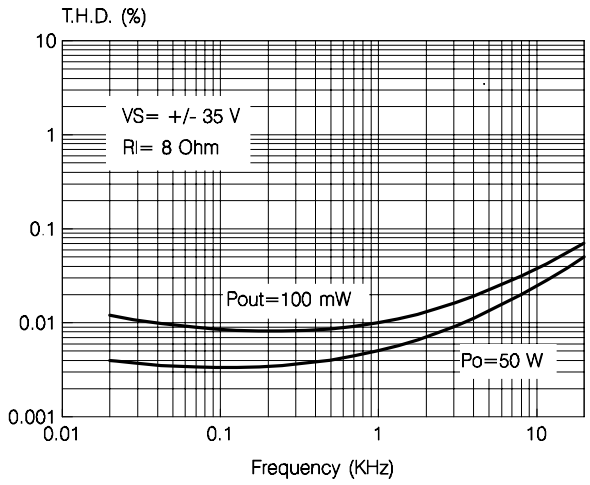


Figure 10. Distortion vs. frequency (Rl = 4 Ω)

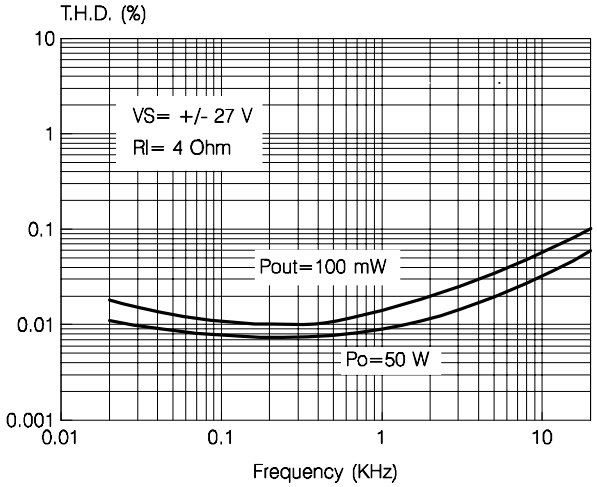


Figure 11. Quiescent current vs. supply voltage

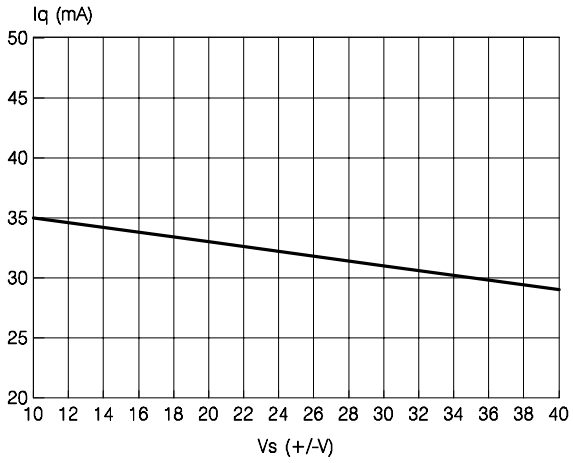


Figure 12. Supply voltage rejection vs. frequency

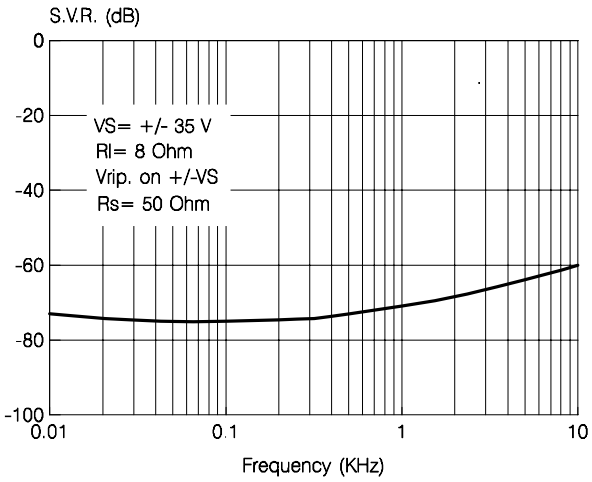


Figure 13. Mute attenuation vs. V_{pin10}

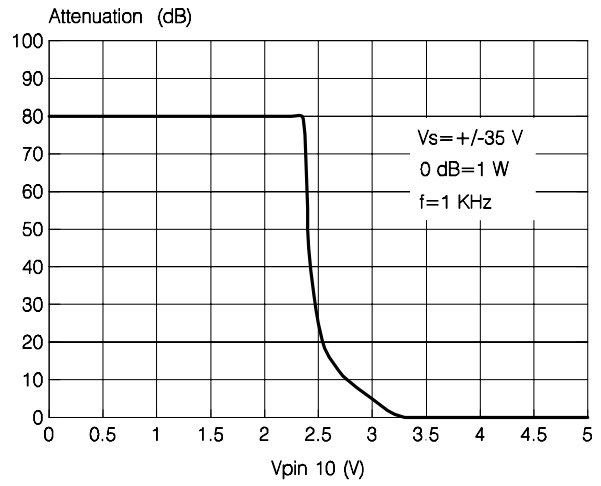


Figure 14. St-by attenuation vs. V_{pin9}

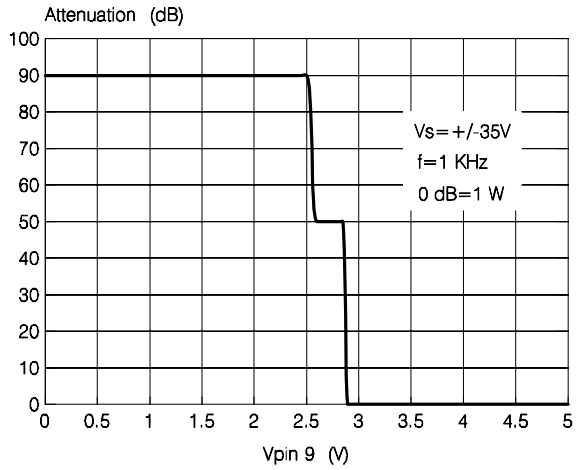


Figure 15. Power dissipation vs. output power (Rl = 4 Ω)

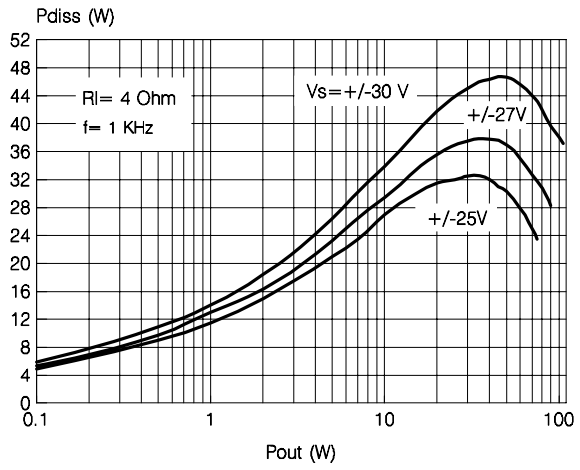
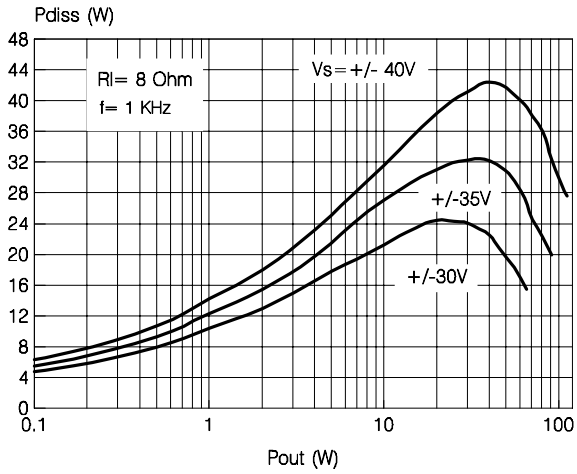


Figure 16. Power dissipation vs. output power (Rl = 8 Ω)



9 Introduction

In consumer electronics, an increasing demand has arisen for very high power monolithic audio amplifiers able to match, with a low cost the performance obtained from the best discrete designs.

The task of realizing this linear integrated circuit in conventional bipolar technology is made extremely difficult by the occurence of 2nd breakdown phenomenon. It limits the safe operating area (SOA) of the power devices, and as a consequence, the maximum attainable output power, especially in presence of highly reactive loads.

Moreover, full exploitation of the SOA translates into a substantial increase in circuit and layout complexity due to the need for sophisticated protection circuits.

To overcome these substantial drawbacks, the use of power MOS devices, which are immune from secondary breakdown is highly desirable.

The device described has therefore been developed in a mixed bipolar-MOS high voltage technology called BCD 100.

9.1 Output stage

The main design task one is confronted with while developing an integrated circuit as a power operational amplifier, independently of the technology used, is that of realizing the output stage.

The solution shown as a principle shematic by Figure 17 represents the DMOS unity-gain output buffer of the TDA7294.

This large-signal, high-power buffer must be capable of handling extremely high current and voltage levels while maintaining acceptably low harmonic distortion and good behaviour over frequency response; moreover, an accurate control of quiescent current is required.

A local linearizing feedback, provided by differential amplifier A, is used to fullfil the above requirements, allowing a simple and effective quiescent current setting.

Proper biasing of the power output transistors alone is however not enough to guarantee the absence of crossover distortion.

While a linearization of the DC transfer characteristic of the stage is obtained, the dynamic behaviour of the system must be taken into account.

A significant aid in keeping the distortion contributed by the final stage as low as possible is provided by the compensation scheme, which exploits the direct connection of the Miller capacitor at the amplifier’s output to introduce a local AC feedback path enclosing the output stage itself.

9.2 Protections

In designing a power IC, particular attention must be reserved to the circuits devoted to protection of the device from short circuit or overload conditions.

Due to the absence of the 2nd breakdown phenomenon, the SOA of the power DMOS transistors is delimited only by a maximum dissipation curve dependent on the duration of the applied stimulus.

In order to fully exploit the capabilities of the power transistors, the protection scheme implemented in this device combines a conventional SOA protection circuit with a novel local temperature sensing technique which " dynamically" controls the maximum dissipation.

Figure 17. **Principle schematic of a DMOS unity-gain buffer**

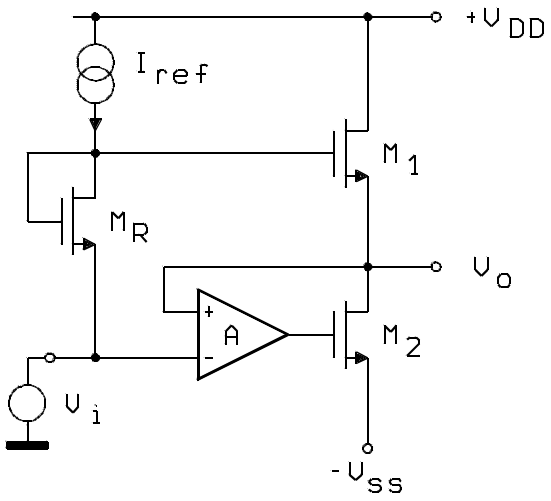
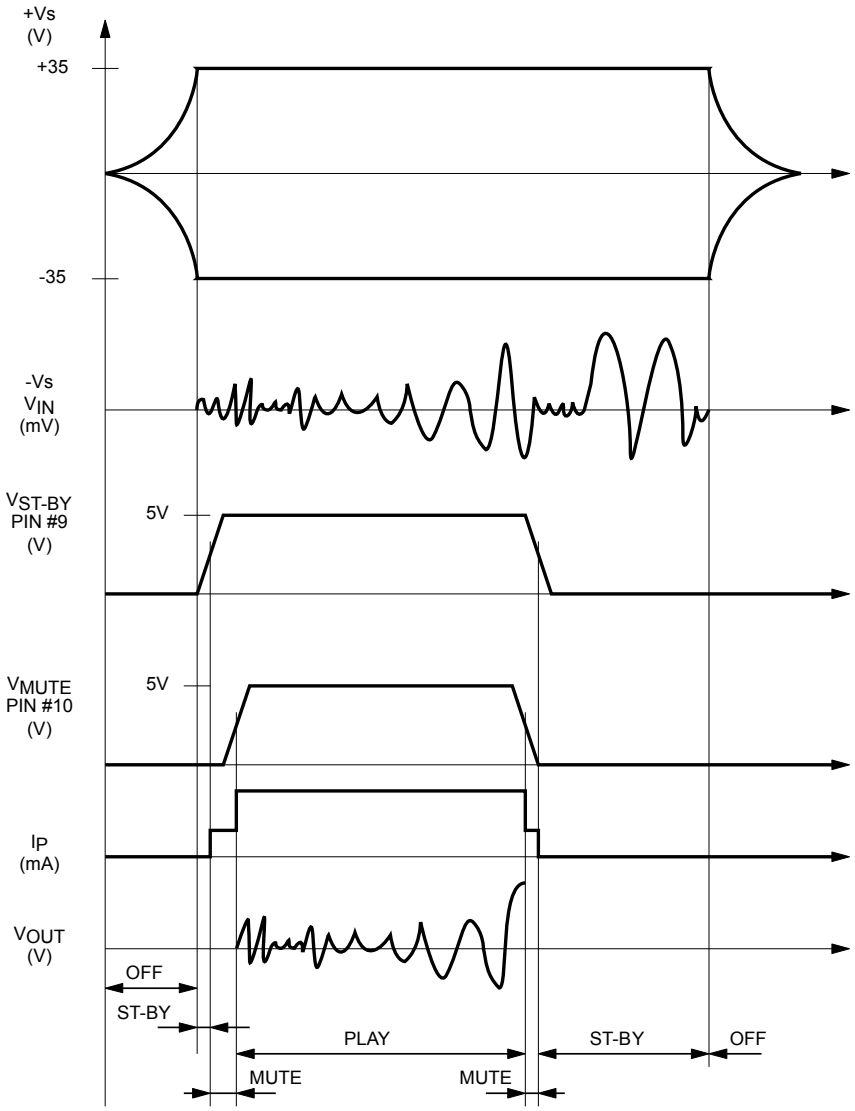


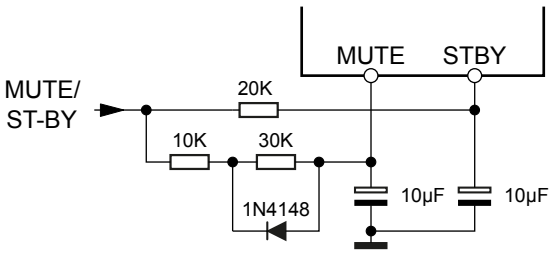
Figure 18. **Turn ON/OFF suggested sequence**



In addition to the overload protection described above, the device features a thermal shutdown circuit which initially puts the device into a muting state (@ T_j = 145 °C) and then into stand-by (@ T_j = 150 °C).

Full protection against electrostatic discharges on every pin is included.

Figure 19. **Single signal ST-BY/MUTE control circuit**



9.3 Other features

The device is provided with both stand-by and mute functions, independently driven by two CMOS logic compatible input pins.

The circuits dedicated to the switching on and off of the amplifier have been carefully optimized to avoid any kind of uncontrolled audible transient at the output.

The sequence that we recommend during the ON/OFF transients is shown by Figure 18.

The application of Figure 19 shows the possibility of using only one command for both st-by and mute functions. On both the pins, the maximum applicable range corresponds to the operating supply voltage.

10 Application information

High-efficiency

Constraints of implementing high power solutions are the power dissipation and the size of the power supply. These are both due to the low efficiency of conventional AB class amplifier approaches.

Here below (Figure 18) is described a circuit proposal for a high efficiency amplifier which can be adopted for both HI-FI and CAR-RADIO applications.

The TDA7294 is a monolithic MOS power amplifier which can be operated at 80 V supply voltage (100 V with no signal applied) while delivering output currents up to ± 10 A.

This allows the use of this device as a very high power amplifier (up to 180 W as peak power with

T.H.D. = 10 % and Rl = 4 Ohm); the only drawback is the power dissipation, hardly manageable in the above power range.

Figure 22 shows the power dissipation versus output power curve for a class AB amplifier, compared with a high efficiency one.

In order to dimension the heatsink (and the power supply), a generally used average output power value is one tenth of the maximum output power at T.H.D. = 10 %.

From Figure 22, where the maximum power is around 200 W, we get an average of 20 W, in this condition, for a class AB amplifier the average power dissipation is equal to 65 W.

The typical junction-to-case thermal resistance of the TDA7294 is 1 °C/W (max= 1.5 °C/W). To avoid that, in worst case conditions, the chip temperature exceedes 150 °C, the thermal resistance of the heatsink must be 0.038 °C/W (@ max ambient temperature of 50 °C).

As the above value is pratically unreachable; a high efficiency system is needed in those cases where the continuous RMS output power is higher than 50-60 W.

The TDA7294 was designed to work also in higher efficiency way.

For this reason there are four power supply pins: intended for the signal part and two for the power part.

T1 and T2 are two power transistors that only operate when the output power reaches a certain threshold (e.g. 20 W). If the output power increases, these transistors are switched on during the portion of the signal where more output voltage swing is needed, thus "bootstrapping" the power supply pins (#13 and #15).

The current generators formed by T4, T7, zener diodes Z1,Z2 and resistors R7, R8 define the minimum drop across the power MOS transistors of the TDA7294. L1, L2, L3 and the snubbers C9, R1 and C10, R2 stabilize the loops formed by the "bootstrap" circuits and the output stage of the TDA7294.

Figure 20. **High efficiency application circuit**

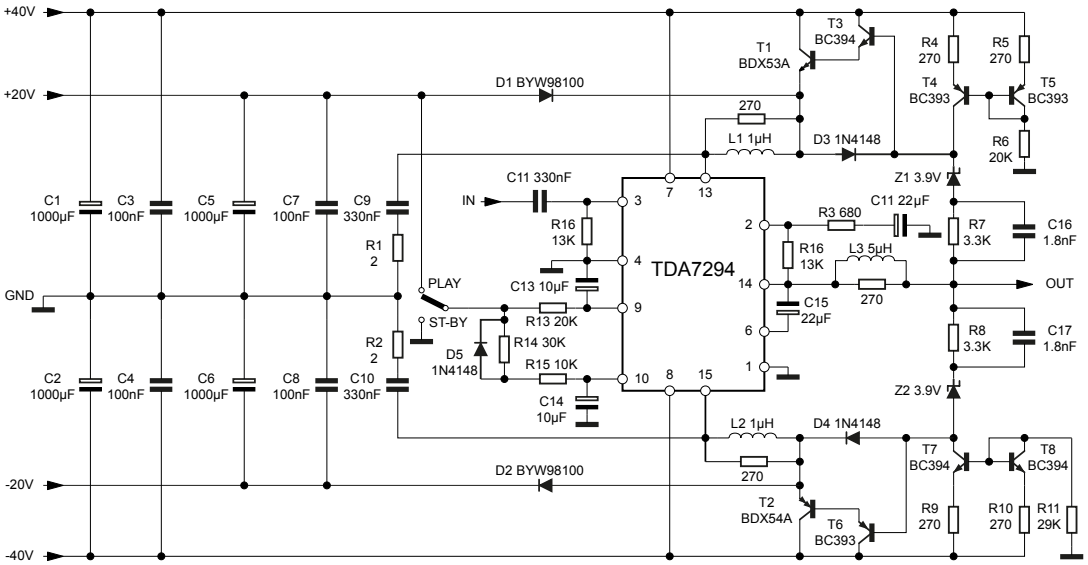
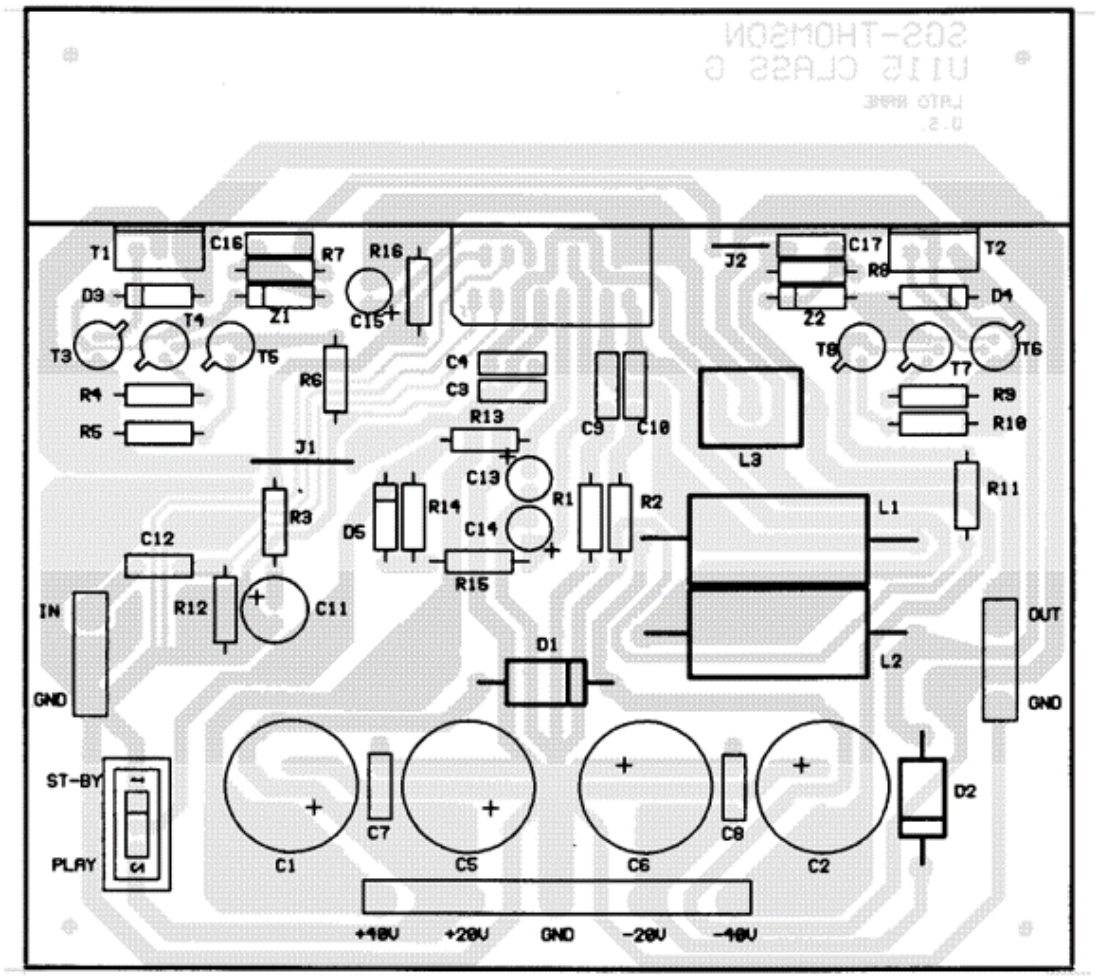


Figure 21. **P.C.B. and components layout of the circuit of figure 18 (1:1 scale)**



In Figure 23, Figure 24 the performances of the system in terms of distortion and output power at various frequencies (measured on PCB shown in Figure 21) are displayed.

The output power that the TDA7294 in highefficiency application is able to supply at Vs = + 40 V / + 20 V / - 20 V / - 40 V; f = 1 kHz is:

- Pout = 150 W @ T.H.D. = 10 % with Rl = 4 Ω
- Pout = 120 W @ T.H.D. = 1 % with Rl = 4 Ω
- Pout = 100 W @ T.H.D. = 10 % with Rl = 8 Ω
- Pout = 80 W @ T.H.D. = 10 % with Rl = 8 Ω

Results from efficiency measurements (4 and 8 Ω loads, Vs = ± 40 V) are shown by figures Figure 25 and Figure 26. We have 3 curves: total power dissipation, power dissipation of the TDA7294 and power dissipation of the darlingtons.

By considering again a maximum average output power (music signal) of 20 W, in case of the high efficiency application, the thermal resistance value needed from the heatsink is 2.2 °C / W (Vs = ± 40 V and Rl = 4 Ω).

All components (TDA7294 and power transistors T1 and T2) can be placed on a 1.5 °C / W heatsink, with the power darlingtons electrically insulated from the heatsink.

Since the total power dissipation is less than that of a usual class AB amplifier, additional cost savings can be obtained while optimizing the power supply, even with a high headroom.

Figure 22. Power dissipation vs. output power (Rl = 4 Ω)

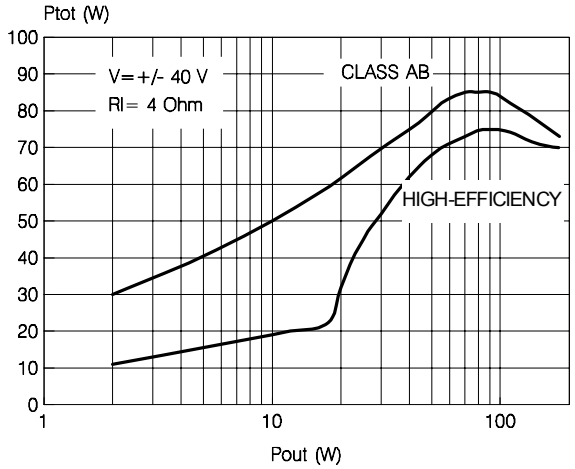


Figure 23. Distortion vs. output power (Rl = 4 Ω)

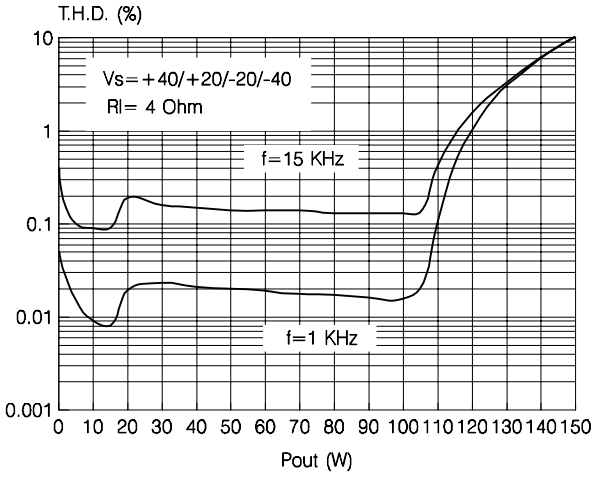


Figure 24. Distortion vs. output power (Rl = 8 Ω)

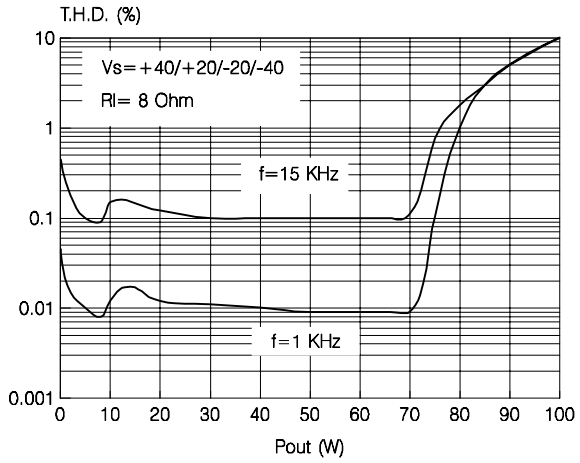


Figure 25. Power dissipation vs. output power (Rl = 4 Ω)

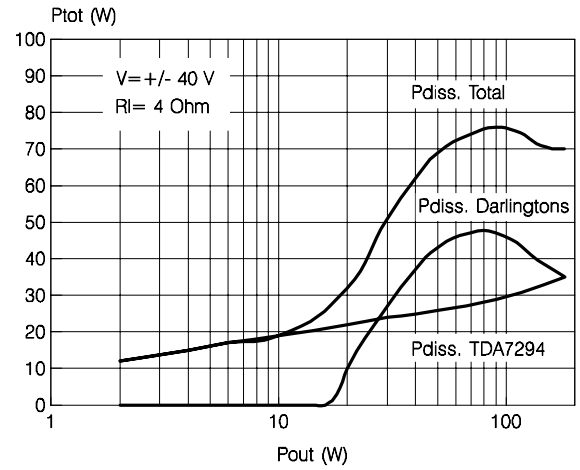
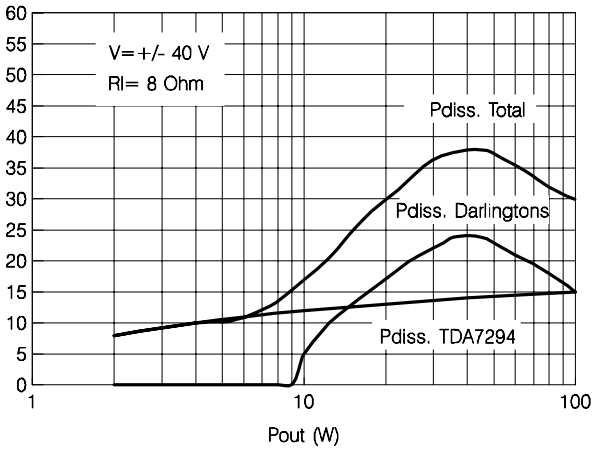


Figure 26. **Power dissipation vs. output power (Rl = 8 Ω)**



11 Bridge application

Another application suggestion is the BRIDGE configuration, where two TDA7294 are used, as shown by the schematic diagram of Figure 27.

In this application, the value of the load must not be lower than 8 Ω for dissipation and current capability reasons.

A suitable field of application includes HI-FI/TV subwoofers realizations.

The main advantages offered by this solution are:

- High power performances with limited supply voltage level.
- Considerably high output power even with high load values (i.e. 16 Ω).

The characteristics shown by Figure 29 and Figure 30, measured with loads respectively 8 Ω and 16 Ω.

With Rl = 8 Ω, Vs = ± 25 V the maximum output power obtainable is 150 W, while with Rl = 16 Ω, Vs = ± 35 V the maximum Pout is 170 W.

Figure 27. Bridge application circuit

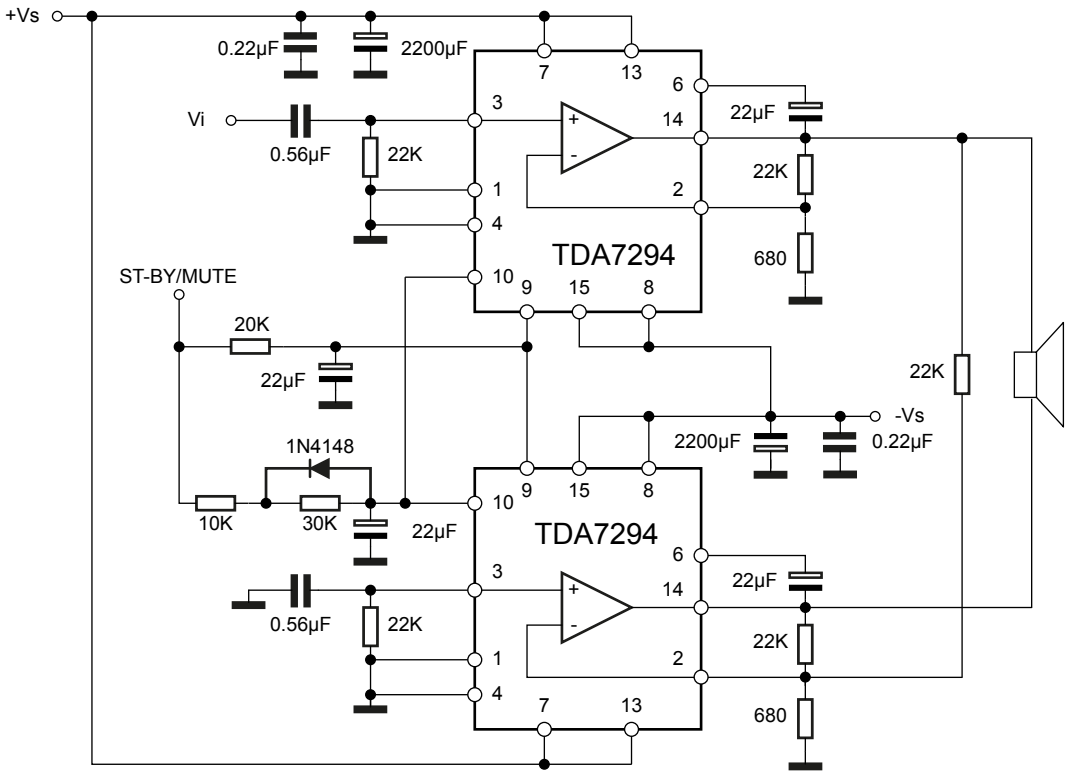


Figure 28. **Frequency response of the bridge application**

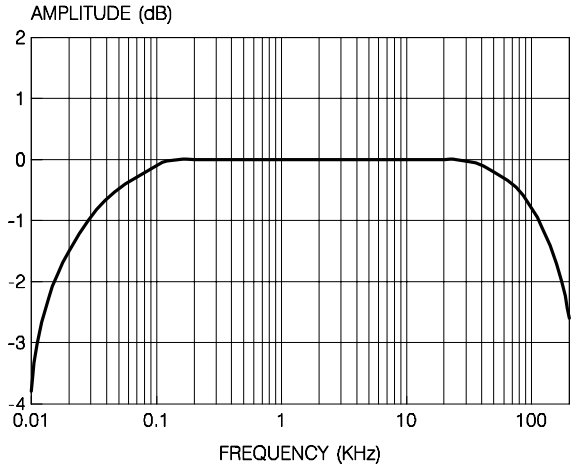


Figure 29. **Distortion vs. output power (Rl = 8 Ω)**

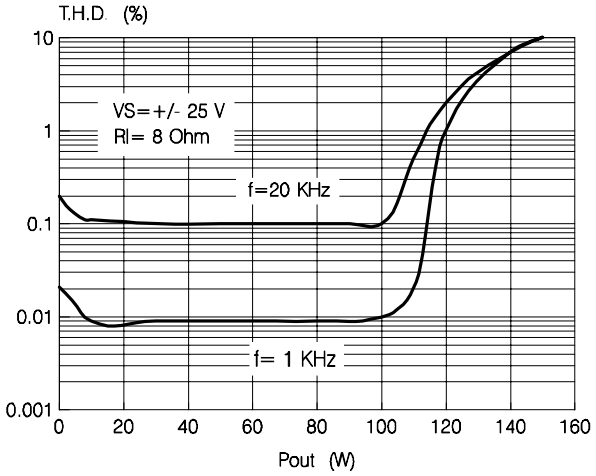
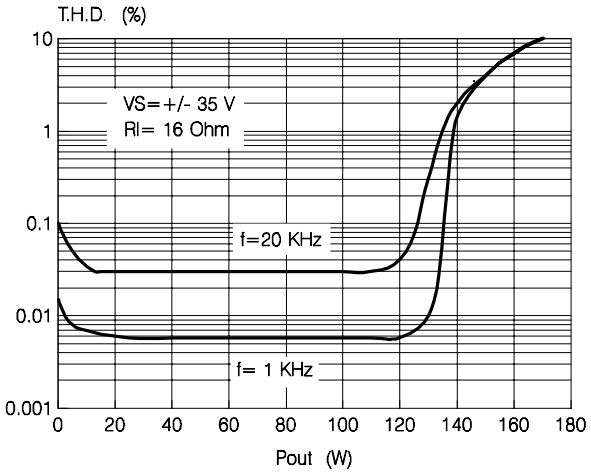


Figure 30. **Distortion vs. output power (Rl = 16 Ω)**



12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

12.1 Multiwatt15 V package information

Figure 31. **Multiwatt15 V package outline**

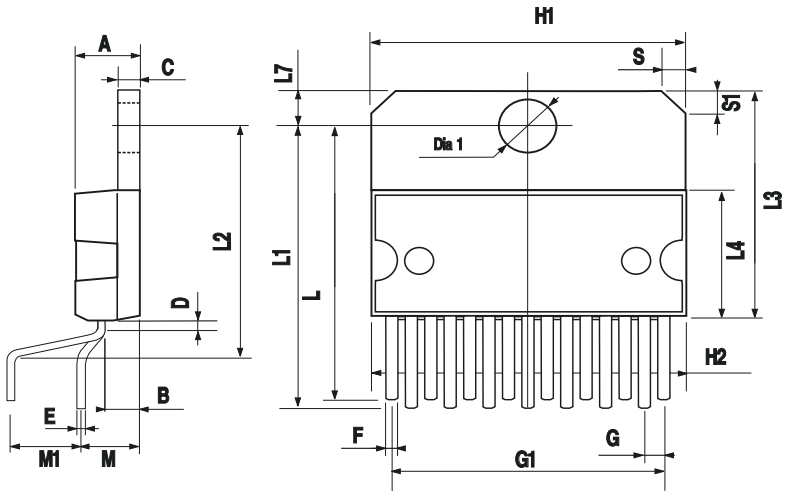


Table 4. **Multiwatt15 V mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			5
B			2.65
C			1.6
D		1	
E	0.49		0.55
F	0.66		0.75
G	1.02	1.27	1.52
G1	17.53	17.78	18.03
H1	19.6		
H2			20.2
L	21.9	22.2	22.5
L1	21.7	22.1	22.5
L2	17.65		18.1
L3	17.25	17.5	17.75
L4	10.3	10.7	10.9
L7	2.65		2.9
M	4.25	4.55	4.85
M1	4.63	5.08	5.53
S	1.9		2.6
S1	1.9		2.6
Diam. 1	3.65		3.85

12.2 Multiwatt15 H package information

Figure 32. **Multiwatt15 H package outline**

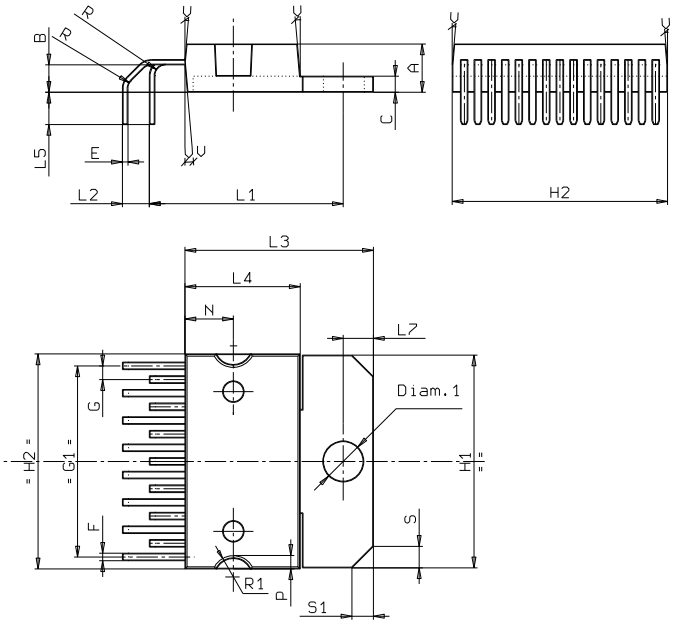


Table 5. **Multiwatt15 H mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			5.00
B			2.65
C			1.60
E	0.49		0.55
F	0.66		0.75
G	1.02	1.27	1.52
G1	17.53	17.78	18.03
H1	19.60		20.20
H2	19.60		20.20
L1	17.80	18.0	18.20
L2	2.30	2.50	2.80
L3	17.25	17.50	17.75
L4	10.3	10.70	10.90
L5	2.70	3.00	3.30
L7	2.65		2.90
R		1.50	
S	1.90		2.60
S1	1.90		2.60
Diam. 1	3.65		3.85

Revision history

Table 6. **Document revision history**

Date	Version	Changes
Apr-2003	7	First issue in EDOCS DMS.
31-Jul-2020	8	Updated Section 12.2 Multiwatt15 H package information.

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