The P1011 and P1020 processors have an advanced set of features for ease of use. The 256 KB L2 cache offers incremental configuration to partition the cache between the two cores or to configure it as SRAM or stashing memory. The integrated security engine supports the cryptographic algorithms commonly used in IPsec, SSL, 3GPP and other networking and wireless security protocols. The memory controller offers future-proofing against memory technology migration with support for both DDR2 and DDR3. It also supports error correction codes, a baseline requirement for any high-reliability system.

The P1011 and P1020 processors integrate a rich set of interfaces, including a 4-lane multiprotocol SerDes, Gigabit Ethernet, PCI Express® and USB. The three 10/100/1000 Ethernet ports support advanced packet parsing, flow control and quality of service features, as well as IEEE® 1588 time-stamping—all ideal for managing the datapath traffic between the LAN and WAN interface. A TDM interface can support voice for legacy phone applications. Four SerDes lanes can be portioned across two PCI Express ports and two SGMII ports. The PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support. USB or SD/MMC interfaces can be used to support local storage. A second USB interface is also available to support USB attached printers or as a console port. Multiple memory connection ports are available, including the 16-bit local bus, two USB 2.0 controllers, eSDHC and SPI.

Target Applications

The P1011 and P1020 processors serve in a wide variety of applications. The devices are well suited for various combinations of data plane and control plane workloads in networking and telecom applications. With an available junction temperature range of –40 ºC to +125 ºC, the devices can be used in power-sensitive defense and industrial applications, and outdoor environments less protected from the environment. The devices' primary target applications are networking and telecom linecards.

A multiservice router or business gateway requires a combination of high performance and a rich set of peripherals to support the datapath throughputs and required system functionality. The P1011 and P1020 devices offer a scalable platform to develop a range of products that can support the same feature set. Integrated 10/100/1000 Ethernet controllers with classification and QoS capabilities are ideal for managing the datapath traffic between the LAN and WAN interface. PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support, TDM for legacy phone interfaces to support voice and the USB or SD/MMC interfaces can be used to support local storage. The second USB interface is also available to support USB-attached printers or as a console port. And the integrated security engine can provide encrypted secure communications for remote users with VPN support.

Technical Specifications

- Dual (P1020) or single (P1011) high-performance Power Architecture e500 cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 533–800 MHz core clock frequency
- 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- Three 10/100/1000 Mb/s enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE 1588 support
  - Lossless flow control
  - RGMII, SGMII
- High-speed interfaces (not all available simultaneously)
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Two PCI Express controllers
  - Two SGMII interfaces
- Two High-Speed USB controllers (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Enhanced secure digital host controller (eSDHC)
- Serial peripheral interface
- Integrated security engine (SEC 3.3)
  - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Snow 3G and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (e.g., IPsec, SSL, SRTP, WiMAX)
  - XOR acceleration
- 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals
- Package: 689-pin wirebond power-BGA (TEPBGA2)

QorIQ P1020 and P1011 Features

QorIQ Platform	Device	Cores	Top Core Frequency	L2 Size	DDR 2/3 Support	GE Ports	QUICC Engine	SerDes	PCI Express	Serial RapidIO	TDM
P1	P1011	1	800 MHz	256 KB	32-bit with ECC	3	4	2	N/A	Yes	Yes
P1	P1020	2	800 MHz	256 KB	32-bit with ECC	3	4	2	N/A	Yes	Yes
P2	P2010	1	1200 MHz	512 KB	64-bit with ECC	3	4	3	2	N/A	In QUICC Engine
P2	P2020	2	1200 MHz	512 KB	64-bit with ECC	3	4	3	2	N/A	In QUICC Engine

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