Absolute Maximum Ratings

IO Voltage Range to GND.....-0.5V to +6.0V
IO Sink Current DS1990A.....20mA
IO Sink Current DS1990AA.....±10mA
Junction Temperature.....+125°C
Storage Temperature Range..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values at +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	DS1990A (Note 1)	2.8		6.0	V
		DS1990AA (Note 1)	3.0		5.25	V
1-Wire Pullup Resistance	R_{PUP}	DS1990A (Notes 1 and 2)	0.6		5	kΩ
		DS1990AA (Notes 1 and 2)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	DS1990A (Notes 3, 4, and 5)		100	800	pF
		DS1990AA (Notes 4 and 5)		1000		pF
Input Load Current	I_L	DS1990A (Note 6)		0.25		µA
		DS1990AA IO pin at V_{PUP} (Note 6)	0.05	1.75	6.7	µA
Input Low Voltage	V_{IL}	(Notes 1 and 7)			0.3	V
Input High Voltage	V_{IH}	DS1990A (Notes 4 and 8)	2.2			V
		DS1990AA (Notes 4 and 8)		0.75 x V_{PUP}		
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Recovery Time	t_{REC}	DS1990A (Note 1)	1			µs
		DS1990AA (Note 1)	5			µs
Time Slot Duration	t_{SLOT}	DS1990A (Note 1)	61			µs
		DS1990AA (Note 1)	65			µs
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time	t_{RSTL}	DS1990A (Notes 1 and 9)	480			µs
		DS1990AA (Note 1)	480		640	µs
Reset High Time	t_{RSTH}	(Notes 1 and 10)	480			µs
Presence-Detect High Time	t_{PDH}		15		60	µs
Presence-Detect Low Time	t_{PDL}	(Note 11)	60		240	µs
Presence-Detect Sample Time	t_{MSP}	(Note 1)	60		75	µs
IO PIN: 1-Wire WRITE						
Write-Zero Low Time	t_{W0L}	(Notes 1 and 12)	60		120	µs
Write-One Low Time	t_{W1L}	(Notes 1 and 12)	1		15	µs
IO PIN: 1-Wire READ						
Read Low Time	t_{RL}	(Notes 1 and 13)	1		15 - d	µs
Read Sample Time	t_{MSR}	(Notes 1 and 13)	t_{RL} + d		15	µs

Note 1: System requirement.
Note 2: Full R_{PUP} range is guaranteed by design and simulation and not production tested. Production testing performed at a fixed R_{PUP} value. Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.

Electrical Characteristics (continued)

(Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values at +25°C.)

Note 3: Capacitance on the IO pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull up the IO line to V_{PUP} 5µs after power has been applied, the parasite capacitance will not affect normal communications.
Note 4: Guaranteed by design, simulation only. Not production tested.
Note 5: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication.
Note 6: Input load is to ground.
Note 7: The voltage on IO must be less than or equal to V_{ILMAX} whenever the master drives the line low.
Note 8: V_{IH} is a function of the internal supply voltage.
Note 9: The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs to allow interrupt signaling. A longer duration could mask or conceal interrupt pulses if this device is used in parallel with a DS1994.
Note 10: An additional reset or communication sequence cannot begin until the reset high time has expired.
Note 11: Presence pulse is guaranteed only after a preceding reset pulse (t_{RSTL}).
Note 12: ε in Figure 7 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{IH}. The actual maximum duration for the master to pull the line low is $t_{W1LMAX} + t_F - \varepsilon$ and $t_{W0LMAX} + t_F - \varepsilon$, respectively.
Note 13: δ in Figure 7 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is $t_{RLMAX} + t_F$.

iButton CAN PHYSICAL SPECIFICATION

SIZE	See the *Package Information* section.
WEIGHT (DS1990A)	Ca. 2.5 grams

Detailed Description

The block diagram in Figure 1 shows the major function blocks of the device. The DS1990A takes the energy it needs to operate from the IO line, as indicated by the parasite power block. The ROM function control unit includes the 1-Wire interface and the logic to implement the ROM function commands, which access 64 bits of unique ROM.

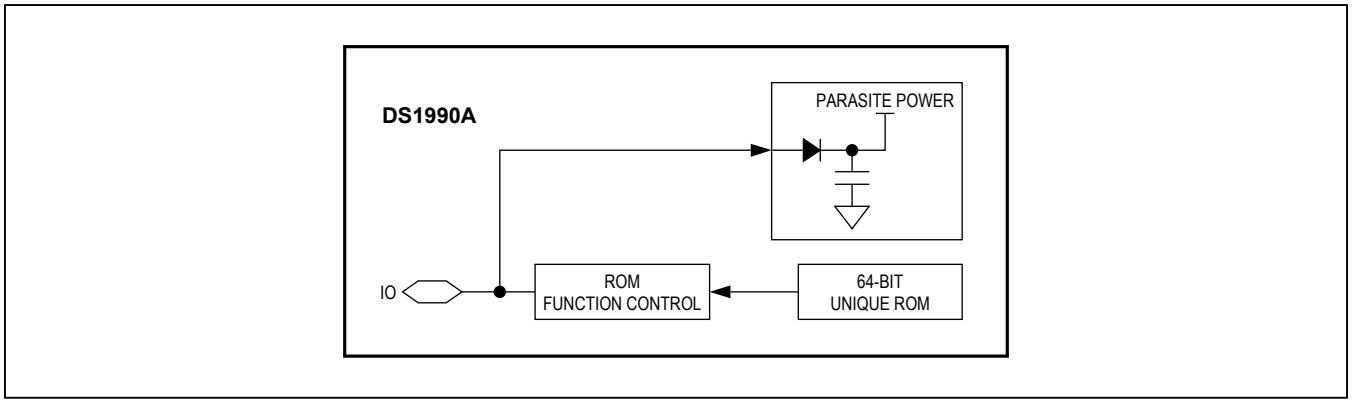

Figure 1. Block Diagram

64-Bit Unique ROM

Each DS1990A contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. See Figure 2 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 3. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the 1-Wire Cyclic Redundancy Check (CRC) is available in **Application Note 27: *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products***.

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8th bit of the family code has been entered, the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC returns the shift register to all 0s.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus master and one or more slaves. In all instances, the DS1990A is a slave device. The bus master is typically a microcontroller or PC. For small configurations, the 1-Wire communication signals can be generated under software control using a single port pin. Alternatively, the DS2480B 1-Wire line driver chip or serial-port adapters based on this chip (DS9097U series) can be used. This simplifies the hardware design and frees the microprocessor from responding in real time. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the **Book of iButton Standards**.

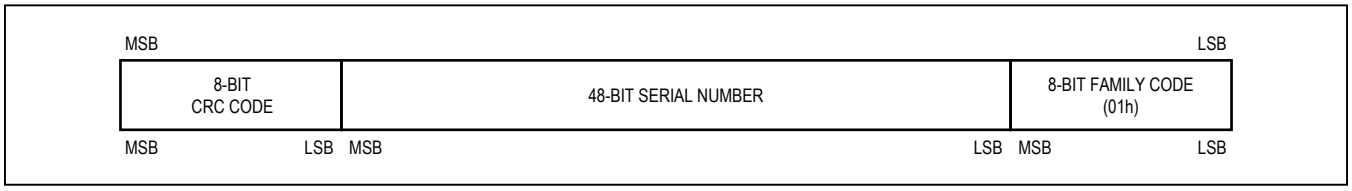

Figure 2. 64-Bit Unique ROM

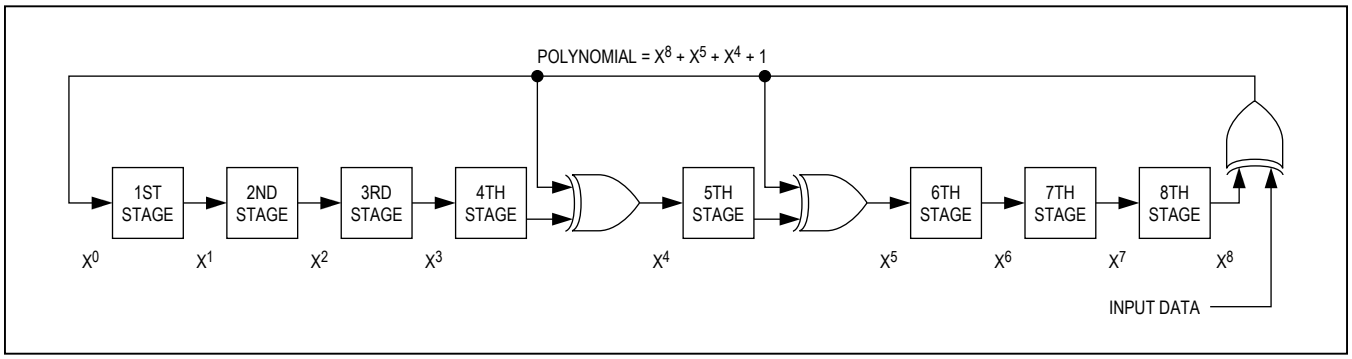

Figure 3. 1-Wire CRC Generator

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS1990A is open drain with an internal circuit equivalent to that shown in Figure 4. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed, the 1-Wire bus has a maximum data rate of 16.3kbps. The value of the pullup resistor primarily depends on the network size and load conditions. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus **must** be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120µs, one or more devices on the bus may be reset.

Transaction Sequence

The protocol for accessing the DS1990A through the 1-Wire port is as follows:

- Initialization
- ROM Function Command

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1990A is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

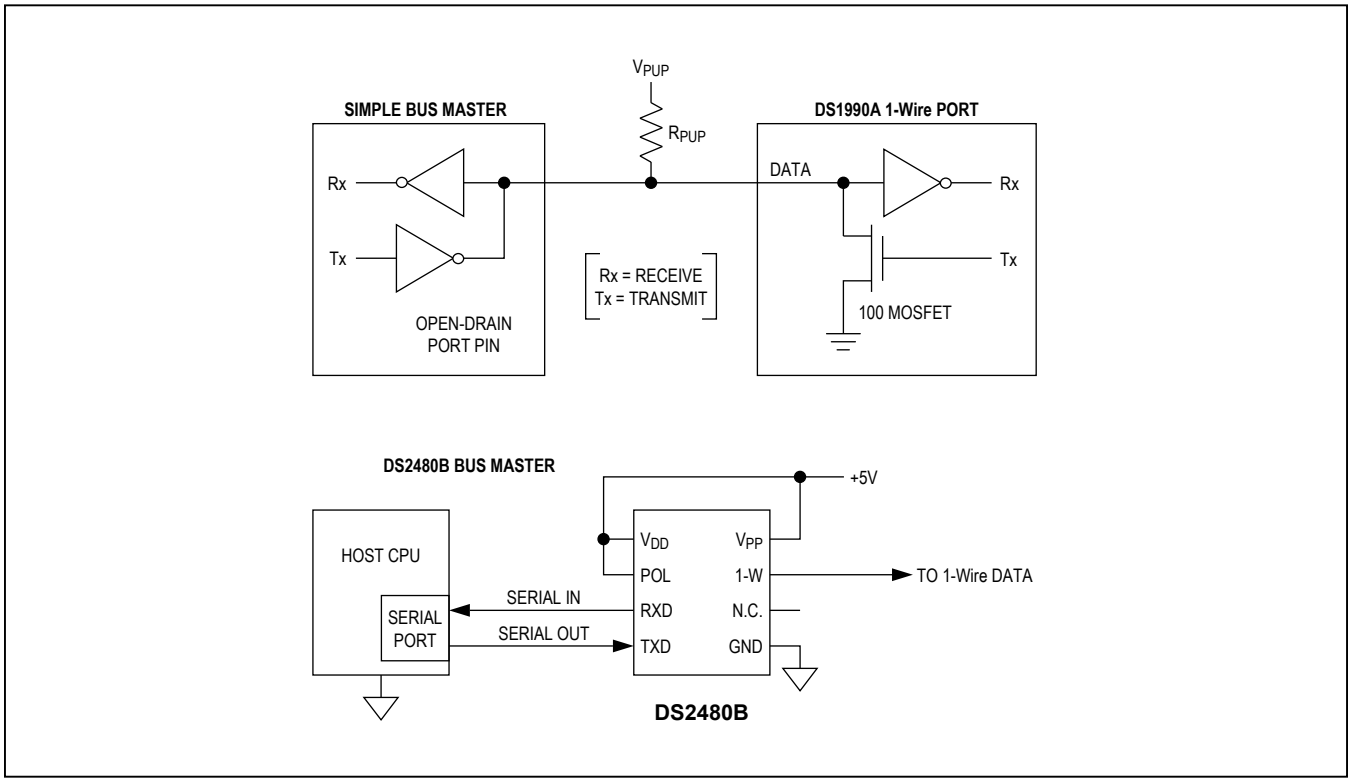

Figure 4. Hardware Configuration

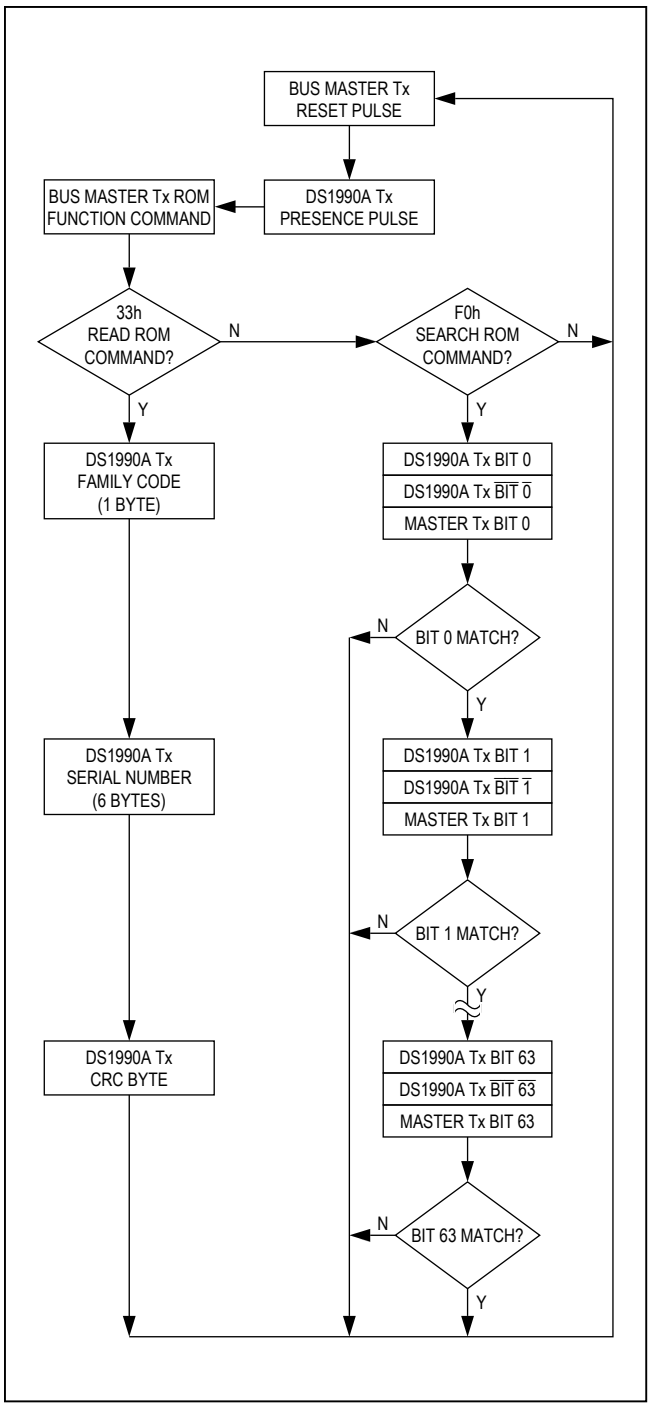

Figure 5. ROM Functions Flowchart

1-Wire ROM Function Commands

Once the bus master has detected a presence, it can issue one of the ROM function commands the DS1990A supports. All ROM function commands are 8 bits long. A list of these commands follows. (See Figure 5 for a flowchart.)

Read ROM [33h]

This command allows the bus master to read the DS1990A's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave device on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number results in a mismatch of the CRC.

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the ROM code tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to **Application Note 187: *1-Wire Search Algorithm*** for a detailed discussion, including an example.

Match ROM [55h]/Skip ROM [CCh]

The minimum set of 1-Wire ROM function commands includes a Match ROM and a Skip ROM command. Because the DS1990A contains only the 64-bit ROM without any additional data fields, Match ROM and Skip ROM are not applicable. The DS1990A remains silent (inactive) upon receiving a ROM function command that it does not support. This allows the DS1990A to coexist on a multidrop bus with other 1-Wire devices that do respond to Match ROM or Skip ROM. DS1990AA will return a response after MatchROM/Skip ROM. If a multidrop configuration exists in the application, this should be taken into account.

1-Wire Signaling

The DS1990A requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all these signals.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} to below V_{ILMAX}. To get from active to idle, the voltage needs to rise from V_{ILMAX} to above V_{IHMIN}. The time it takes for the voltage to make this rise, referenced as ε in Figure 6, depends on the value of the pullup resistor (R_{PUP}) and capacitance of the 1-Wire network attached.

The initialization sequence required to begin any communication with the DS1990A is shown in Figure 6. A reset pulse followed by a presence pulse indicates that the DS1990A is ready to receive a ROM function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge.

After the bus master has released the line, it goes into receive mode (Rx). Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a DS2480B driver, by active circuitry. When the V_{IHMIN} is crossed, the DS1990A waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

Read/Write Time Slots

Data communication with the DS1990A takes place in time slots that carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. The definitions of the write and read time slots are illustrated in Figure 7.

All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below V_{ILMAX}, the DS1990A starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Master-to-Slave

For a **write-one** time slot, the voltage on the data line must have risen above V_{IHMIN} after the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below V_{ILMAX} until the **write-zero** low time t_{W0LMIN} is expired. For most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} window. After the voltage has risen above V_{IHMIN}, the DS1990A needs a recovery time t_{REC} before it is ready for the next time slot.

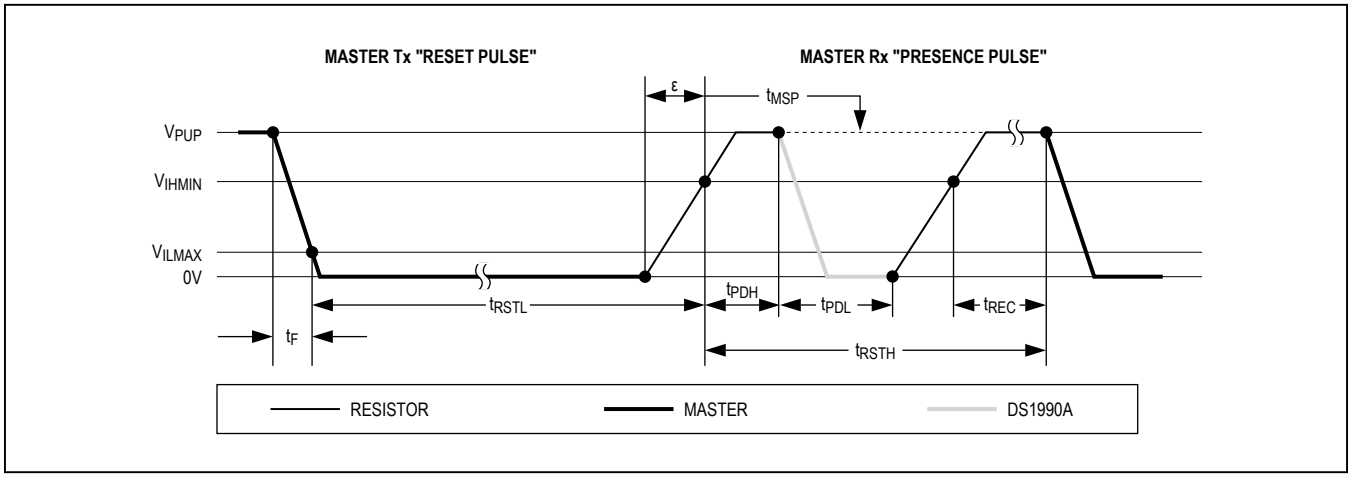

Figure 6. Initialization Procedure: Reset and Presence Pulses

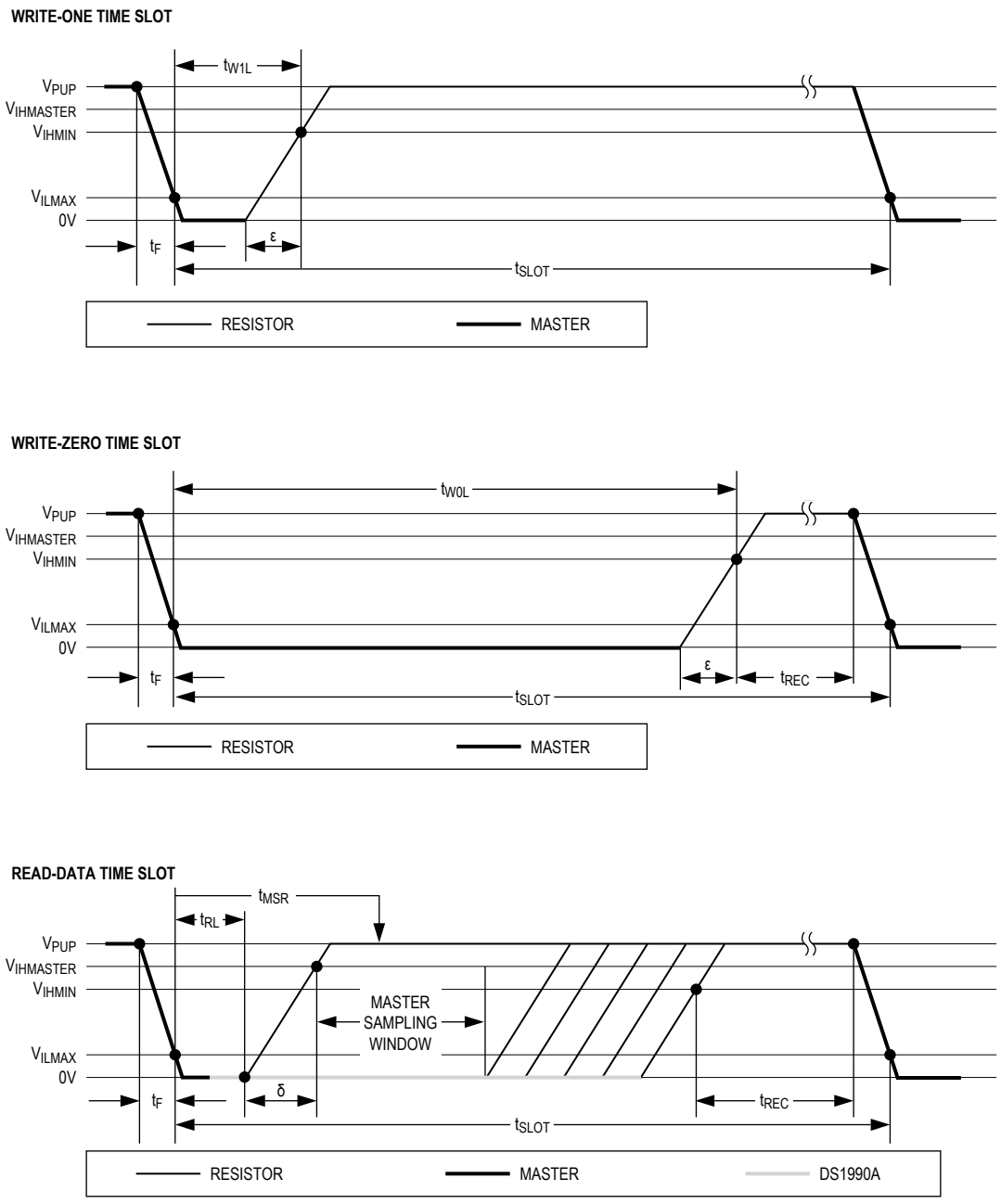

Figure 7. Read/Write Timing Diagram

Slave-to-Master

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{ILMAX} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS1990A starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS1990A does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS1990A on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For most reliable communication, t_{RL} should be as short as permissible and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS1990A to get ready for the next time slot.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.
F3 iButton	IB#3NB	21-0252
F5 iButton	IB#5NB	21-0266

Revision History

REVISION DATE	DESCRIPTION	PAGES CHANGED
033005	Redid the formatting based on newer template style. Also deleted the 0F Read ROM command and added a note about presence pulse criteria.	1–8
10/08	Created newer template-style data sheet.	All
	Updated *Ordering Information* with lead-free part numbers.	1
	Deleted *Meets UL 913 (4th Edit)*; *Intrinsically Safe Apparatus*: *Approved Under Entity Concept for Use in Class I*, *Division I*, *Group A*, *B*, *C*, and *D* from the *Common iButton Features and iButton Can Physical Specification* sections.	1, 3
	Updated *Electrical Characteristics* table: Deleted *Output High Voltage* parameter. Moved *1-Wire Pullup* voltage parameter from table header to table body. Changed V_{ILMAX} from 0.8V to 0.3V. Added Note 14 to the t_{W0L} specification. Changed t_{W1LMAX} from 15µs – ε to 15µs.	2
	Added the epsilon timing to the *Write-Zero Time Slot* in Figure 7.	8
11/21	Added the DS1990AA part number and related changes	1–6

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Maxim Integrated:

DS1990A-F3+ DS1990A-F5+ DS1990A-F3 DS1990A-F5 DS1990A-F3# DS1990A-F5# DS1990A-F3/C00+ DS1990A-F3+C0B DS1990A-F3+C80 DS1990A-F3+C8F DS1990A-F3-W DS1990A-F5+E00 DS1990A-F5-W DS1990A-F5/E4F