Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
PG_, $\overline{RESET}$, $\overline{WDO}$ .....-0.3V to +14V
IN1–IN8, TH0–TH4, $\overline{ENABLE}$, WDI, $\overline{MR}$, $\overline{MARGIN}$, SRT, SWT, V_{CC} .....-0.3V to +6V
DBP .....-0.3V to +3V
Input/Output Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derate 21.3mW/°C above +70°C).....1702mW
32-Pin Thin QFN (derate 21.3mW/°C above +70°C).....1702mW
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-Free.....+260°C
Containing Lead (Pb).....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = V_{IN6}–V_{IN8} = V_{GND}, V_{IN2}–V_{IN5} = 2.7V to 5.5V, WDI = $\overline{ENABLE}$ = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)		Voltage on either one of IN2–IN5 or V_{CC} that guarantees the part is fully operational		2.7		5.5	V
Undervoltage Lockout	V_{UVLO}	For 1V < (V_{IN2}–V_{IN5} or V_{CC}) < V_{UVLO}, PG_ are pulled down to GND with a 10µA current				2.5	V
Digital Bypass Voltage	V_{DBP}	No load		2.48	2.55	2.67	V
Supply Current	I_{CC}	V_{IN2} = 5.5V, V_{IN1}, V_{IN3}–V_{IN8} = V_{GND}, no load			0.9	1.1	mA
Threshold Accuracy (Table 2)	V_{TH}	IN1–IN8, IN_ falling	T_A = +25°C to +85°C	-1		+1	% V_{TH}
			T_A = -40°C to +85°C	-2		+2	
Threshold Hysteresis	V_{TH-HYS}				0.3		% V_{TH}
Threshold Tempco	ΔV_{TH}/°C				10		ppm/°C
Input Leakage Current	I_{IN}	IN1, IN6–IN8		-50		+50	nA
		IN2–IN5 set as adjustable thresholds					
IN2–IN5 Input Impedance	$R_{IN2–IN5}$	For IN_ voltages < the highest IN_ supply or < V_{CC} and thresholds are not set as adjustable		290	400	555	kΩ
Power-Up Delay	t_{D-PO}	V_{CC} ≥ V_{UVLO}				3	ms
IN_ to PG_ Delay	t_{D-R}	IN_ falling/rising, 100mV overdrive			25		µs
PG_ Timeout Period	t_{PG}			5.625	6.25	6.875	ms
$\overline{RESET}$ Default Timeout Period	t_{RP}	V_{SRT} = V_{CC}		180	200	220	ms
$\overline{RESET}$ Adjustable Timeout Period	t_{RP-ADJ}	C_{SRT} = 47nF		135	207	280	ms
SRT Adjustable Timeout Current	I_{SRT}	V_{SRT} = V_{GND}		180	230	280	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN6}–V_{IN8} = V_{GND}, V_{IN2}–V_{IN5} = 2.7V to 5.5V, WDI = $\overline{ENABLE}$ = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SRT Default Timeout Threshold	$V_{SRT-DEF}$	$V_{SRT} \geq V_{SRT-DEF}$, selects reset default timeout	1.1	1.25	1.5	V
SRT Adjustable Timeout Threshold	$V_{SRT-ADJ}$	(Note 4)	0.95	1.0	1.05	V
SRT Adjustable Timeout Discharge Threshold	$V_{SRT-DIS}$	(Note 5)		100		mV
SRT Adjustable Timeout Output Low Discharge Current	$I_{SRT-DIS}$	V_{SRT} = 0.3V	0.7			mA
PG_, $\overline{RESET}$, $\overline{WDO}$ Output Low	V_{OL}	I_{SINK} = 4mA, output asserted			0.4	V
PG_, $\overline{RESET}$, $\overline{WDO}$ Output Initial Pulldown Current	I_{UV}	$V_{CC} \leq V_{UVLO}$, $V_{PG\_}$, $V_{\overline{RESET}}$, $V_{\overline{WDO}}$ = 0.8V		10	40	µA
PG_, $\overline{RESET}$, $\overline{WDO}$ Output Open-Drain Leakage Current	I_{LKG}	Output high impedance	-1		+1	µA
$\overline{MR}$, $\overline{MARGIN}$, $\overline{ENABLE}$, TH0–TH4, WDI Input Voltage	V_{IL}				0.6	V
	V_{IH}		1.4			
$\overline{MR}$ Input Pulse Width	$T_{\overline{MR}}$		1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to $\overline{RESET}$ Delay	$t_{D-\overline{MR}}$			2		µs
$\overline{MR}$ to DBP Pullup Current	$I_{\overline{MR}}$	$V_{\overline{MR}}$ = 1.4V	5	10	15	µA
$\overline{MARGIN}$ to DBP Pullup Current	$I_{\overline{MARGIN}}$	$V_{\overline{MARGIN}}$ = 1.4V	5	10	15	µA
$\overline{ENABLE}$ to PG_ Delay	t_{D-ENPG}			200		ns
$\overline{ENABLE}$ Pulldown Current		$V_{\overline{ENABLE}}$ = 0.6V	5	10	15	µA

Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN6}–V_{IN8} = V_{GND}, V_{IN2}–V_{IN5} = 2.7V to 5.5V, WDI = $\overline{ENABLE}$ = GND, TH0–TH4 = $\overline{MARGIN}$ = $\overline{MR}$ = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

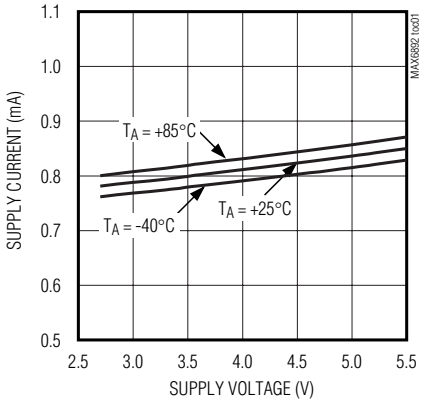
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TH0–TH4 Input Current				-1		+1	µA
WDI Pulldown Current	I_{WDI}	V_{WDI} = 0.6V		5	10	15	µA
WDI Input Pulse Width				50			ns
Watchdog Default Timeout Period	t_{WD}	V_{SWT} = V_{CC}	Initial mode	92.16	102.4	112.64	s
			Normal mode	1.44	1.6	1.76	
Watchdog Adjustable Timeout Period	t_{WD-ADJ}	C_{SWT} = 0.33µF	Initial mode	53.7	82.5	111.9	s
			Normal mode	0.93	1.43	1.94	
SWT Adjustable Timeout Current	I_{SWT}	V_{SWT} = V_{GND}		180	230	280	nA
SWT Default Timeout Threshold	$V_{SWT-DEF}$	V_{SWT} ≥ $V_{SWT-DEF}$, selects watchdog default timeout period		1.1	1.25	1.5	V
SWT Adjustable Timeout Threshold	$V_{SWT-ADJ}$	(Note 4)		0.95	1.0	1.05	V
SWT Adjustable Timeout Discharge Threshold	$V_{SWT-DIS}$	(Note 5)			100		mV
SWT Adjustable Timeout Output Low Discharge Current	$I_{SWT-DIS}$	V_{SWT} = 0.3V		0.7			mA

Note 1: 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.
Note 2: Device may be supplied from any one of IN2–IN5, or V_{CC}.
Note 3: The internal supply voltage, measured at V_{CC}, equals the maximum of IN2–IN5.
Note 4: External capacitor is charged by I_{S_T} when V_{S_T-DIS} < V_{S_T} < V_{S_T-ADJ}.
Note 5: External capacitor is discharged by I_{S_T-DIS} down to V_{S_T-DIS} after V_{S_T} reaches V_{S_T-ADJ}.

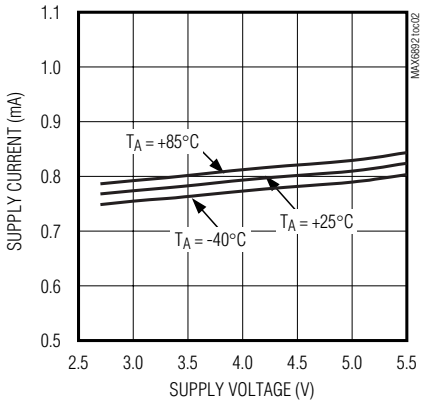
Typical Operating Characteristics

(V_{IN1} = V_{IN6}–V_{IN8} = V_{GND}, V_{IN2}–V_{IN5} = 2.7V to 5.5V, V_{WDI} = V_{GND}, V_{TH0}–V_{TH4} = $V_{\overline{MARGIN}}$ = $V_{\overline{MR}}$ = V_{DBP}. Typical values are at T_A = +25°C.)

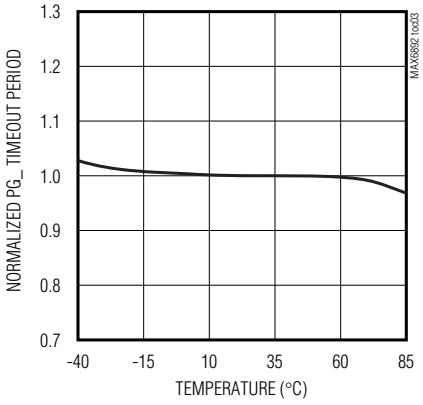
SUPPLY CURRENT vs. SUPPLY VOLTAGE (IN2–IN5)



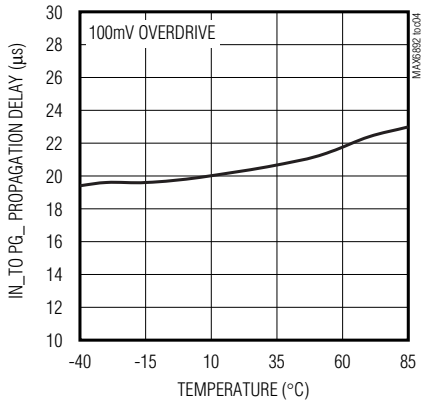
SUPPLY CURRENT vs. SUPPLY VOLTAGE (V_{CC})



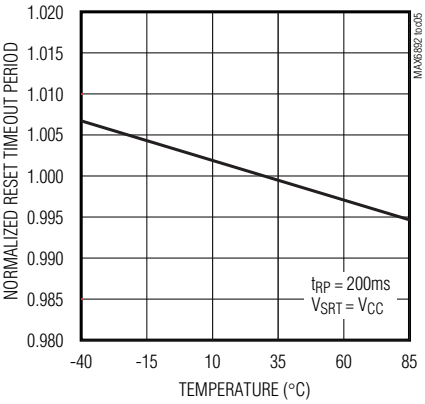
NORMALIZED PG_ TIMEOUT PERIOD vs. TEMPERATURE



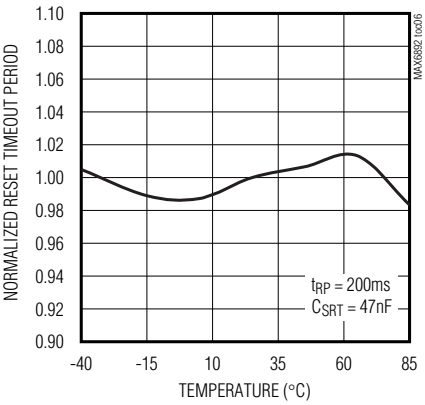
IN_ TO PG_ PROPAGATION DELAY vs. TEMPERATURE



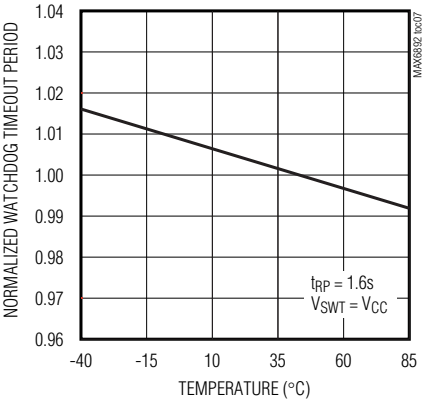
NORMALIZED DEFAULT RESET TIMEOUT PERIOD vs. TEMPERATURE



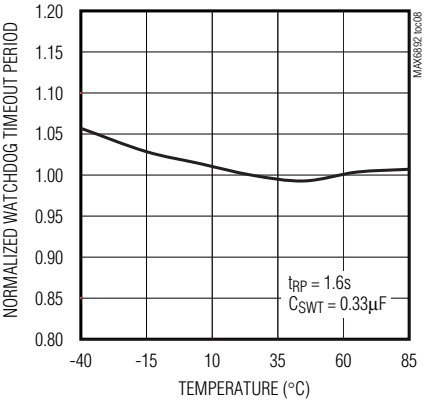
NORMALIZED ADJUSTABLE RESET TIMEOUT PERIOD vs. TEMPERATURE



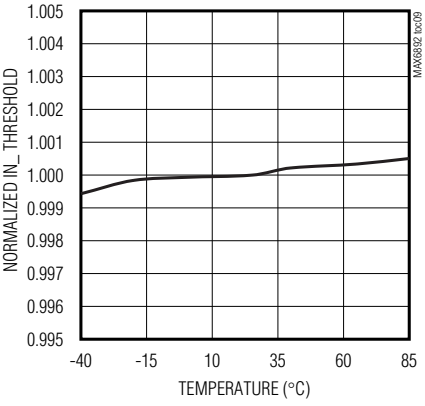
NORMALIZED DEFAULT WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



NORMALIZED ADJUSTABLE WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



NORMALIZED IN_ THRESHOLD vs. TEMPERATURE

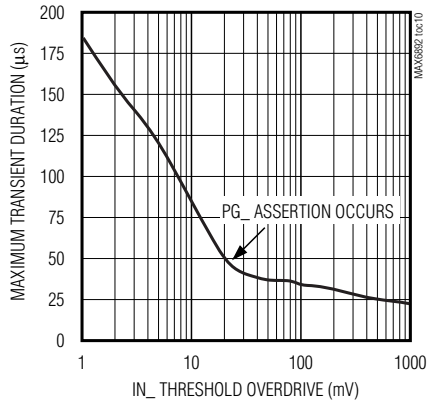


Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

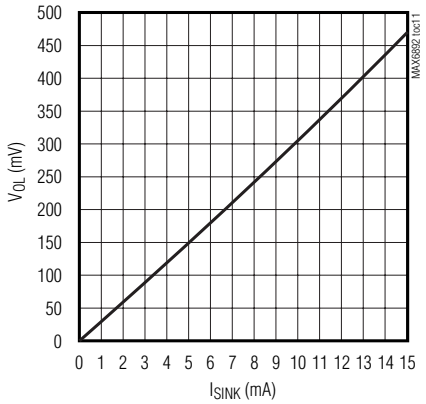
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN6}–V_{IN8} = V_{GND}, V_{IN2}–V_{IN5} = 2.7V to 5.5V, V_{WDI} = V_{GND}, V_{TH0}–V_{TH4} = $V_{\overline{MARGIN}}$ = $V_{\overline{MR}}$ = V_{DBP}. Typical values are at T_A = +25°C.)

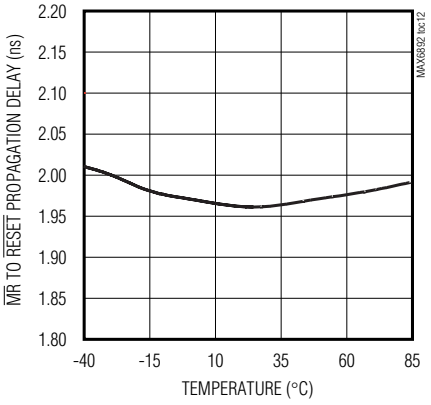
MAXIMUM IN_ TRANSIENT vs. IN_ THRESHOLD OVERDRIVE



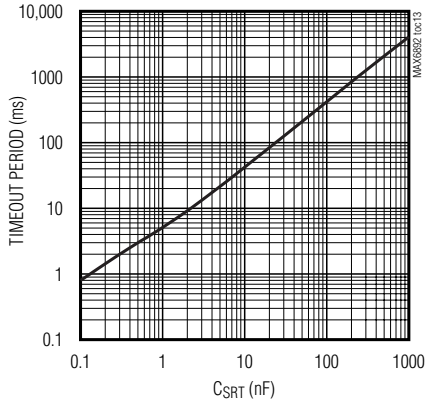
OUTPUT VOLTAGE LOW vs. SINK CURRENT



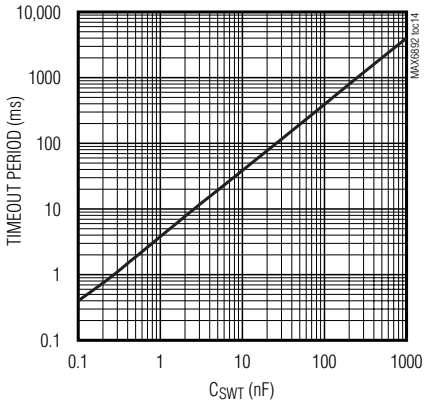
$\overline{MR}$ TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



RESET TIMEOUT PERIOD vs. C_{SRT}



WATCHDOG TIMEOUT PERIOD vs. C_{SWT}



Pin Description

PIN			NAME	FUNCTION
MAX6892	MAX6893	MAX6894		
1	1	1	PG2	Open-Drain, Power-Good Output 2. PG2 asserts low when the voltage input at IN2 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG2 deasserts with a factory preset timeout period of 6.25ms.
2	2	2	PG3	Open-Drain, Power-Good Output 3. PG3 asserts low when the voltage input at IN3 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG3 deasserts with a factory preset timeout period of 6.25ms.
3	3	3	PG4	Open-Drain, Power-Good Output 4. PG4 asserts low when the voltage input at IN4 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG4 deasserts with a factory preset timeout period of 6.25ms.
4	4	4	GND	Ground
5	5	—	PG5	Open-Drain, Power-Good Output 5. PG5 asserts low when the voltage input at IN5 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG5 deasserts with a factory preset timeout period of 6.25ms.
6	6	—	PG6	Open-Drain, Power-Good Output 6. PG6 asserts low when the voltage input at IN6 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG6 deasserts with a factory preset timeout period of 6.25ms.
7	—	—	PG7	Open-Drain, Power-Good Output 7. PG7 asserts low when the voltage input at IN7 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG7 deasserts with a factory preset timeout period of 6.25ms.
8	—	—	PG8	Open-Drain, Power-Good Output 8. PG8 asserts low when the voltage input at IN8 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG8 deasserts with a factory preset timeout period of 6.25ms.
9	7	7	$\overline{\text{RESET}}$	Open-Drain, Active-Low Reset Output Stage. $\overline{\text{RESET}}$ asserts low when any monitored input (IN_) is below the selected threshold or manual reset ($\overline{\text{MR}}$) is pulled low. $\overline{\text{RESET}}$ remains low for the reset timeout period after all reset-causing conditions are cleared, and then deasserts.
10	8	8	$\overline{\text{WDO}}$	Open-Drain, Active-Low Watchdog Output Stage. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and the $\overline{\text{WDO}}$ output asserts low. The internal watchdog timer clears whenever $\overline{\text{RESET}}$ is asserted or WDI sees a rising or falling edge. Connect $\overline{\text{WDO}}$ to $\overline{\text{MR}}$ to automatically assert the $\overline{\text{RESET}}$ output after each watchdog timeout fault.
11	9	9	$\overline{\text{MARGIN}}$	Margin Input. $\overline{\text{MARGIN}}$ holds PG_, $\overline{\text{RESET}}$, and $\overline{\text{WDO}}$ in their existing states when driven low. Leave $\overline{\text{MARGIN}}$ unconnected or connect to DBP if unused. $\overline{\text{MARGIN}}$ overrides $\overline{\text{MR}}$ if both assert at the same time. $\overline{\text{MARGIN}}$ is internally pulled up to DBP through a 10µA current source.
12	10	10	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Pull $\overline{\text{MR}}$ low to assert $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ remains asserted for its preset/adjustable reset timeout period when $\overline{\text{MR}}$ is driven/pulled high. $\overline{\text{MR}}$ is internally pulled up to DBP through a 10µA current source.
13	11	11	TH0	Threshold Selection Input 0. Logic input to select desired thresholds. Connect TH0 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.

Pin Description (continued)

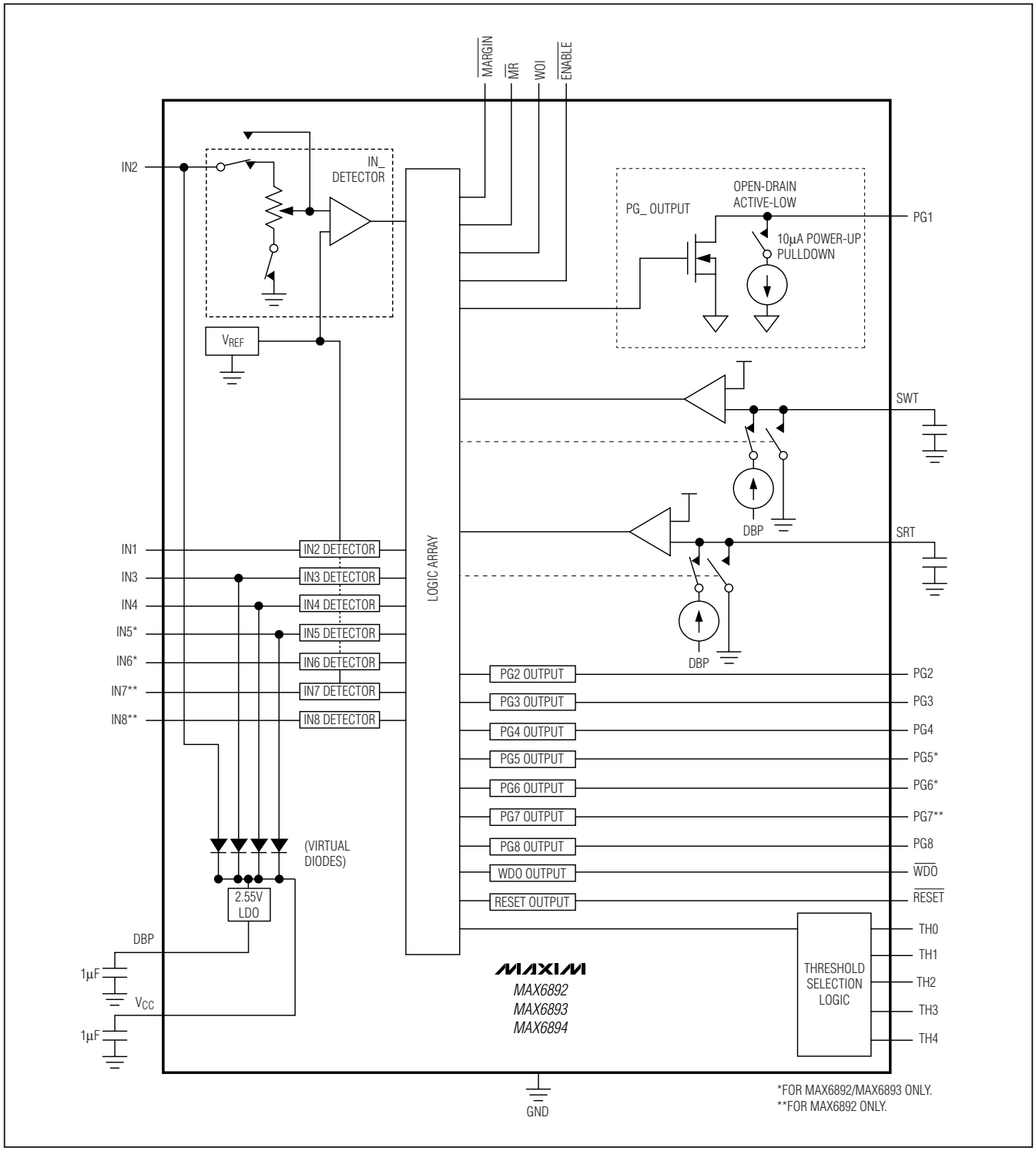
PIN			NAME	FUNCTION
MAX6892	MAX6893	MAX6894		
14	12	12	TH1	Threshold Selection Input 1. Logic input to select desired thresholds. Connect TH1 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
15	13	13	TH2	Threshold Selection Input 2. Logic input to select desired thresholds. Connect TH2 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
16	14	14	TH3	Threshold Selection Input 3. Logic input to select desired thresholds. Connect TH3 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
17	15	15	TH4	Threshold Selection Input 4. Logic input to select desired thresholds. Connect TH4 to GND or DBP. See Table 2 for available thresholds. Input has no internal pullup or pulldown.
18	16	16	SWT	Watchdog Timeout Adjust Input. Connect SWT to V_{CC} to select the default watchdog timeout period. Connect an external capacitor between SWT and GND to adjust the watchdog timeout period. The adjustable timeout period is calculated by t_{WP} = 4.348E6 x C_{SWT} (t_{WP} in seconds and C_{SWT} in Farads). Disable the watchdog timer by connecting SWT to GND.
19	17	17	SRT	Reset Timeout Adjust Input. Connect SRT to V_{CC} to select the default reset timeout period. Connect an external capacitor between SRT and GND to adjust the reset timeout period. The adjustable timeout period is calculated by t_{RP} = 4.348E6 x C_{SWT} (t_{RP} in seconds and C_{SRT} in Farads).
20	18	18	$\overline{\text{ENABLE}}$	Active-Low, PG_ Enable Input. Pull $\overline{\text{ENABLE}}$ high to force all PG_ outputs low. PG_ outputs remain asserted for their timeout period when $\overline{\text{ENABLE}}$ is driven/pulled low. $\overline{\text{ENABLE}}$ is internally pulled down to GND through a 10µA current sink.
21	19	19	V_{CC}	Internal Supply Voltage. Bypass V_{CC} to GND with a 1µF capacitor as close to the device as possible. V_{CC} supplies power to the internal circuitry. V_{CC} is internally powered from the highest of the monitored IN2–IN5 voltages. Do not use V_{CC} to supply power to external circuitry. To externally supply V_{CC}, see the *Powering the MAX6892/MAX6893/MAX6894* section.
22	20	20	DBP	Digital Bypass Voltage. DBP supplies power to the output stages. Bypass DBP to GND with a 1µF capacitor as close to the device as possible. Do not use DBP to supply power to external circuitry.
23	—	—	IN8	Input Voltage 8. Select undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN8 to GND with a 0.1µF capacitor as close to the device as possible.
24	—	—	IN7	Input Voltage 7. Select undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN7 to GND with a 0.1µF capacitor as close to the device as possible.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX6892	MAX6893	MAX6894		
25	21	—	IN6	Input Voltage 6. Select undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor as close to the device as possible.
26	22	—	IN5	Input Voltage 5. Select undervoltage threshold using TH0–TH4. See Table 2. Power the device through IN2–IN5 or V_{CC} (see the *Powering the MAX6892/MAX6893/MAX6894* section). For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor as close to the device as possible.
27	23	23	IN4	Input Voltage 4. Select undervoltage threshold using TH0–TH4. See Table 2. Power the device through IN2–IN5 or V_{CC} (see the *Powering the MAX6892/MAX6893/MAX6894* section). For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor as close to the device as possible.
28	24	24	IN3	Input Voltage 3. Select undervoltage threshold using TH0–TH4. See Table 2. Power the device through IN2–IN5 or V_{CC} (see the *Powering the MAX6892/MAX6893/MAX6894* section). For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor as close to the device as possible.
29	25	25	IN2	Input Voltage 2. Select undervoltage threshold using TH0–TH4. See Table 2. Power the device through IN2–IN5 or V_{CC} (see the *Powering the MAX6892/MAX6893/MAX6894* section). For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor as close to the device as possible.
30	26	26	IN1	Input Voltage 1. Select undervoltage threshold using TH0–TH4. See Table 2. For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor as close to the device as possible.
31	27	27	WDI	Watchdog Timer Input. Logic input for the watchdog timer function. If WDI is not strobed with a valid low-to-high or high-to-low transition within the watchdog timeout period, the watchdog output asserts low. The watchdog timeout period is externally adjustable with capacitor C_{SWT} or selectable for a fixed internal timeout period. The watchdog has a long timeout period (92.16s minimum fixed or 64x the adjusted short timeout period) after each reset event and a short timeout period (1.44s minimum or an adjusted timeout period) after the first valid WDI transition.
32	28	28	PG1	Open-Drain, Power-Good Output 1. PG1 asserts low when the voltage input at IN1 is below the pin-selectable/adjustable input threshold or $\overline{\text{ENABLE}}$ is pulled high. PG1 deasserts with a factory preset timeout period of 6.25ms.
—	—	5, 6, 21, 22	N.C.	No Connection. Not internally connected.
—	—	—	EP	Exposed Pad. Internally connected to GND. Connect EP to GND or leave unconnected.

Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

Functional Diagram



Detailed Description

The MAX6892/MAX6893/MAX6894 pin-selectable, multivoltage supply sequencers/supervisors monitor several voltage detector inputs and one watchdog input, asserting the outputs when the respective input thresholds have been reached or a timeout occurs. All versions have an enable manual reset and margin input disable. The MAX6892/MAX6893/MAX6894 voltage thresholds are selected by logic inputs and/or an external voltage-divider. A $\overline{RESET}$ output ensures all monitored inputs are above the pin-selected/adjustable thresholds. Watchdog and reset timeout periods can use factory default settings or are independently adjustable by connecting external capacitors. In addition, all devices can be powered through the voltage detector inputs alone, or externally supplied from a constant supply on the V_{CC} pin (see the *Powering the MAX6892/MAX6893/MAX6894* section). The outputs are factory configured as open drain.

Powering the MAX6892/MAX6893/MAX6894

The MAX6892/MAX6893/MAX6894 derive power from the voltage detector inputs: IN2–IN5 (MAX6892/MAX6893), IN2–IN4 (MAX6894), or through an externally supplied V_{CC}. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). The highest input voltage on IN2–IN5 (MAX6892/MAX6893)/IN2–IN4 (MAX6894) supplies power to the device. One of IN2–IN5 (MAX6889/MAX6890)/IN2–IN4 (MAX6891) or V_{CC} must be at least 2.7V to ensure proper operation.

Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

V_{CC} powers the analog circuitry and is the bypass connection for the MAX6892/MAX6893/MAX6894 internal supply. Bypass V_{CC} to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at V_{CC}, equals the maximum of IN2–IN5. If V_{CC} is externally supplied, V_{CC} must be at least 200mV higher than any voltage applied to IN2–IN5 and V_{CC} must be brought up first. V_{CC} always powers the device when all IN_ are factory set as "ADJ." Do not use the internally generated V_{CC} to provide power to external circuitry.

The MAX6892/MAX6893/MAX6894 also generate a digital supply voltage (DBP) for the internal logic circuitry and the output stages. Bypass DBP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is 2.55V. Do not use DBP to provide power to external circuitry.

Inputs

The MAX6892/MAX6893/MAX6894 contain multiple logic and voltage detector inputs. Each voltage detector input is monitored for undervoltage thresholds.

Voltage Detector Inputs (IN_)

The MAX6892/MAX6893/MAX6894 offer several monitor options with both pin-selectable and adjustable reset thresholds. The threshold voltage at each adjustable IN_ input is typically 0.6V. To monitor a voltage > 0.6V, connect a resistor-divider network to the circuit as shown in Figure 1:

$$V_{IN\_TH} = V_{TH} (R_1 + R_2)/R_2 \qquad \text{(Equation 1)}$$

where V_{IN_TH} is the desired reset threshold voltage for the respective IN_ and V_{TH} is the input threshold (0.6V).

Resistors R_1 and R_2 can have high values to minimize current consumption due to low-leakage currents. Set R_2 to some conveniently high value (10kΩ, for example) and calculate R_1 based on the desired reset threshold voltage, using the following formula:

$$R_1 = R_2 \times (V_{IN\_TH}/V_{TH} - 1)$$

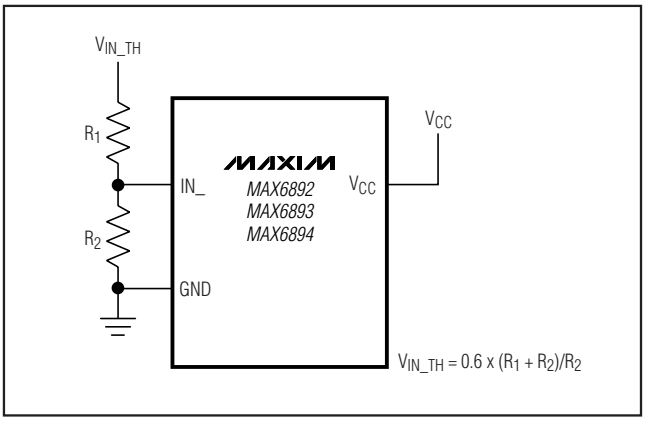


Figure 1. Adjusting the Monitored Threshold

Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

Threshold Logic Inputs (TH0–TH4)

The TH0–TH4 logic inputs select the undervoltage thresholds and tolerance of the IN1–IN8 inputs (MAX6892), IN1–IN6 inputs (MAX6893), and IN1–IN4 inputs (MAX6894). TH0–TH4 define 32 unique options for the supervisor functionality. Connect the respective TH_ to GND for a logic 0 or to DBP for a logic 1. Tables 1 and 2 show the 32 unique threshold options available. TH4 sets the threshold tolerance of the undervoltage threshold. A logic 1 selects a 5% supply tolerance and a logic 0 selects 10% supply tolerance. The MAX6892/MAX6893/MAX6894 logic determines which thresholds should be used for the IN inputs only at power-up. Use the voltage-divider circuit of Figure 1 and Equation 1 to set the threshold for the user-adjustable inputs as described in the *Voltage Detector Inputs (IN_)* section.

Table 1. Nominal Monitored Supply Voltages

SELECTION	TH4–TH0	MONITORED SUPPLY VOLTAGES (V)								SUPPLY TOLERANCE (%)
		IN1	IN2	IN3	IN4	IN5	IN6	IN7	IN8	
1	11111	ADJ	5	3.3	2.5	1.8	ADJ	ADJ	ADJ	5
2	11110	ADJ	5	3	2.5	1.8	ADJ	ADJ	ADJ	5
3	11101	ADJ	5	3.3	2.5	ADJ	ADJ	ADJ	ADJ	5
4	11100	ADJ	5	3	2.5	ADJ	ADJ	ADJ	ADJ	5
5	11011	ADJ	5	3.3	1.8	ADJ	ADJ	ADJ	ADJ	5
6	11010	ADJ	5	3	1.8	ADJ	ADJ	ADJ	ADJ	5
7	11001	ADJ	5	3.3	ADJ	ADJ	ADJ	ADJ	ADJ	5
8	11000	ADJ	5	3	ADJ	ADJ	ADJ	ADJ	ADJ	5
9	10111	ADJ	3.3	2.5	1.8	ADJ	ADJ	ADJ	ADJ	5
10	10110	ADJ	3	2.5	1.8	ADJ	ADJ	ADJ	ADJ	5
11	10101	ADJ	3.3	2.5	ADJ	ADJ	ADJ	ADJ	ADJ	5
12	10100	ADJ	3	2.5	ADJ	ADJ	ADJ	ADJ	ADJ	5
13	10011	ADJ	3.3	1.8	ADJ	ADJ	ADJ	ADJ	ADJ	5
14	10010	ADJ	3	1.8	ADJ	ADJ	ADJ	ADJ	ADJ	5
15	10001	ADJ	3.3	2.5	1.8	1.5	ADJ	ADJ	ADJ	5
16	10000	ADJ	3	2.5	1.8	1.5	ADJ	ADJ	ADJ	5
17	01111	ADJ	5	3.3	2.5	1.8	ADJ	ADJ	ADJ	10
18	01110	ADJ	5	3	2.5	1.8	ADJ	ADJ	ADJ	10
19	01101	ADJ	5	3.3	2.5	ADJ	ADJ	ADJ	ADJ	10
20	01100	ADJ	5	3	2.5	ADJ	ADJ	ADJ	ADJ	10
21	01011	ADJ	5	3.3	1.8	ADJ	ADJ	ADJ	ADJ	10
22	01010	ADJ	5	3	1.8	ADJ	ADJ	ADJ	ADJ	10
23	01001	ADJ	5	3.3	ADJ	ADJ	ADJ	ADJ	ADJ	10
24	01000	ADJ	5	3	ADJ	ADJ	ADJ	ADJ	ADJ	10
25	00111	ADJ	3.3	2.5	1.8	ADJ	ADJ	ADJ	ADJ	10
26	00110	ADJ	3	2.5	1.8	ADJ	ADJ	ADJ	ADJ	10
27	00101	ADJ	3.3	2.5	ADJ	ADJ	ADJ	ADJ	ADJ	10
28	00100	ADJ	3	2.5	ADJ	ADJ	ADJ	ADJ	ADJ	10
29	00011	ADJ	3.3	1.8	ADJ	ADJ	ADJ	ADJ	ADJ	10
30	00010	ADJ	3	1.8	ADJ	ADJ	ADJ	ADJ	ADJ	10
31	00001	ADJ	3.3	2.5	1.8	1.5	ADJ	ADJ	ADJ	10
32	00000	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	ADJ	—

Table 2. Threshold Options

SELECTION	TH4–TH0*	THRESHOLD VOLTAGES (V)							
		IN1	IN2	IN3	IN4	IN5	IN6	IN7	IN8
1	11111	0.60	4.62	3.06	2.31	1.67	0.60	0.60	0.60
2	11110	0.60	4.62	2.78	2.31	1.67	0.60	0.60	0.60
3	11101	0.60	4.62	3.06	2.31	0.60	0.60	0.60	0.60
4	11100	0.60	4.62	2.78	2.31	0.60	0.60	0.60	0.60
5	11011	0.60	4.62	3.06	1.67	0.60	0.60	0.60	0.60
6	11010	0.60	4.62	2.78	1.67	0.60	0.60	0.60	0.60
7	11001	0.60	4.62	3.06	0.60	0.60	0.60	0.60	0.60
8	11000	0.60	4.62	2.78	0.60	0.60	0.60	0.60	0.60
9	10111	0.60	3.06	2.31	1.8	0.60	0.60	0.60	0.60
10	10110	0.60	2.78	2.31	1.8	0.60	0.60	0.60	0.60
11	10101	0.60	3.06	2.31	0.60	0.60	0.60	0.60	0.60
12	10100	0.60	2.78	2.31	0.60	0.60	0.60	0.60	0.60
13	10011	0.60	3.06	1.67	0.60	0.60	0.60	0.60	0.60
14	10010	0.60	2.78	1.67	0.60	0.60	0.60	0.60	0.60
15	10001	0.60	3.06	2.31	1.67	1.39	0.60	0.60	0.60
16	10000	0.60	2.78	2.31	1.67	1.39	0.60	0.60	0.60
17	01111	0.60	4.38	2.88	2.19	1.58	0.60	0.60	0.60
18	01110	0.60	4.38	2.62	2.19	1.58	0.60	0.60	0.60
19	01101	0.60	4.38	2.88	2.19	0.60	0.60	0.60	0.60
20	01100	0.60	4.38	2.62	2.19	0.60	0.60	0.60	0.60
21	01011	0.60	4.38	2.88	1.58	0.60	0.60	0.60	0.60
22	01010	0.60	4.38	2.62	1.58	0.60	0.60	0.60	0.60
23	01001	0.60	4.38	2.88	0.60	0.60	0.60	0.60	0.60
24	01000	0.60	4.38	2.62	0.60	0.60	0.60	0.60	0.60
25	00111	0.60	2.88	2.19	1.8	0.60	0.60	0.60	0.60
26	00110	0.60	2.62	2.19	1.8	0.60	0.60	0.60	0.60
27	00101	0.60	2.88	2.19	0.60	0.60	0.60	0.60	0.60
28	00100	0.60	2.62	2.19	0.60	0.60	0.60	0.60	0.60
29	00011	0.60	2.88	1.58	0.60	0.60	0.60	0.60	0.60
30	00010	0.60	2.62	1.58	0.60	0.60	0.60	0.60	0.60
31	00001	0.60	2.88	2.19	1.58	1.31	0.60	0.60	0.60
32	00000	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60

**TH4 = '1' selects 7.5% threshold tolerance, TH4 = '0' selects 12.5% threshold tolerance.*
Contact factory for alternative thresholds.

Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

Watchdog Timer

The MAX6892/MAX6893/MAX6894s' watchdog circuit monitors the microprocessor's (µP's) activity. If the µP does not toggle the watchdog input (WDI) within the watchdog timeout period, the watchdog output ($\overline{WDO}$) asserts. The internal watchdog timer is cleared by $\overline{RESET}$, or by a transition at WDI (which can detect pulses as short as 50ns). The watchdog timer remains cleared while reset is asserted. The timer starts counting as soon as $\overline{WDO}$ is released (see Figure 2).

The MAX6892/MAX6893/MAX6894 feature two modes of watchdog timer operation: normal mode and initial mode. At power-up, after a reset event, or after the watchdog timer expires, the initial watchdog timeout is active. After the first transition on WDI, the normal watchdog timeout is active. The initial and normal watchdog timeouts are determined by the value of the capacitor connected between SWT and ground or by connecting SWT to V_{CC} (see the *Selecting the Reset and Watchdog Timeout Capacitor* section). The initial watchdog timeout is approximately 64 times the normal watchdog timeout. For example, in initial mode a 1µF capacitor gives a watchdog timeout period of about 5min.

If $\overline{WDO}$ is connected to $\overline{MR}$, the $\overline{WDO}$ asserts for a short duration (~5µs), long enough to assert the $\overline{RESET}$ output. Asserting $\overline{RESET}$ clears the watchdog timer and $\overline{WDO}$ goes high. The reset output remains asserted for its timeout period after a watchdog fault. The watchdog timer stays cleared as long as $\overline{RESET}$ is low.

The watchdog timeout period is determined by the value of the capacitor connected between SWT and ground (see the *Selecting the Reset/Watchdog Timeout Capacitor* section). Connect SWT to DBP to select factory-programmed watchdog timeout. To disable the watchdog timer connect SWT to GND.

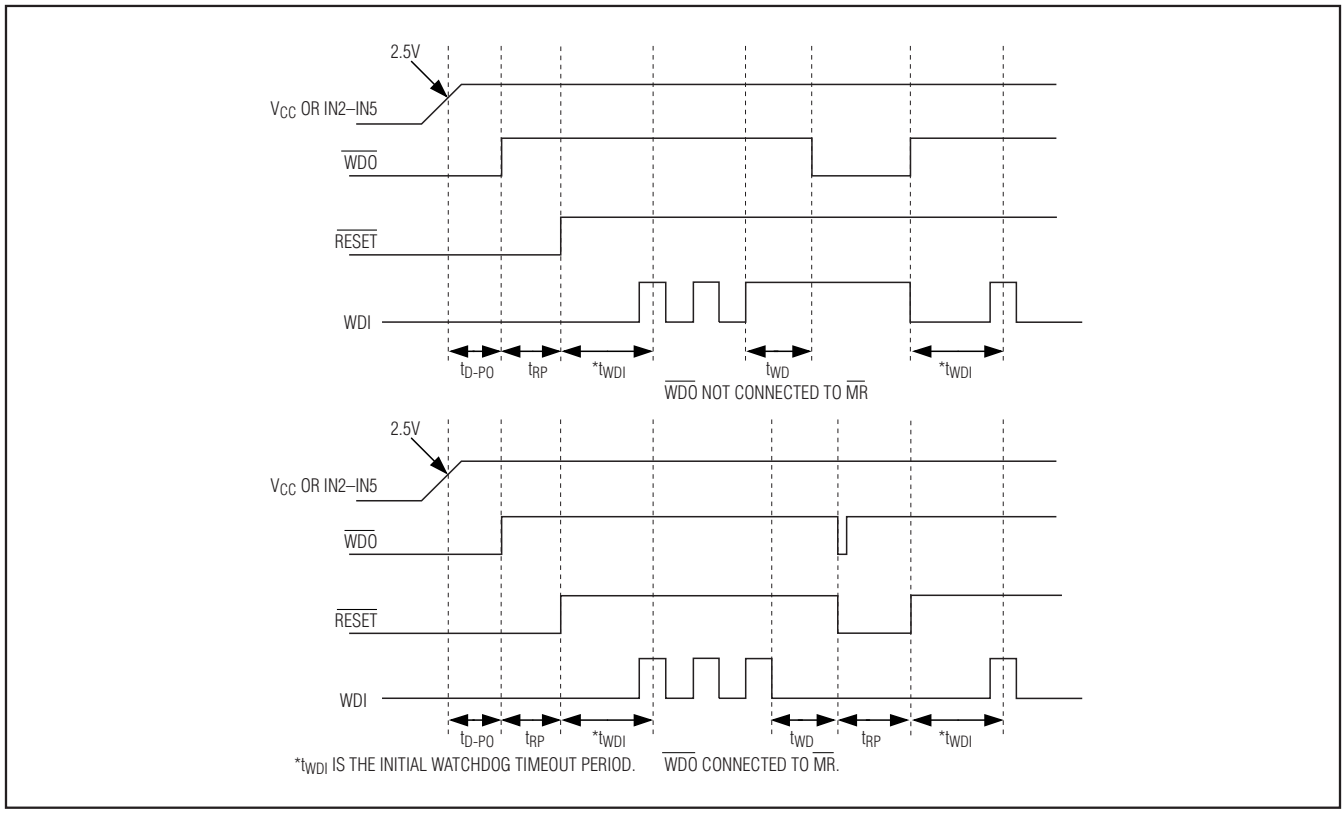


Figure 2. Watchdog, Reset, and Power-Up Timing Diagram

Manual Reset ($\overline{MR}$)

Many µP-based products require manual reset capability to allow an operator or external logic circuitry to initiate a reset. The manual reset input ($\overline{MR}$) can connect directly to a switch without an external pullup resistor or debouncing network. $\overline{MR}$ is internally pulled up to DBP through a 10µA current source and, therefore, can be left unconnected if unused.

$\overline{MR}$ is designed to reject fast falling transients (typically 100ns pulses) and it must be held low for a minimum of 1µs to assert $\overline{RESET}$. After $\overline{MR}$ transitions from low to high, $\overline{RESET}$ remains asserted for the duration of the reset timeout period.

Margin Output Disable ($\overline{MARGIN}$)

$\overline{MARGIN}$ allows system-level testing while power supplies exceed the normal ranges. Driving $\overline{MARGIN}$ low forces PG_, $\overline{RESET}$, and $\overline{WDO}$ to hold the last state while system-level testing occurs. Leave $\overline{MARGIN}$ unconnected or connect to DBP if unused. An internal 10µA current source pulls $\overline{MARGIN}$ to DBP. The state of each programmable output, $\overline{RESET}$, and $\overline{WDO}$ does not change while $\overline{MARGIN}$ = GND.

Enable Input

$\overline{ENABLE}$ is an active-low, logic input. Driving $\overline{ENABLE}$ high pulls all PG_ low. Drive $\overline{ENABLE}$ low or leave unconnected for normal operation. $\overline{ENABLE}$ is internally pulled down to GND through a 10µA current sink.

Power-Good Outputs

The MAX6892 features eight power-good outputs, the MAX6893 features six power-good outputs, and the MAX6894 features four power-good outputs. Each output (PG_) responds to its respective input (IN_). Each PG_ is open drain. During power-up, the outputs pull down to GND with an internal 10µA current sink for 1V < V_{CC} < V_{UVLO}.

$\overline{RESET}$ Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. The MAX6892/MAX6893/MAX6894 supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions.

$\overline{RESET}$ changes from high to low whenever one or more input voltage (IN1–IN8) monitors drop below their respective reset threshold voltage or when $\overline{MR}$ is pulled low for a minimum of 1µs. Once the affected input voltage monitor(s) exceeds its respective reset threshold voltage(s), $\overline{RESET}$ remains low for the reset timeout period, then deaaserts.

Applications Information

Selecting the Reset/Watchdog Timeout Capacitor

The reset timeout period can be adjusted to accommodate a variety of µP applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and ground. Calculate the reset timeout capacitor as follows:

$$C_{SRT} = t_{RP}/(4.348 \times 106)$$

with t_{RP} in seconds and C_{SRT} in Farads. Connect SRT to V_{CC} for a factory-programmed reset timeout of 200ms (typ).

The watchdog timeout period can be adjusted to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a specific value capacitor (C_{SWT}) between SWT and GND. For normal mode operation, calculate the watchdog timeout capacitor as follows:

$$C_{SWT} = t_{WD}/(4.348 \times 10^6)$$

with t_{WD} in seconds and C_{SWT} in Farads. Connect SWT to V_{CC} for a factory-programmed watchdog timeout of 1.6s (normal mode) and 102.4s (initial mode).

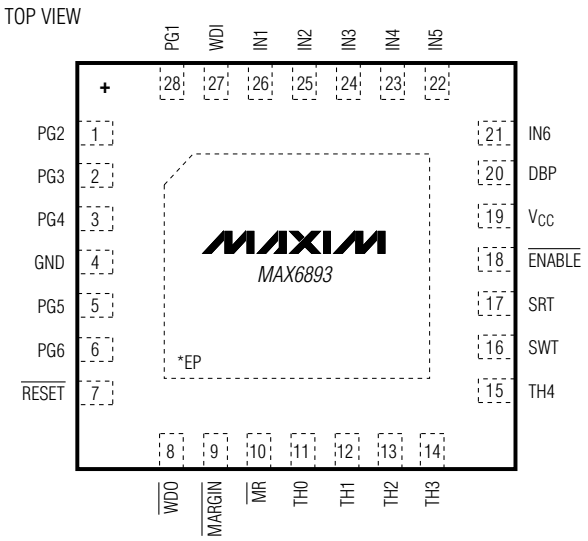
C_{SRT} and C_{SWT} must be a low-leakage (< 10nA) type capacitor. Ceramic capacitors are recommended.

Layout and Bypassing

For better noise immunity, bypass each of the voltage detector inputs to GND with 0.1µF capacitors installed as close to the device as possible. Bypass V_{CC} and DBP to GND with 1µF capacitors installed as close to the device as possible.

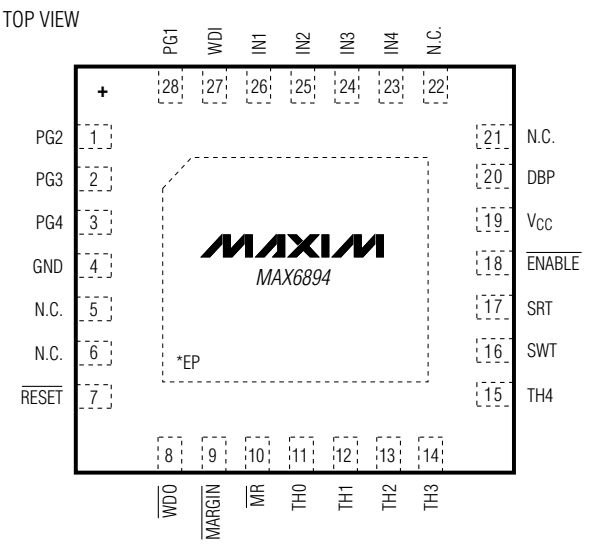
Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

Pin Configuration (continued)



THIN QFN

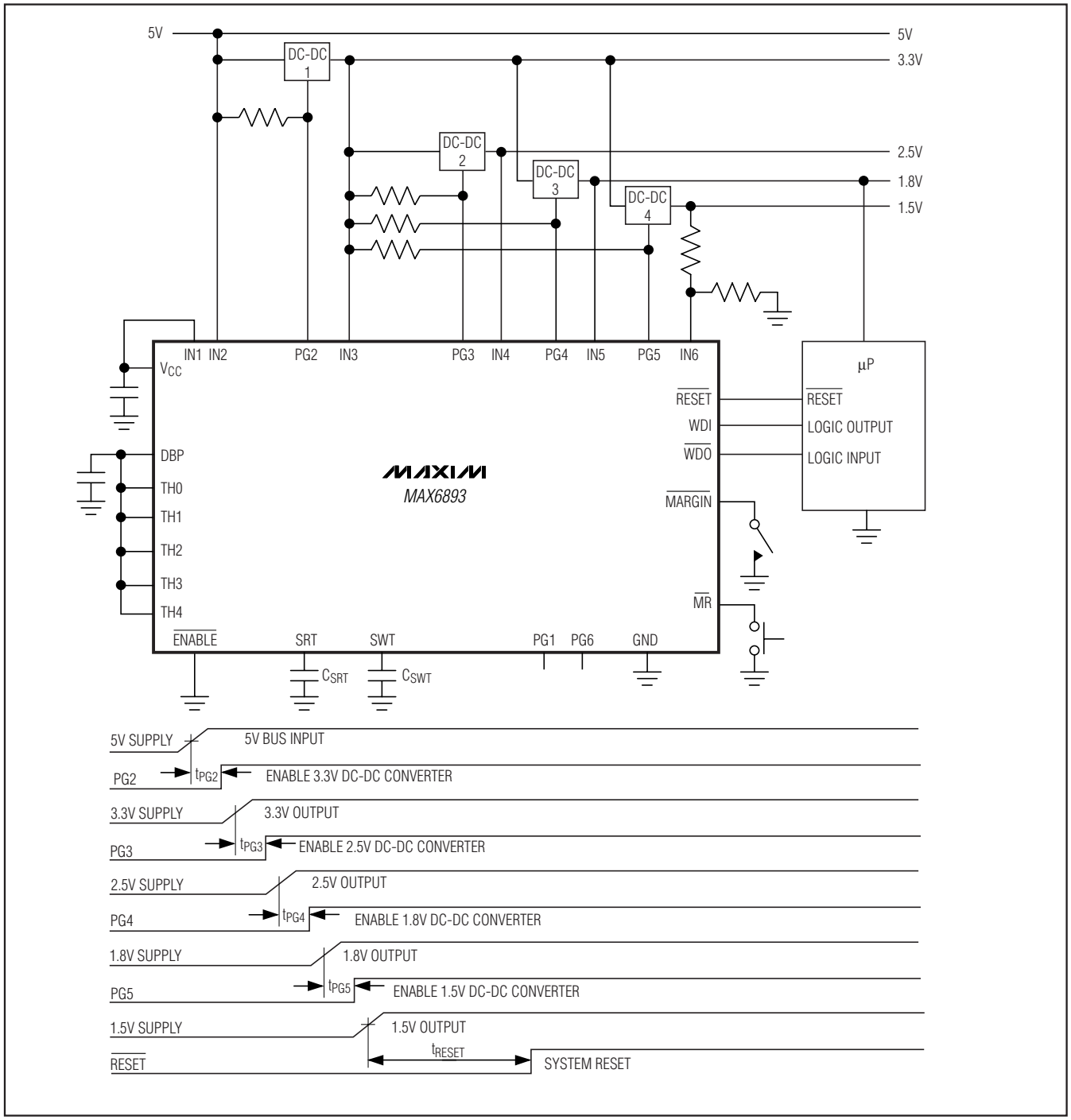
*EXPOSED PAD INTERNALLY CONNECTED TO GND.



THIN QFN

*EXPOSED PAD INTERNALLY CONNECTED TO GND.

Typical Operating Circuit



Pin-Selectable, Octal/Hex/Quad, Power-Supply Sequencers/Supervisors

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 Thin QFN	T2855+8	21-0140	90-0028
32 Thin QFN	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/05	Initial release	—
1	9/10	Add lead-free package, add exposed pad info, update *Absolute Maximum Ratings*, style edits	1–6, 8–11, 13, 15, 16, 18, 19

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