

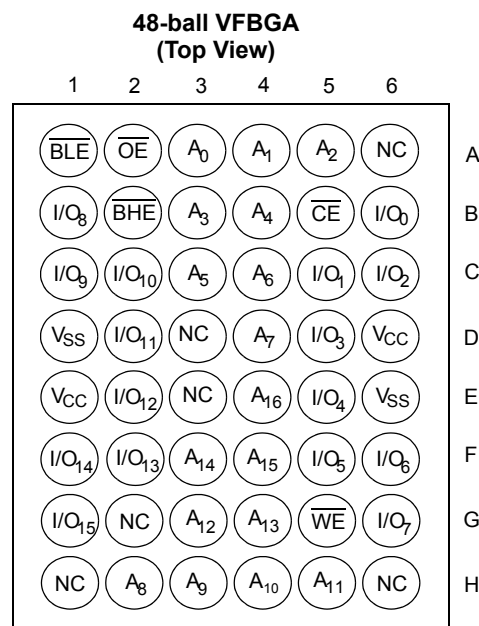
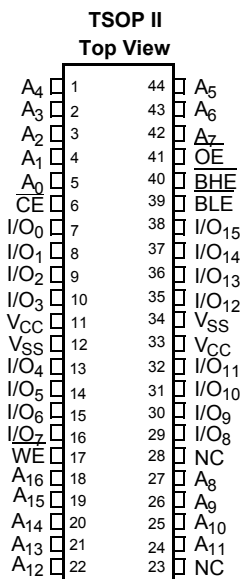
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### Selection Guide

	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current	10	mA

### Pin Configurations



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage on  $V_{CC}$  to relative GND<sup>[3]</sup> ..... -0.3 V to +4.6 V  
 DC voltage applied to outputs in high Z State<sup>[3]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V  
 DC input voltage<sup>[3]</sup> ..... -0.3 V to  $V_{CC} + 0.3$  V

Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage ..... > 2001 V (per MIL-STD-883, method 3015)  
 Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

## DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit	
			Min	Max		
$V_{OH}$	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	V	
$V_{OL}$	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	-	0.4	V	
$V_{IH}$	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V	
$V_{IL}$	Input LOW voltage <sup>[2]</sup>		-0.3	0.8	V	
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	µA	
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	µA	
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}$	100 MHz	-	90	mA
			83 MHz	-	80	
			66 MHz	-	70	
			40 MHz	-	60	
$I_{SB1}$	Automatic CE Power-down Current — TTL Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$	-	20	mA	
$I_{SB2}$	Automatic CE Power-down Current — CMOS Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.3 \text{ V}$ , or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$	-	10	mA	

## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	8	pF
$C_{OUT}$	I/O capacitance		8	pF

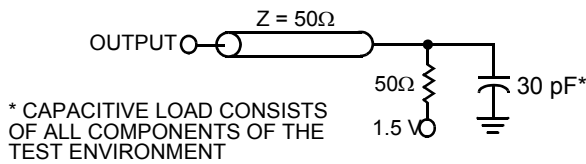
## Thermal Resistance<sup>[3]</sup>

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	50.66	27.89	°C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case)		17.17	14.74	°C/W

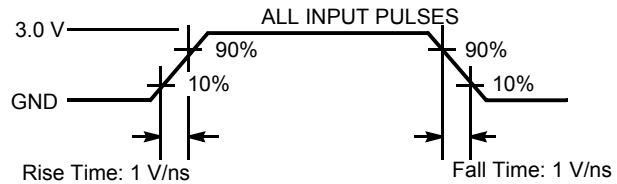
### Notes

- $V_{IL}(\text{min}) = -2.0 \text{ V}$  and  $V_{IH}(\text{max}) = V_{CC} + 2 \text{ V}$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms<sup>[4]</sup>

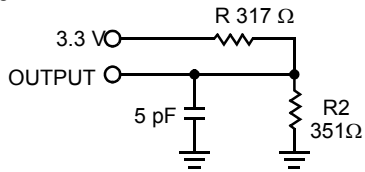


(a)



(b)

High Z characteristics:



(c)

### AC Switching Characteristics

Over the Operating Range<sup>[5]</sup>

Parameter	Description	-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}^{[6]}$	$V_{CC}$ (typical) to the first access	100	–	$\mu$ S
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low Z	0	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[7, 8]</sup>	–	5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low Z <sup>[8]</sup>	3	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high Z <sup>[7, 8]</sup>	–	5	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down	–	10	ns
$t_{DBE}$	Byte enable to data valid	–	5	ns
$t_{LZBE}$	Byte enable to low Z	0	–	ns
$t_{HZBE}$	Byte disable to high Z	–	6	ns

**Notes**

- AC characteristics (except high Z) are tested using the load conditions shown in (a). High Z characteristics are tested for all speeds using the test load shown in (c).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access is performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$  and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.

## AC Switching Characteristics

Over the Operating Range<sup>[5]</sup> (continued)

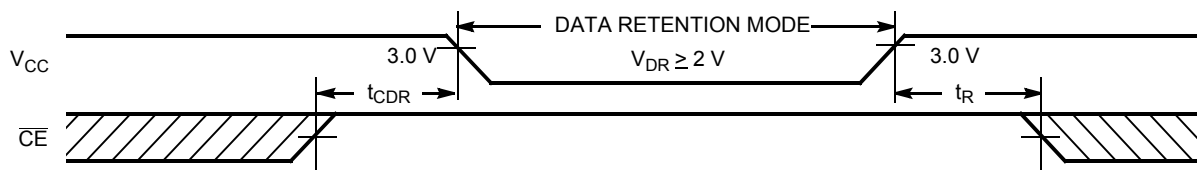
Parameter	Description	-10		Unit
		Min	Max	
<b>Write Cycle<sup>[9, 10]</sup></b>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	7	–	ns
$t_{AW}$	Address set-up to write end	7	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address set-up to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	ns
$t_{SD}$	Data set-up to write end	5	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[12]</sup>	3	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[11, 12]</sup>	–	5	ns
$t_{BW}$	Byte enable to end of write	7	–	ns

## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions <sup>[13]</sup>	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	V
$I_{CCDR}$	Data retention current		–	10	mA
$t_{CDR}$ <sup>[14]</sup>	Chip deselect to data retention time	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	0	–	ns
$t_R$ <sup>[15]</sup>	Operation recovery time		$t_{RC}$	–	ns

## Data Retention Waveform

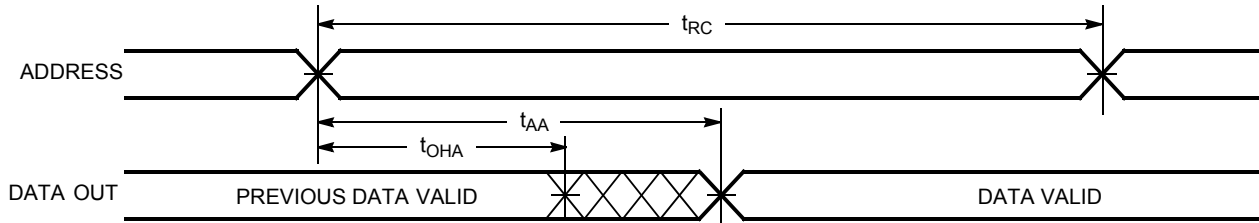


### Notes

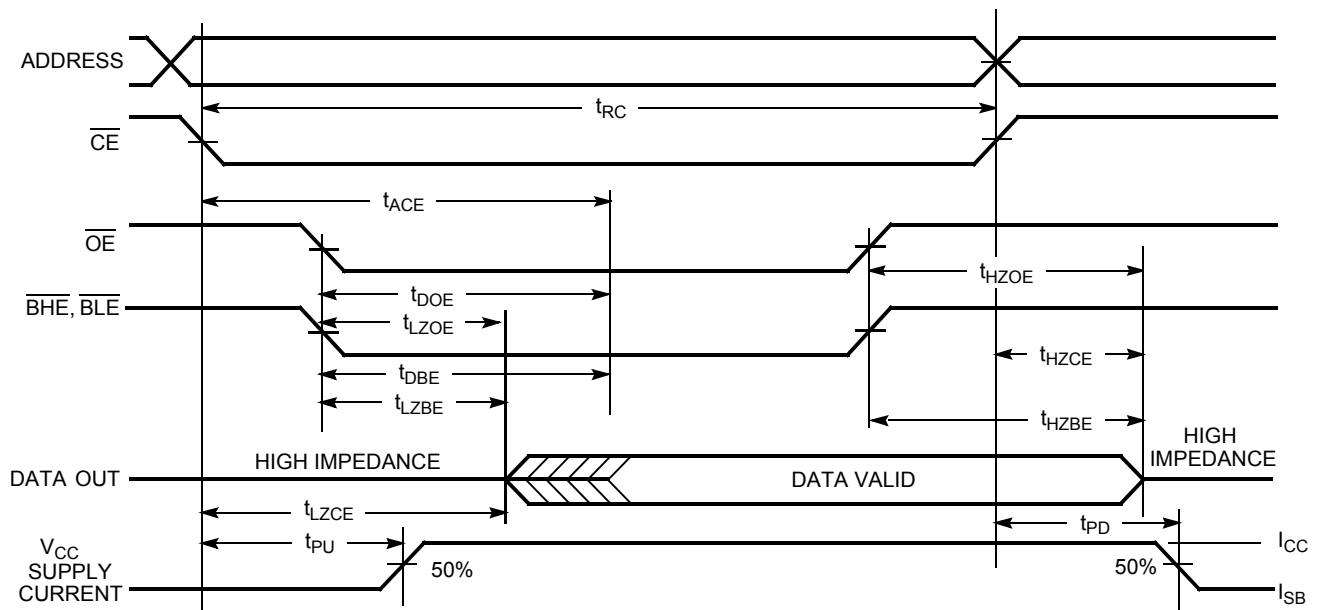
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 4 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$  and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- No input may exceed  $V_{CC} + 0.3\text{ V}$ .
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(\text{min.})} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(\text{min.})} \geq 50\ \mu\text{s}$ .

### Switching Waveforms

#### Read Cycle No. 1<sup>[16, 17]</sup>



#### Read Cycle No. 2 ( $\overline{OE}$ Controlled)<sup>[17, 18]</sup>

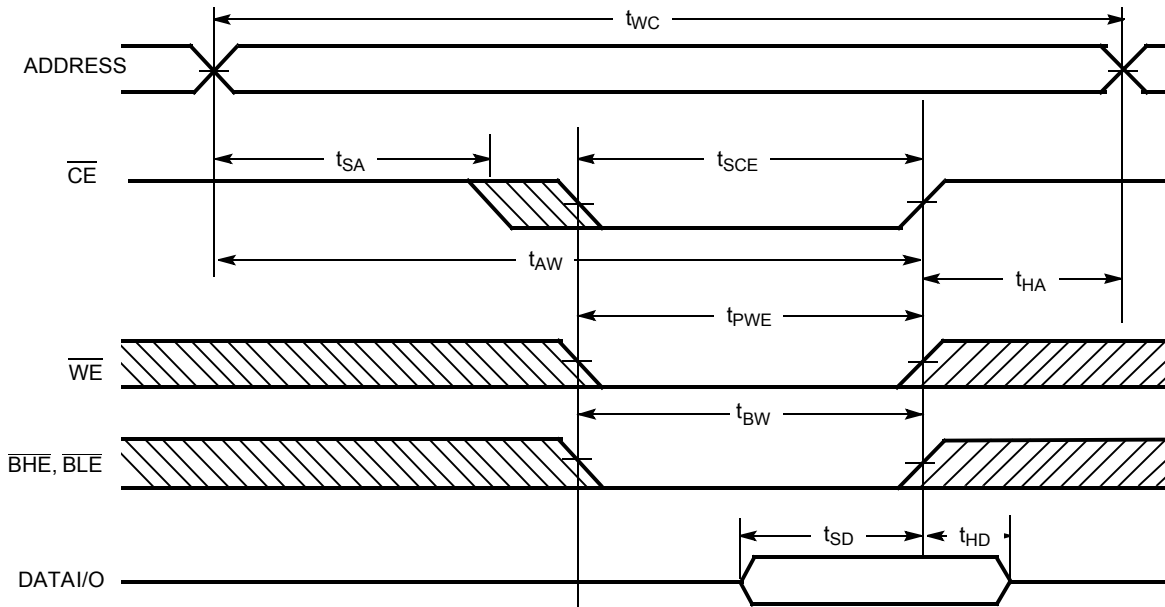


**Notes**

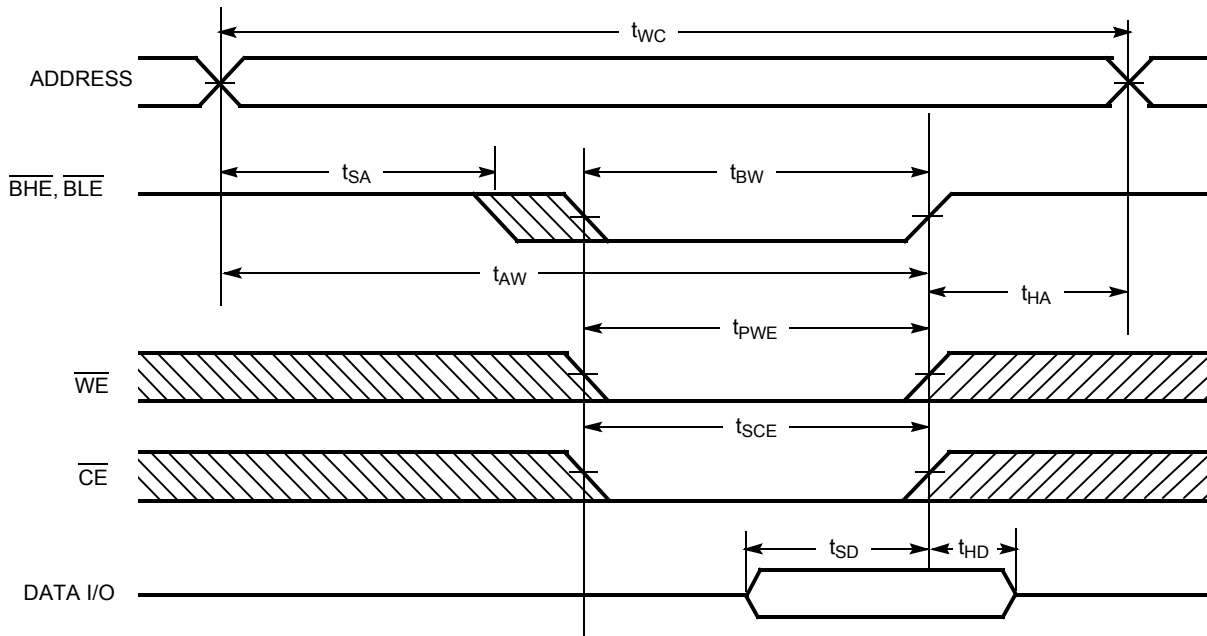
- 16. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
- 17. WE is HIGH for read cycle.
- 18. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[19, 20]</sup>



Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)

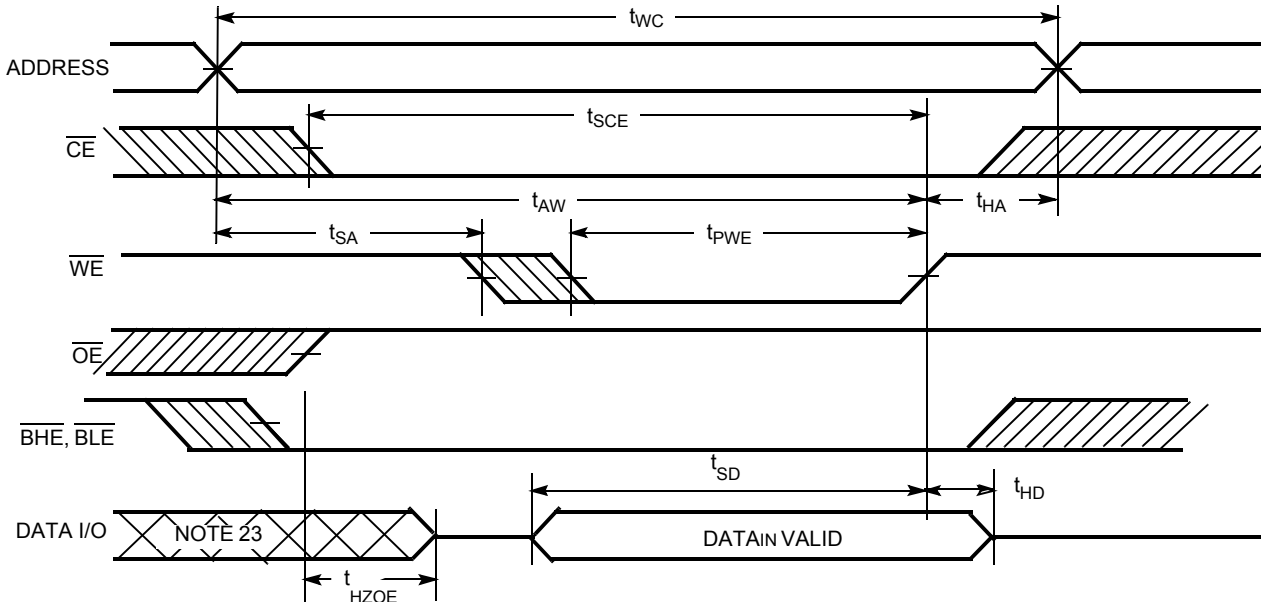


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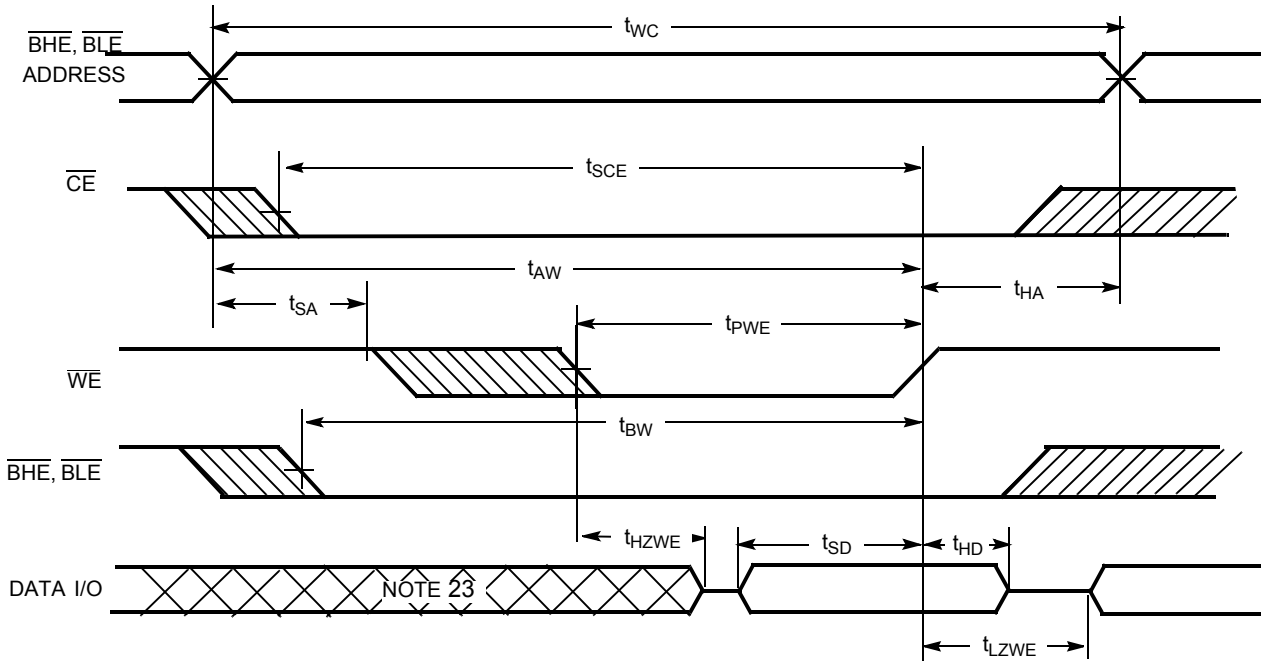
- 19. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 20. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[21, 22]</sup>



Write Cycle No. 4 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)



Notes

- 21. Data I/O is high-impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
- 22. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 23. During this period the I/Os are in the output state and input signals should not be applied.

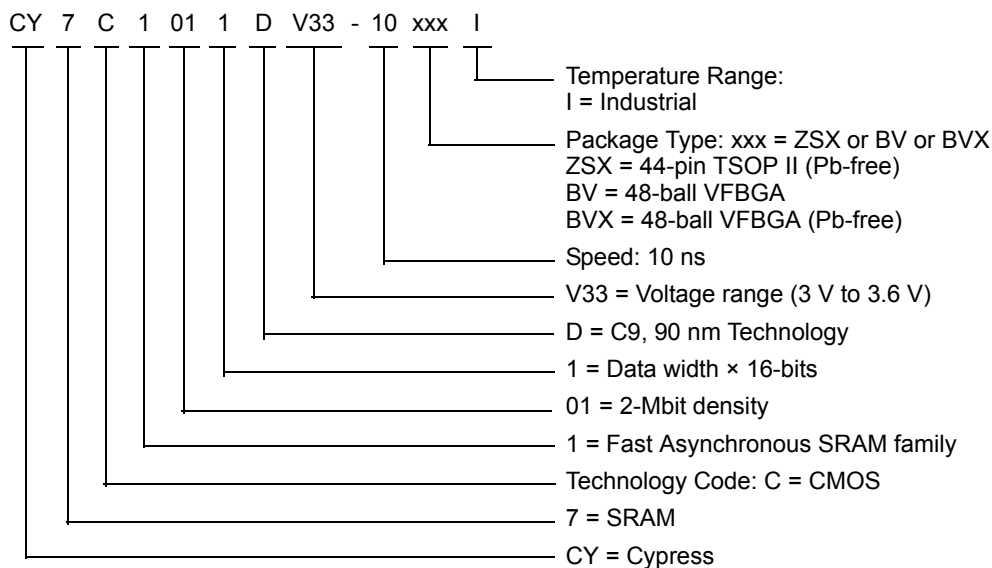


**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data Out	High Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	H	H	L	High Z	Data Out	Read upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write all bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data In	High Z	Write lower bits only	Active (I <sub>CC</sub> )
L	X	L	H	L	High Z	Data In	Write upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1011DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
	CY7C1011DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	

**Ordering Code Definitions**


Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 1. 44-pin TSOP II, 51-85087

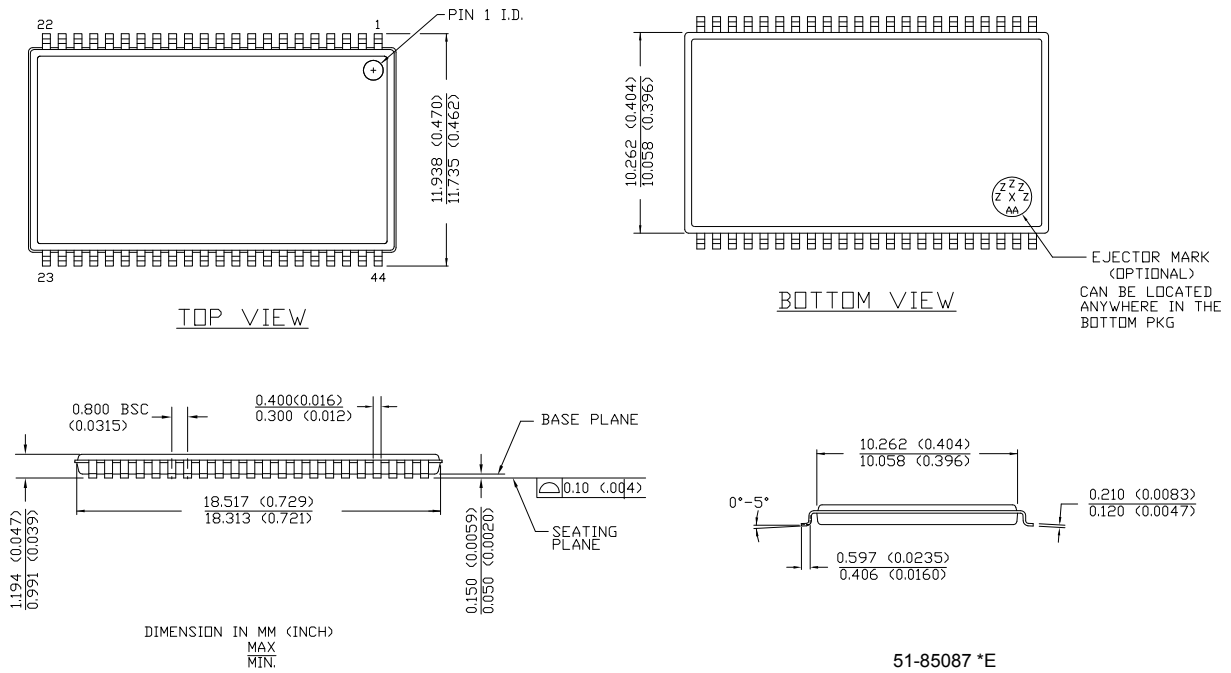
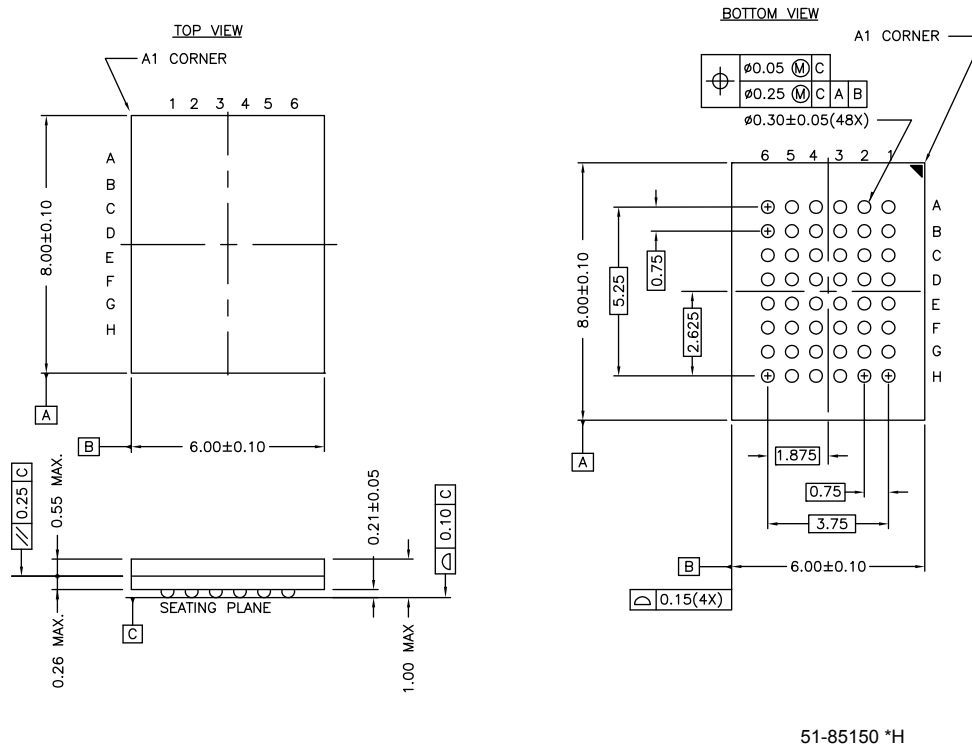


Figure 2. 48-ball VFBGA (6 × 8 × 1 mm), 51-85150



**Acronyms**

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
WE	write enable

**Document Conventions**

**Units of Measure**

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μs	micro seconds
μA	micro Amperes
mA	milli Amperes
MHz	Mega Hertz
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

Document History

Document Title: CY7C1011DV33 2-Mbit (128 K × 16) Static RAM				
Document Number: 38-05609				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	250650	See ECN	RKF	New Data Sheet
*A	399070	See ECN	NXR	<p>Changed from Advance to Preliminary</p> <p>Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court"</p> <p>Removed TQFP Package from product offering</p> <p>Removed -15 speed bin</p> <p>Corrected DC voltage limits in maximum ratings section from -0.5 to -0.3V and <math>V_{CC} +0.5V</math> to <math>V_{CC} +0.3V</math></p> <p>Redefined <math>I_{CC}</math> values for Com'l and Ind'l temperature ranges</p> <p><math>I_{CC}</math> (Com'l): Changed from 100, 80 and 70 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively</p> <p><math>I_{CC}</math> (Ind'l): Changed from 80 and 70 mA to 90 and 85 mA for 10 and 12ns speed bins respectively</p> <p>Modified Note# 4 on AC Test Loads</p> <p>Added Static Discharge Voltage and latch-up current spec</p> <p>Added <math>V_{IH(max)}</math> spec in Note# 2</p> <p>Changed reference voltage level for measurement of Hi-Z parameters from <math>\pm 500</math> mV to <math>\pm 200</math> mV</p> <p>Added Data Retention Characteristics Table and footnote on <math>t_R</math></p> <p>Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram</p> <p>Changed package name for 44-pin TSOP II from Z to ZS</p> <p>Added 8 ns parts in the Ordering Information table</p> <p>Shaded Ordering Information Table</p>
*B	459073	See ECN	NXR	<p>Converted Preliminary to Final.</p> <p>Removed -8 and -12 Speed bins</p> <p>Removed Commercial Operating Range from product offering.</p> <p>Changed the description of <math>I_{IX}</math> from "Input Load Current" to "Input Leakage Current"</p> <p>Updated the Thermal Resistance table.</p> <p>Changed <math>t_{HZBE}</math> from 5 ns to 6 ns.</p> <p>Updated footnote #7 on High-Z parameter measurement</p> <p>Added footnote #12.</p> <p>Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.</p>
*C	480177	See ECN	VKN	Added -10BVI product ordering code in the Ordering Information table.
*D	3059162	10/14/2010	PRAS	<p>Added <a href="#">Ordering Code Definitions</a>.</p> <p>Updated <a href="#">Package Diagrams</a>.</p>
*E	3098812	12/01/2010	PRAS	<p>Added <a href="#">Acronyms and Units of Measure</a>.</p> <p>Minor edits and updated in new template.</p>
*F	3861347	01/08/2013	TAVA	<p>Updated <a href="#">Ordering Information</a> (Updated part numbers).</p> <p>Updated <a href="#">Package Diagrams</a>:</p> <p>spec 51-85087 – Changed revision from *C to *E.</p> <p>spec 51-85150 – Changed revision from *F to *H.</p>

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