

# MAX941/MAX942/ MAX944

# High-Speed, Low-Power, 3V/5V, Rail-to-Rail, Single-Supply Comparators

## Absolute Maximum Ratings

### Power-Supply Ranges

Supply Voltage $V+$ to GND	+6.5V
Differential Input Voltage	-0.3V to ( $V+ + 0.3V$ )
Common-Mode Input Voltage	-0.3V to ( $V+ + 0.3V$ )
LATCH Input (MAX941 only)	-0.3V to ( $V+ + 0.3V$ )
SHDN Control Input (MAX941 only)	-0.3V to ( $V+ + 0.3V$ )

Current Into Input Pins .....  $\pm 20\text{mA}$

### Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )

8-Pin Plastic DIP (derate 9.09mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ )	..727mW
8-Pin SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$ )	.....471mW

8-Pin  $\mu\text{MAX}$  (derate 4.1mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ).....330mW

14-Pin Plastic DIP (derate 10.00mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ )..800mW

14-Pin SO (derate 8.33mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ).....667mW

### Operating Temperature Ranges

MAX94\_C\_..... $0^\circ\text{C}$  to  $+70^\circ\text{C}$

MAX94\_E\_..... $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

MAX94\_AUA..... $-40^\circ\text{C}$  to  $+125^\circ\text{C}$

MAX942MSA..... $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

Storage Temperature Range..... $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

Lead Temperature (soldering, 10s)..... $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical Characteristics

( $V+ = 2.7\text{V}$  to  $5.5\text{V}$ ,  $T_A = T_{\text{MIN}}$  to  $T_{\text{MAX}}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 14)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
Positive Supply Voltage	$V+$			2.7		5.5	V	
Input Voltage Range	$V_{\text{CMR}}$	(Note 1)		-0.2		$V+ + 0.2$	V	
Input-Referred Trip Points	$V_{\text{TRIP}}$	$V_{\text{CM}} = 0\text{V}$ or $V_{\text{CM}} = V+$ (Note 2)	$T_A = +25^\circ\text{C}$	MAX94_C_-, MAX94_EP_, MAX94_ES_, MAX942MSA	1	3	mV	
				MAX941_UA/MAX942_UA	1	4		
		$T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$		MAX94_C_-, MAX94_EP_, MAX94_ES_, MAX942MSA		4		mV
				MAX941_UA/MAX942_UA		6		
Input Offset Voltage	$V_{\text{OS}}$	$V_{\text{CM}} = 0\text{V}$ or $V_{\text{CM}} = V+$ (Note 3)	$T_A = +25^\circ\text{C}$	MAX94_C_-, MAX94_EP_, MAX94_ES_, MAX942MSA	1	2	mV	
				MAX941_UA/MAX942_UA	1	3		
		$T_A = T_{\text{MIN}}$ to $T_{\text{MAX}}$		MAX94_C_-, MAX94_EP_, MAX94_ES_, MAX942MSA		3		mV
				MAX941_UA/MAX942_UA		5.5		
Input Bias Current	$I_{\text{B}}$	$V_{\text{IN}} = V_{\text{OS}}$ , $V_{\text{CM}} = 0\text{V}$ or $V_{\text{CM}} = V+$ (Note 4)		MAX94_C	150	300	nA	
				MAX94_E/A, MAX942MSA	150	400		
Input Offset Current	$I_{\text{OS}}$	$V_{\text{IN}} = V_{\text{OS}}$ , $V_{\text{CM}} = 0\text{V}$ or $V+$		10	150	nA		
Input Differential Clamp Voltage	$V_{\text{CLAMP}}$	Force $100\mu\text{A}$ into $\text{IN}+$ , $\text{IN}- = \text{GND}$ , measure $V_{\text{IN}+} - V_{\text{IN}-}$ , Figure 3		2.2			V	
Common-Mode Rejection Ratio	CMRR	(Note 5)		MAX94_C_-, MAX94_EP_, MAX94_ES_, MAX942MSA	80	300	$\mu\text{V}/\text{V}$	
				MAX941_UA/MAX942_UA	80	800		
Power-Supply Rejection Ratio	PSRR	$2.7\text{V} \leq V+ \leq 5.5\text{V}$ , $V_{\text{CM}} = 0\text{V}$		MAX94_C_-, MAX94_EP_, MAX94_ES_, MAX942MSA	80	300	$\mu\text{V}/\text{V}$	
				MAX941_UA/MAX942_UA	80	350		
Output High Voltage	$V_{\text{OH}}$	$I_{\text{SOURCE}} = 400\mu\text{A}$		$V+ - 0.4$	$V+ - 0.2$		V	
		$I_{\text{SOURCE}} = 4\text{mA}$		$V+ - 0.4$	$V+ - 0.3$			
Output Low Voltage	$V_{\text{OL}}$	$I_{\text{SINK}} = 400\mu\text{A}$		0.2	0.4		V	
		$I_{\text{SINK}} = 4\text{mA}$		0.3	0.4			
Output Leakage Current	$I_{\text{LEAK}}$	(Note 6)				1	$\mu\text{A}$	

**Electrical Characteristics (continued)**

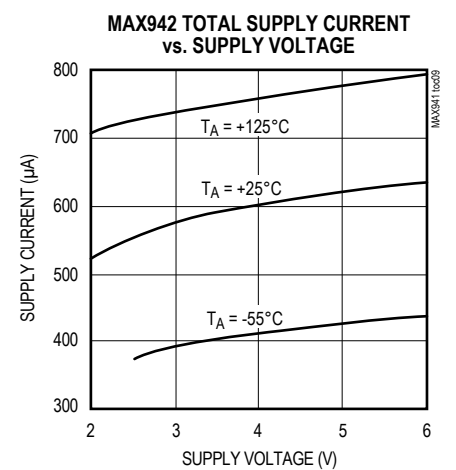
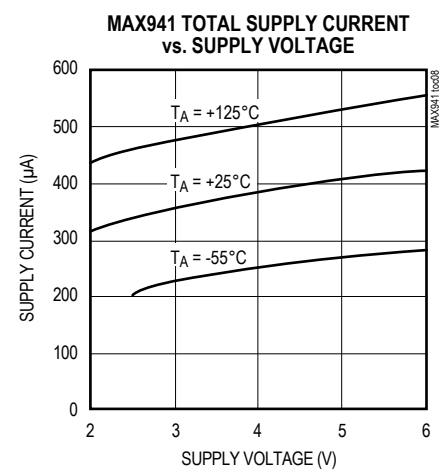
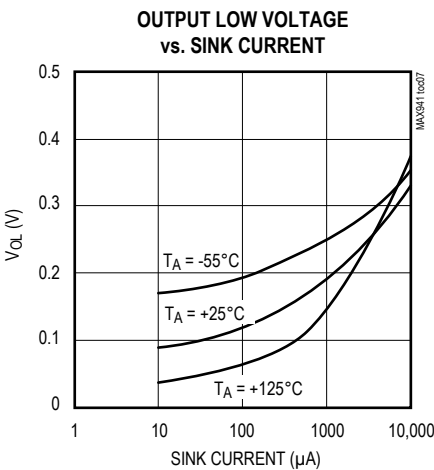
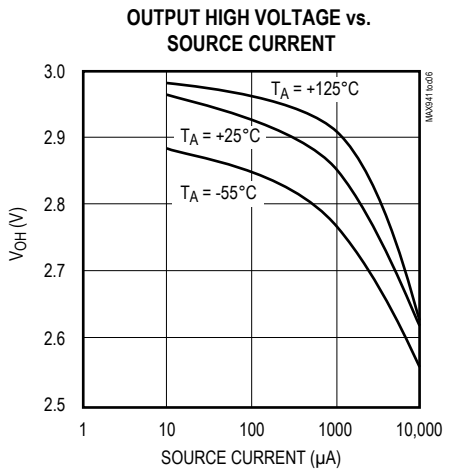
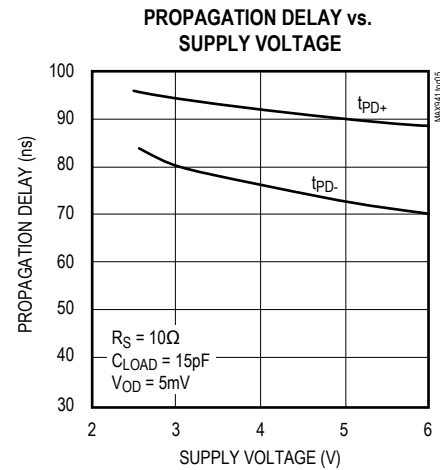
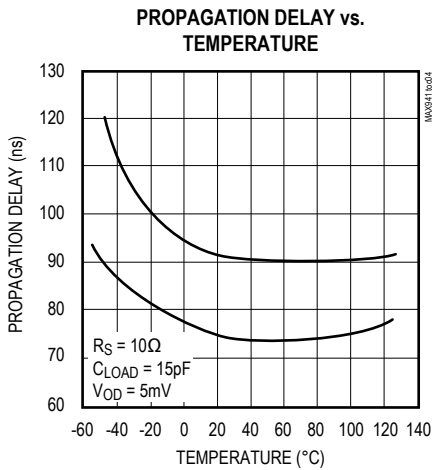
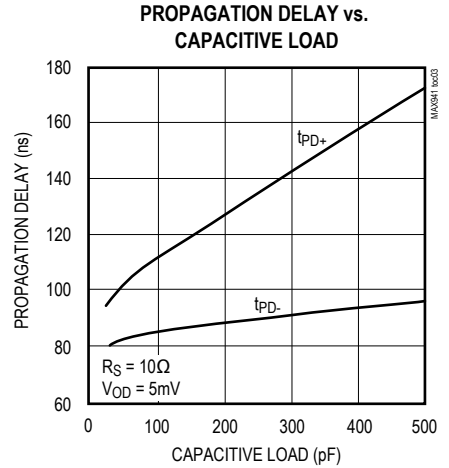
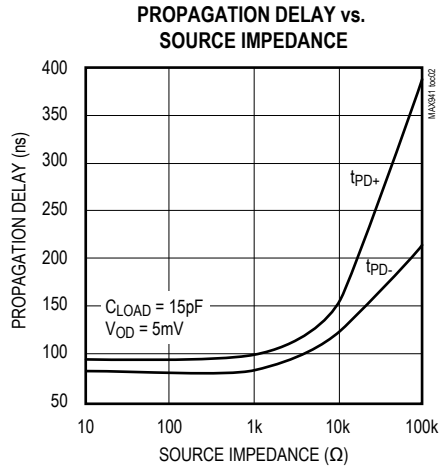
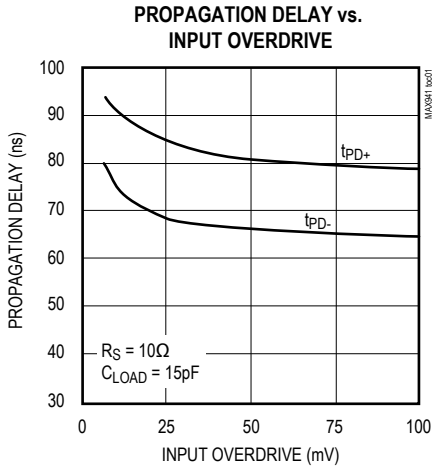
(V+ = 2.7V to 5.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 14)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current per Comparator	I <sub>CC</sub>	V+ = 3V	MAX941		380	600	μA
			MAX942/MAX944		350	500	
		V+ = 5V	MAX941		430	700	
			MAX942/MAX944		400	600	
		MAX941 only, shutdown mode (V+ = 3V)			12	60	
Power Dissipation per Comparator	PD	(Note 7)	MAX941		1.0	4.2	mW
			MAX942/MAX944		1.0	3.6	
Propagation Delay	t <sub>PD+</sub> , t <sub>PD-</sub>	(Note 8)	MAX94_C		80	150	ns
			MAX94_E/A, MAX942MSA		80	200	
Differential Propagation Delay	dt <sub>PD</sub>	(Note 9)			10		ns
Propagation Delay Skew		(Note 10)			10		ns
Logic-Input Voltage High	V <sub>IH</sub>	(Note 11)			V+/2 + 0.4		V
Logic-Input Voltage Low	V <sub>IL</sub>	(Note 11)				V+/2 - 0.4	V
Logic-Input Current	I <sub>IL</sub> , I <sub>IH</sub>	V <sub>LOGIC</sub> = 0V or V+ (Note 11)			2	10	μA
Data-to-Latch Setup Time	t <sub>S</sub>	(Note 12)			20		ns
Latch-to-Data Hold Time	t <sub>H</sub>	(Note 12)			30		ns
Latch Pulse Width	t <sub>LPW</sub>	MAX941 only			50		ns
Latch Propagation Delay	t <sub>LPD</sub>	MAX941 only			70		ns
Shutdown Time		(Note 13)			3		ns
Shutdown Disable Time		(Note 13)			10		ns

- Note 1:** Inferred from the CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.
- Note 2:** The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone (see Figure 1).
- Note 3:** V<sub>OS</sub> is defined as the center of the input-referred hysteresis zone (see Figure 1).
- Note 4:** The polarity of IB reverses direction as V<sub>CM</sub> approaches either supply rail. See *Typical Operating Characteristics* for more detail.
- Note 5:** Specified over the full common-mode range (V<sub>CMR</sub>).
- Note 6:** Applies to the MAX941 only when in shutdown mode. Specification is for current flowing into or out of the output pin for V<sub>OUT</sub> driven to any voltage from V+ to GND.
- Note 7:** Typical power dissipation specified with V+ = 3V; maximum with V+ = 5.5V.
- Note 8:** Parameter is guaranteed by design and specified with V<sub>OD</sub> = 5mV and C<sub>LOAD</sub> = 15pF in parallel with 400μA of sink or source current. V<sub>OS</sub> is added to the overdrive voltage for low values of overdrive (see Figure 2).
- Note 9:** Specified between any two channels in the MAX942/MAX944.
- Note 10:** Specified as the difference between t<sub>PD+</sub> and t<sub>PD-</sub> for any one comparator.
- Note 11:** Applies to the MAX941 only for both SHDN and LATCH pins.
- Note 12:** Applies to the MAX941 only. Comparator is active with LATCH pin driven high and is latched with LATCH pin driven low (see Figure 2).
- Note 13:** Applicable to the MAX941 only. Comparator is active with SHDN pin driven high and is in shutdown with SHDN pin driven low. Shutdown disable time is the delay when SHDN is driven high to the time the output is valid.
- Note 14:** The MAX941\_UA and MAX942\_UA are 100% production tested at T<sub>A</sub> = +25°C. Specifications over temperature are guaranteed by design.

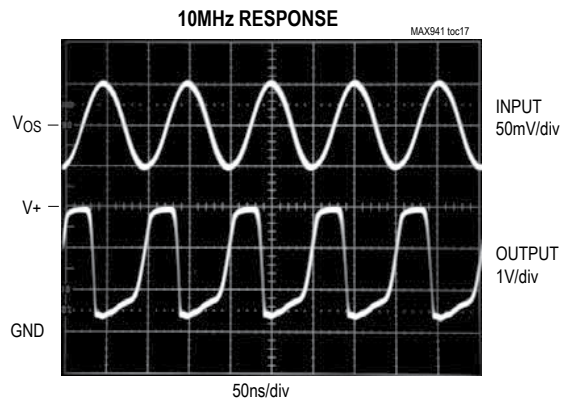
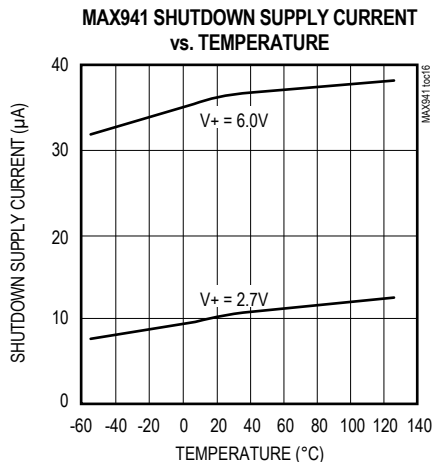
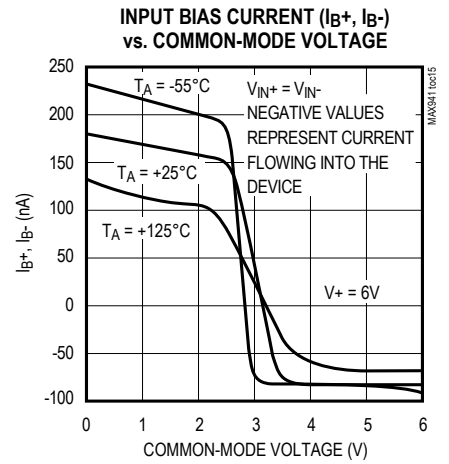
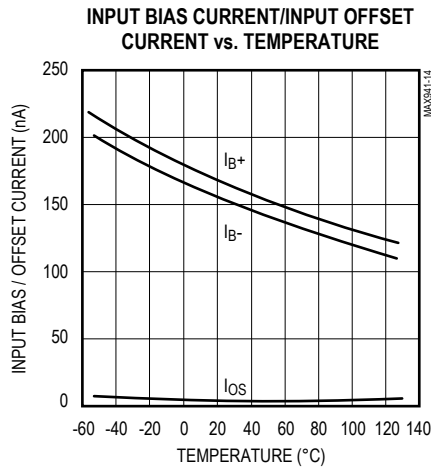
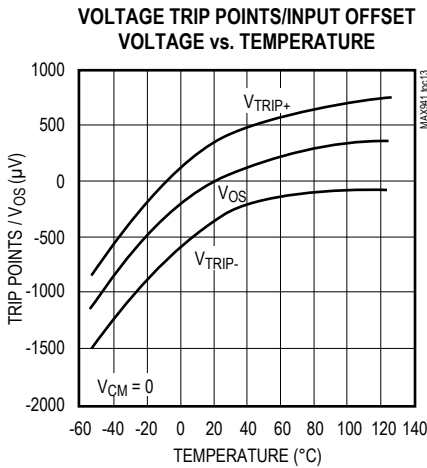
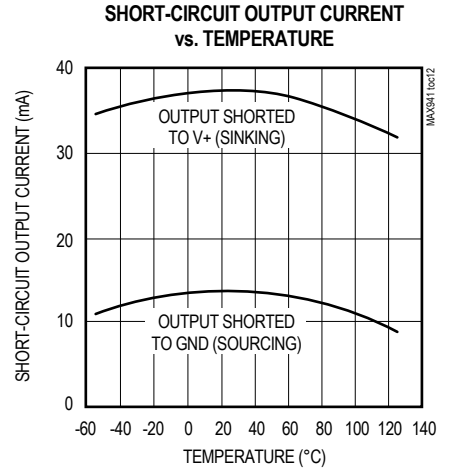
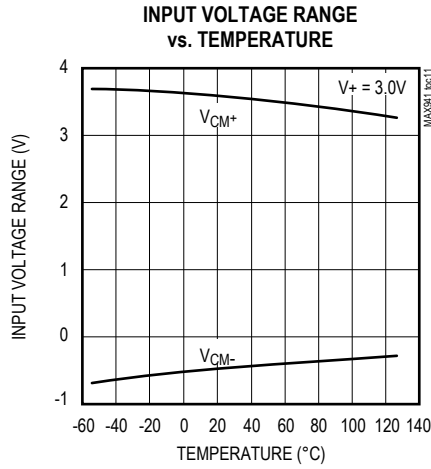
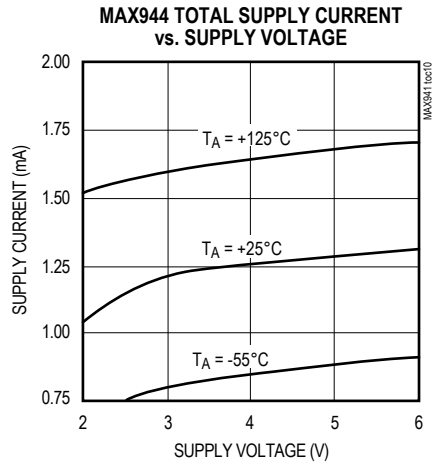
Typical Operating Characteristics

( $V_+ = 3.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



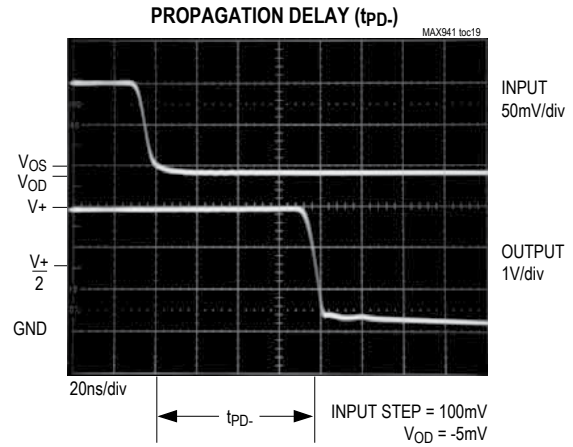
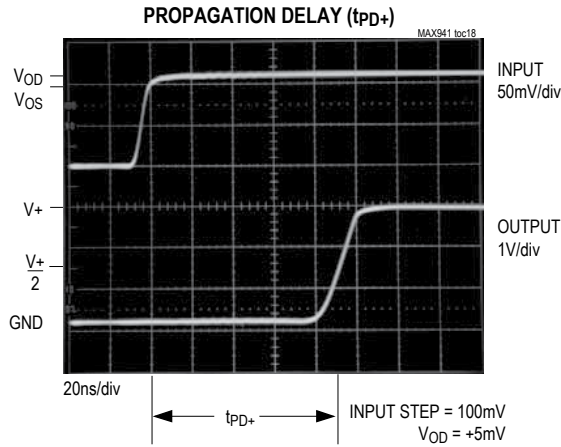
Typical Operating Characteristics (continued)

( $V_+ = 3.0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



Typical Operating Characteristics (continued)

(V+ = 3.0V, TA = +25°C, unless otherwise noted.)



Pin Description

PIN			NAME	FUNCTION
MAX941	MAX942	MAX944		
—	1	1	OUTA	Comparator A Output
—	2	2	INA-	Comparator A Inverting Input
—	3	3	INA+	Comparator A Noninverting Input
1	8	4	V+	Positive Supply (V+ to GND must be ≤ 6.5V)
—	5	5	INB+	Comparator B Noninverting Input
—	6	6	INB-	Comparator B Inverting Input
—	7	7	OUTB	Comparator B Output
—	—	8	OUTC	Comparator C Output
—	—	9	INC-	Comparator C Inverting Input
—	—	10	INC+	Comparator C Noninverting Input
6	4	11	GND	Ground
—	—	12	IND+	Comparator D Noninverting Input
—	—	13	IND-	Comparator D Inverting Input
—	—	14	OUTD	Comparator D Output
2	—	—	IN+	Noninverting Input
3	—	—	IN-	Inverting Input
4	—	—	$\overline{\text{SHDN}}$	Shutdown: MAX941 is active when $\overline{\text{SHDN}}$ is driven high; MAX941 is in shutdown when $\overline{\text{SHDN}}$ is driven low.
5	—	—	$\overline{\text{LATCH}}$	The output is latched when $\overline{\text{LATCH}}$ is low. The latch is transparent when $\overline{\text{LATCH}}$ is high.
7	—	—	OUT	Comparator Output
8	—	—	N.C.	No Connection. Not internally connected.

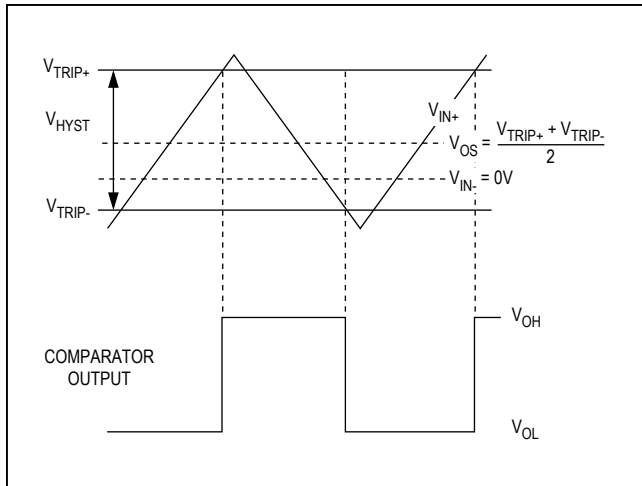


Figure 1. Input and Output Waveform, Noninverting Input Varied

## Detailed Description

The MAX941/MAX942/MAX944 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.4V of either supply rail without external pullup or pulldown circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX941/MAX942/MAX944 interface directly to CMOS and TTL logic.

## Timing

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX941/MAX942/MAX944 have internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX941/MAX942/MAX944's

fixed internal hysteresis eliminates these resistors and the equations needed to determine appropriate values.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX941 includes an internal latch that allows storage of comparison results. The LATCH pin has a high input impedance. If LATCH is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when LATCH is pulled low. All timing constraints must be met when using the latch function (Figure 2).

## Shutdown Mode (MAX941 Only)

The MAX941 shuts down when SHDN is low. When shut down, the supply current drops to less than 60µA, and the three-state output becomes high impedance. The SHDN pin has a high input impedance. Connect SHDN to V+ for normal operation. Exit shutdown with LATCH high; otherwise, the output will be indeterminate.

## Input Stage Circuitry

The MAX941/MAX942/MAX944 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two back-to-back diodes between IN+ and IN- as well as two 4.1kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than 2VF, where VF is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding 2VF), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(\text{IN}+ - \text{IN}-) - 2V_F}{2 \times 4.1\text{k}\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (IB). As long as the differential input voltage is less than 2VF, this input current is equal to IB. The protection circuitry also allows for the input common-mode range of the MAX941/MAX942/MAX944 to extend beyond both power-supply rails. The output is in the correct logic state if one or both inputs are within the common-mode range.

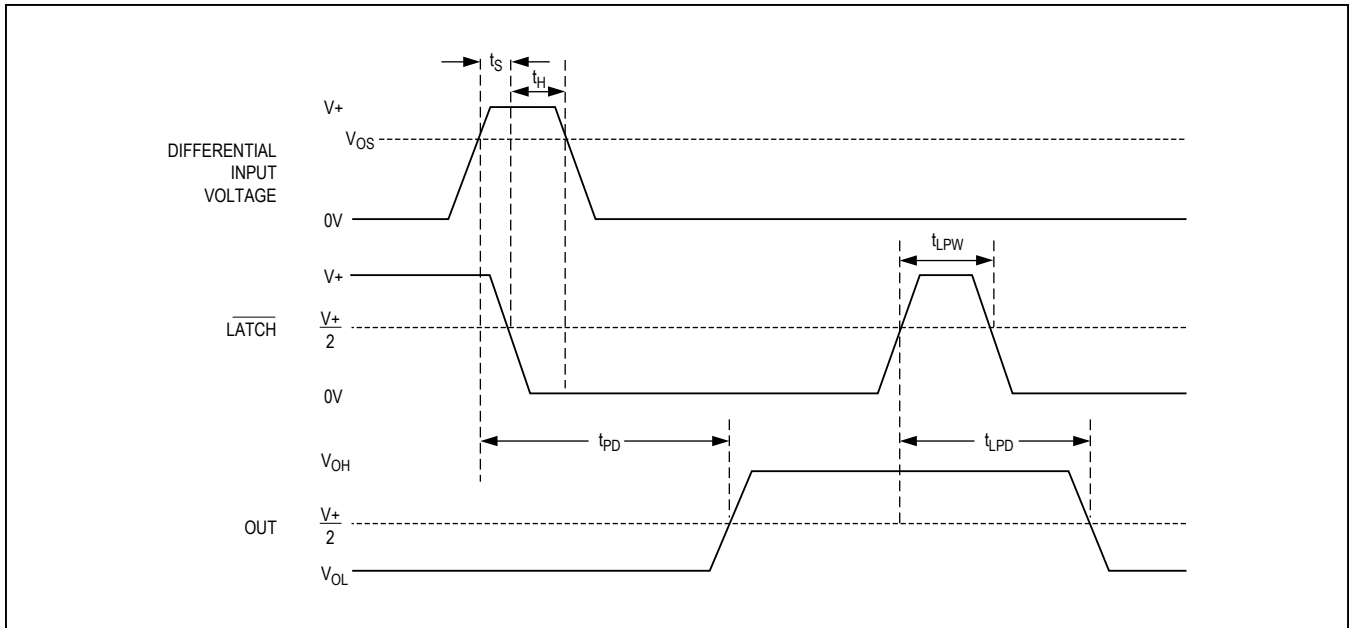


Figure 2. MAX941 Timing Diagram with Latch Operator

### Output Stage Circuitry

The MAX941/MAX942/MAX944 contain a current-driven output stage as shown in Figure 4. During an output transition,  $I_{SOURCE}$  or  $I_{SINK}$  is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches  $V_{OH}$  or  $V_{OL}$ , the source or sink current decreases to a small value, capable of maintaining the  $V_{OH}$  or  $V_{OL}$  static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noisesensitive applications where fast edges may cause interference.

### Applications Information

#### Circuit Layout and Bypassing

The high gain bandwidth of the MAX941/MAX942/MAX944 requires design precautions to realize the comparators' full high-speed capability. The recommended precautions are:

- 1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
- 2) Place a decoupling capacitor (a  $0.1\mu\text{F}$  ceramic capacitor is a good choice) as close to  $V+$  as possible.
- 3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
- 4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
- 5) Solder the device directly to the printed circuit board instead of using a socket.

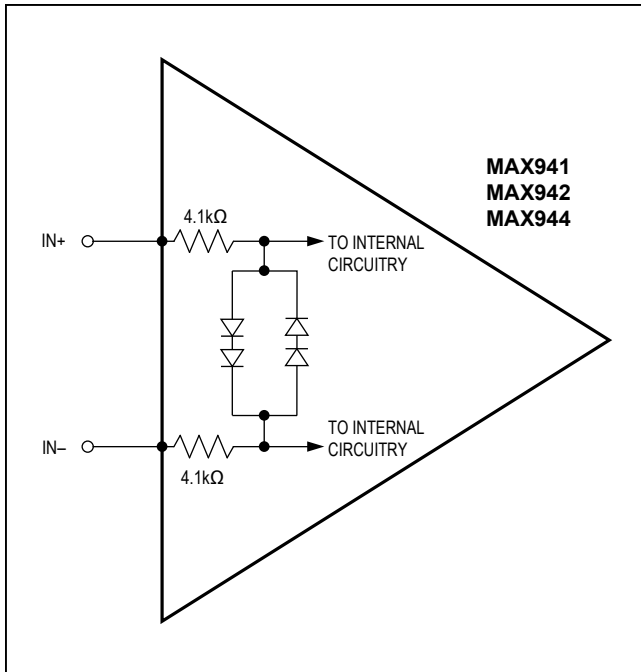


Figure 3. Input Stage Circuitry

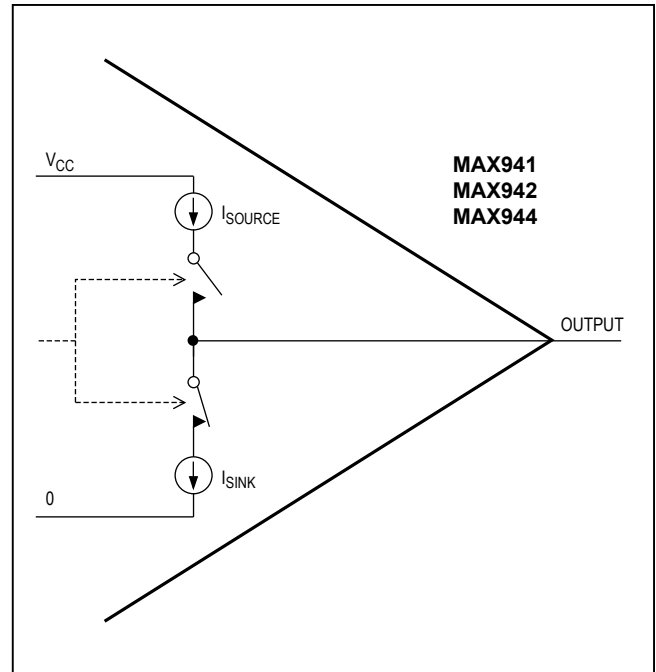


Figure 4. Output Stage Circuitry

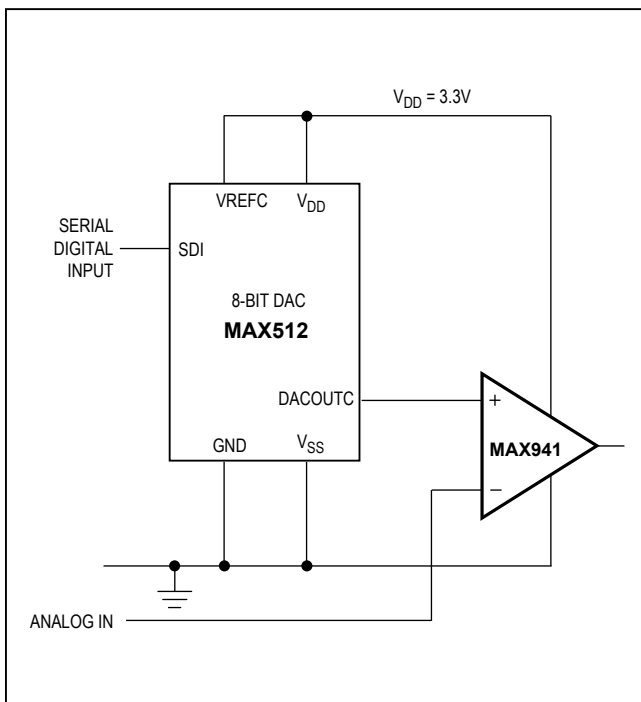


Figure 5. 3.3V Digitally Controlled Threshold Detector

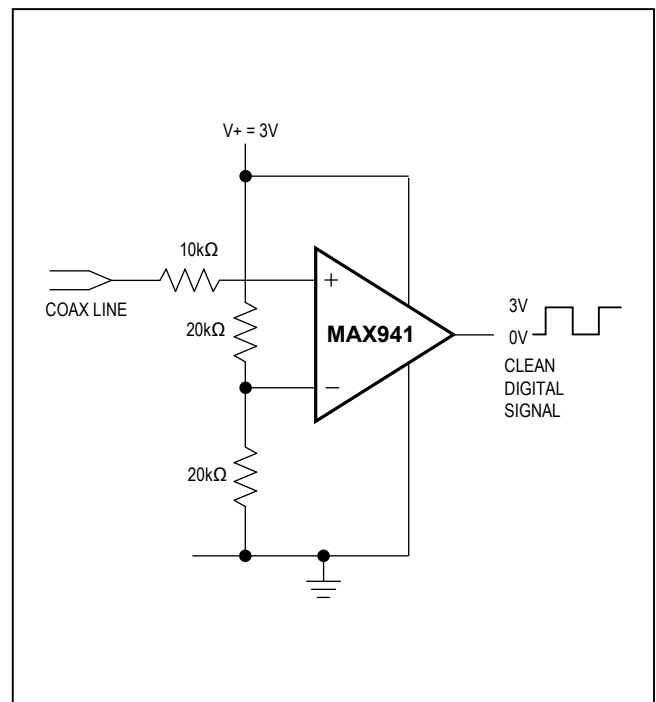


Figure 6. Line Transceiver Application



MAX941/MAX942/  
MAX944

High-Speed, Low-Power, 3V/5V, Rail-to-Rail,  
Single-Supply Comparators

### Ordering Information (continued)

PART	TEMP RANGE	PIN- PACKAGE
<b>MAX942</b> MSA/PR	-55°C to +125°C	8 SO
MAX942CPA	0°C to +70°C	8 PDIP
MAX942CSA	0°C to +70°C	8 SO
MAX942EPA	-40°C to +85°C	8 PDIP
MAX942ESA	-40°C to +85°C	8 SO
MAX942EUA-T	-40°C to +85°C	8 $\mu$ MAX
MAX942AUA-T	-40°C to +125°C	8 $\mu$ MAX
<b>MAX944</b> CPD	0°C to +70°C	14 PDIP
MAX944CSD	0°C to +70°C	14 SO
MAX944EPD	-40°C to +85°C	14 PDIP
MAX944ESD	-40°C to +85°C	14 SO

T = Tape and reel.

### Chip Information

PROCESS: BIPOLAR

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 $\mu$ MAX	U8-1	<a href="#">21-0036</a>	<a href="#">90-0092</a>
8 PDIP	P8-1	<a href="#">21-0043</a>	—
8 SO	S8-2	<a href="#">21-0041</a>	<a href="#">90-0096</a>
14 PDIP	P14-3	<a href="#">21-0043</a>	—
14 SO	S14-1	<a href="#">21-0041</a>	<a href="#">90-0112</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
8	12/08	Added SO package diagram and removed transistor count	10
9	3/09	Corrected <i>Ordering Information</i> for MAX944ESD	10
10	9/14	Corrected <i>Electrical Characteristics</i> and removed automotive reference from Features	1, 3

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