High-Voltage PWM Power-Supply Controller

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +120V
ES to GND .....-0.3V to +40V
V_{DD} to GND .....-0.3V to +19V
V_{CC} to GND .....-0.3V to +12.5V
MAXTON, COMP, CS, FB, CON to GND .....-0.3V to +8V
NDRV, SS, FREQ to GND .....-0.3V to (V_{CC} + 0.3V)
I_{NDIV}, REF to GND .....-0.3V to +4.5V
V_{CC}, V_{DD}, V+, ES Current .....±20mA
NDRV Current, Continuous .....±25mA
NDRV Current, ≤ 1µs .....±1A
CON and REF Current .....±20mA
All Other Pins .....±20mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin SO (derate 9.5mW/°C above +70°C) 762mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
Maximum Junction Temperature (T_J) .....+150°C
Operating Temperature Ranges
MAX5003C_E .....0°C to +70°C
MAX5003E_E .....-40°C to +85°C
Operating Junction Temperature (T_J) .....+125°C
16-Pin SO θ_{JA} .....105°C/W
16-Pin QSOP θ_{JA} .....120°C/W
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = V_{ES} = V_{DD} = +12V, V_{INDIV} = 2V, V_{CON} = 0, R_{FREQ} = R_{MAXTON} = 200kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY CURRENT							
Shutdown Current	I+	V_{INDIV} = 0, V+ = 110V, V_{ES} = V_{DD} = unconnected			35	75	µA
Supply Current	I_{DD}	V+ = V_{ES} , V_{DD} = 18.75				1.2	mA
PREREGULATOR/STARTUP							
V+ Input Voltage (Note 1)	V+	E_S = V_{DD} = unconnected	I_{NDRV} = 2mA	25			V
			I_{NDRV} = 5mA			110	V
E_S Input Voltage (Note 1)	V_{ESI}	V_{DD} = unconnected, V+ = V_{ES}, I_{NDRV} = 7.5mA		10.8		36	V
E_S Output Voltage	V_{ESO}	V+ = 110V, V_{DD} = unconnected				36	V
V_{DD} Output Voltage	V_{DD}	V+ = 36V, I_{DD} = 0 to 7.5mA, ES = unconnected		9	9.75	10.5	V
V_{DD} Input Voltage Range	V_{DD}	V+ = V_{ES} = 36V, I_{NDRV} = 7.5mA		10.75		18.75	V
V_{DD} Regulator Turn-Off Voltage	V_{TO}	V+ = 36V, I_{V+} < 75µA, ES = unconnected		10.75			V
CHIP SUPPLY (V_{CC})							
V_{CC} Output Voltage	V_{CC}	V+ = 36V, ES = unconnected, V_{DD} = 18.75V		7.4		12	V
V_{CC} Undervoltage Lockout Voltage	V_{CCLO}	V_{CC} falling			6.3		V
OUTPUT DRIVER							
Peak Source Current		V_{NDRV} = 0, V_{CC} supported by V_{CC} capacitor			570		mA
Peak Sink Current		V_{NDRV} = V_{CC}			1000		mA
NDRV Resistance High	R_{OH}	I_{NDRV} = 50 mA			4	12	Ω
NDRV Resistance Low	R_{OL}	I_{NDRV} = 50 mA			1		Ω
REFERENCE							
REF Output Voltage	V_{REF}	No load		2.905	3.000	3.098	V
REF Voltage Regulation	ΔV_{REF}	I_{REF} = 0 to 1mA			5	20	mV

ELECTRICAL CHARACTERISTICS (continued)

(V+ = V_{ES} = V_{DD} = +12V, V_{INDIV} = 2V, V_{CON} = 0, R_{FREQ} = R_{MAXTON} = 200kΩ, T_A = $T_{MIN\ to}$ T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT LIMIT							
CS Threshold Voltage	V_{CS}	V_{CON} = 1.25V		80	100	120	mV
CS Input Bias Current	I_{CS}	0 < V_{CS} < 0.1V		-1		+1	µA
Overcurrent Delay	t_D	From end of blanking time 25mV overdrive			240		ns
CS Blanking Time	t_B				70		ns
ERROR AMPLIFIER							
Voltage Gain	A_V	I_{COMP} = 5µA; V_{COMP} = 0.5V, 2.5V		60	80		dB
Unity-Gain Bandwidth	BW	R_{LOAD} = 200kΩ, C_{LOAD} = 100pF			1.2		MHz
Phase Margin	ϕ	A_{VOL} = 1V/V, C_{LOAD} = 100pF			65		degrees
Output Clamp Low	V_{COMPL}	At COMP			0.25		V
Output Clamp High	V_{COMPH}	At COMP			3.00		V
FEEDBACK INPUT AND SET POINT							
FB Regulation Voltage	V_{SET}	FB = COMP, V_{CON} = 1.5V		1.448	1.485	1.522	V
FB Bias Current	I_{FB}	V_{FB} = 1.5V		-1	0.1	+1	µA
FB V_{SET} Tempco	TC_{FB}				100		ppm/°C
UNDERVOLTAGE LOCKOUT							
INDIV Undervoltage Lockout	$V_{INDIVLO}$	V+ = V_{ES} = V_{DD} = 10.8V and 18.75V	V_{INDIV} falling	1.15	1.20	1.25	V
			V_{INDIV} rising	1.23	1.32	1.45	
INDIV Hysteresis	V_{HYST}				125		mV
INDIV Bias Current		V_{INDIV} = 1.28V		-1	0.01	+1	µA
MAIN OSCILLATOR—EXTERNAL MODE							
FREQ Input Low	V_{IL}	V_{CON} = 3.0V				0.8	V
FREQ Input High	V_{IH}	V_{CON} = 3.0V		2.7			V
FREQ Output Low	I_{OL}	V_{FREQ} = 5V, V_{CON} = 3.0V				1	µA
External Oscillator Maximum Low Time	t_{EXT}	(Note 2)		8	13		µs
FREQ Range	f_{FREQ}			200		1200	kHz
Frequency Range	f_S	f_S = 1/4 f_{FREQ}		50		300	kHz
FREQ HI/LO Pulse Width				150			ns
MAIN OSCILLATOR—INTERNAL MODE							
FREQ Resistor Range	R_{FREQ}			50		500	kΩ
Oscillator Frequency				80	100	120	kHz
FREQ Output Current High	I_{OH}	V_{FREQ} = 0				300	µA
FREQ Output Current Low	I_{OL}	V_{FREQ} = 1.5V				1	µA
MAXIMUM DUTY CYCLE (MAXTON)							
Maximum Programmable Duty Cycle		V_{INDIV} = 1.25V			75		%

High-Voltage PWM Power-Supply Controller

ELECTRICAL CHARACTERISTICS (continued)

(V+ = V_{ES} = V_{DD} = +12V, V_{INDIV} = 2V, V_{CON} = 0, R_{FREQ} = R_{MAXTON} = 200kΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

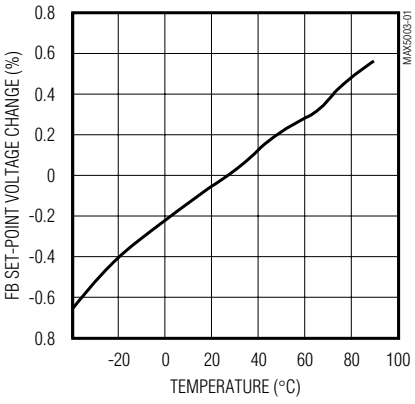
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM OSCILLATOR						
MAXTON Resistor Range	R_{MAXTON}		50		500	kΩ
Maximum On-Time Range	t_{ON}	R_{MAXTON} = 200kΩ, V_{INDIV} = 1.25V		7.5		µs
Input Voltage Feed Forward Ratio		V_{INDIV} stepped from 1.5V to 1.875V, V_{CON} = 3.0V (Note 3)	0.72	0.8	0.88	
RAMP Voltage Low		V_{INDIV} = 1.875V	0.48	0.5	0.53	V
RAMP Voltage High				2.5		V
Minimum On-Time				200		ns
SOFT-START						
SS Source Current		V_{SS} = 0.5V, V_{DD} = unconnected, V_{CON} = 1.5V	3.4	5.5	9	µA
SS Sink Current		V_{SS} = 0.4V (Note 4)		10		mA
SS Time				0.45		s/µF
PWM COMPARATOR						
CON Bias Current	I_{CON}	V_{CON} = 0.5V and 2.5V	-1	0.01	1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature				150		°C
Thermal Hysteresis				20		°C

Note 1: See the *Typical Operating Characteristics* for preregulator current-to-voltage characteristics.
Note 2: Maximum time FREQ can be held below V_{IL} and still remain in external mode.
Note 3: Feed-forward Ratio = Duty cycle at (V_{INDIV} = 1.5V)/Duty cycle at (V_{INDIV} = 1.875V)
Note 4: Occurs at start-up and until V_{REF} is valid.

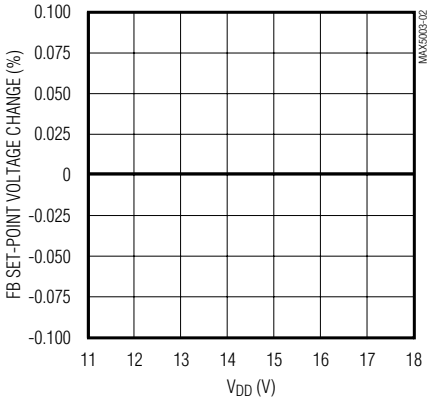
Typical Operating Characteristics

(V_{DD} = +12V, R_{FREQ} = 200kΩ, R_{MAXTON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

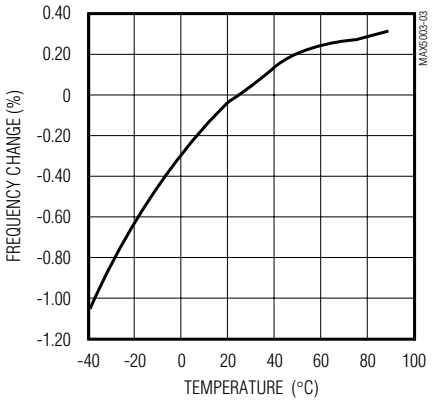
FB SET-POINT VOLTAGE CHANGE vs. TEMPERATURE



FB SET-POINT VOLTAGE CHANGE vs. SUPPLY VOLTAGE



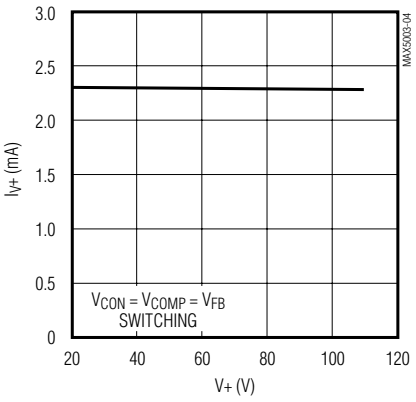
SWITCHING FREQUENCY CHANGE vs. TEMPERATURE



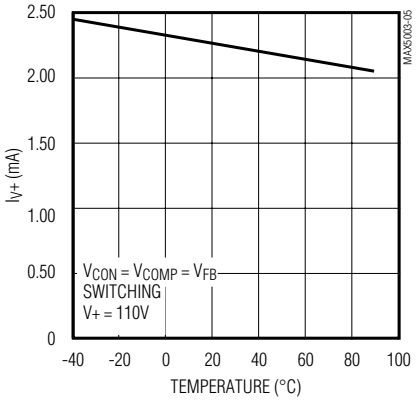
Typical Operating Characteristics (continued)

(V_{DD} = +12V, R_{FREQ} = 200kΩ, R_{MAXTON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

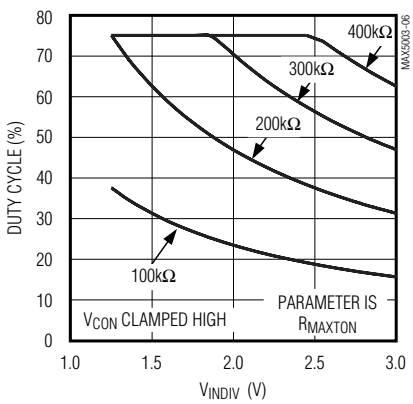
V+ INPUT CURRENT vs. VOLTAGE



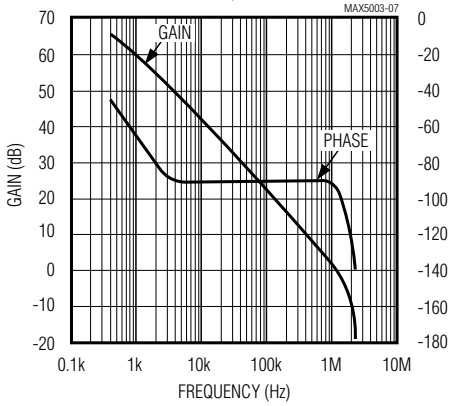
V+ INPUT CURRENT vs. TEMPERATURE



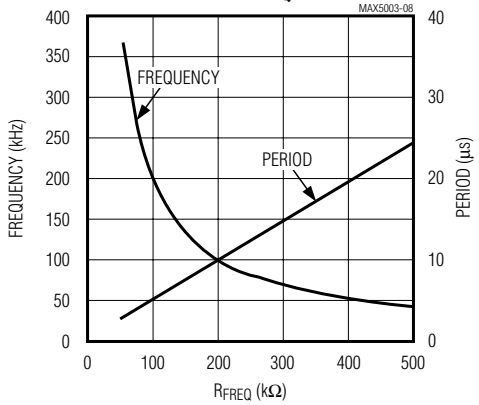
MAXIMUM DUTY CYCLE vs. V_{INDIV}



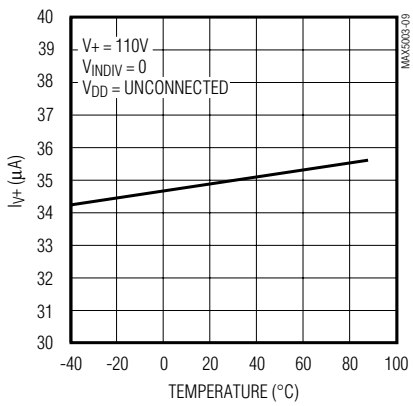
ERROR AMP FREQUENCY RESPONSE



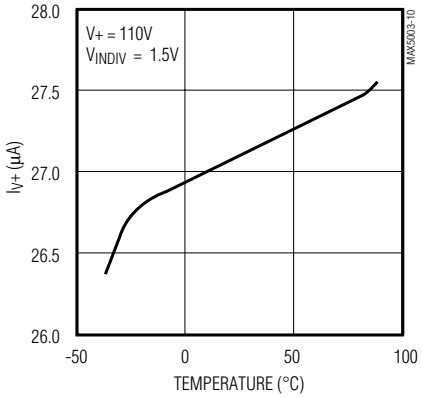
SWITCHING FREQUENCY AND PERIOD vs. R_{FREQ}



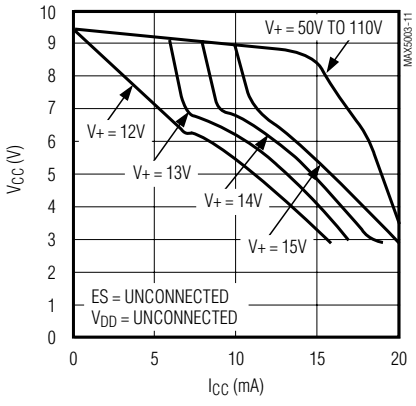
V+ SHUTDOWN CURRENT vs. TEMPERATURE



V+ CURRENT IN BOOTSTRAPPED OPERATION vs. TEMPERATURE



V_{CC} LOAD REGULATION

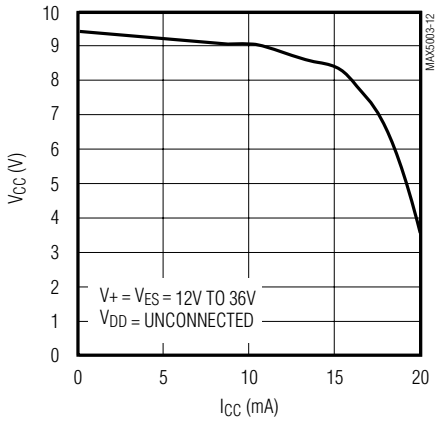


High-Voltage PWM Power-Supply Controller

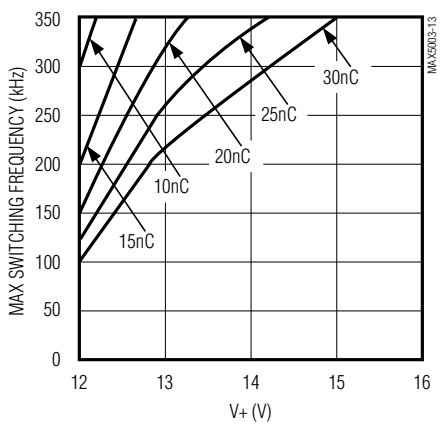
Typical Operating Characteristics (continued)

(V_{DD} = +12V, R_{FREQ} = 200kΩ, R_{MAXTON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

V_{CC} LOAD REGULATION



MAXIMUM FREQUENCY vs. INPUT VOLTAGE AND FET TOTAL GATE-SWITCHING CHARGE



Pin Description

PIN	NAME	FUNCTION
1	V+	Preregulator Input. Connect to the power line for use with 25V to 110V line voltages. Bypass V+ to ground with a 0.1µF capacitor, close to the IC. Connects internally to the drain of a depletion FET preregulator.
2	INDIV	Undervoltage Sensing and Feed-Forward Input. Connect to the center point of an external resistive divider connected between the main power line and AGND. Undervoltage lockout takes over and shuts down the controller when V_{INDIV} < 1.2V. INDIV bias is typically 0.01µA.
3	ES	Preregulator Output. When V+ ranges above 36V, bypass ES to AGND with a 0.1µF capacitor close to the IC. When V+ is always below 36V, connect ES to V+.
4	FREQ	Oscillator Frequency Adjust and Synchronization Input. In internal free-running mode, the voltage on this pin is internally regulated to 1.25V. Connect a resistor between this pin and AGND to set the PWM frequency. Drive between V_{IL} and V_{IH} at four times the desired frequency for external synchronization.
5	SS	Soft-Start Capacitor Connection. Ramp time to full current limit is approximately 0.5ms/nF. Limits duty cycle when V_{SS} < V_{CON}.
6	REF	Reference Voltage Output (3.0V). Bypass to AGND with a 0.1µF capacitor.
7	CON	Control Input of the PWM Comparator
8	COMP	Compensation Connection. Output of the error amplifier, available for compensation.
9	FB	Feedback Input. Regulates to V_{FB} = V_{REF} / 2 = 1.5V.
10	MAXTON	Maximum On-Time Programming. A resistor from MAXTON to AGND sets the PWM gain and limits the maximum duty cycle. The voltage on MAXTON tracks the voltage on the INDIV pin. Maximum on-time is proportional to the value of the programming resistor. The maximum duty cycle is limited to 75%, regardless of the programming resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
11	AGND	Analog Ground. Connect to PGND close to the IC.
12	CS	Current Sense with Blanking. Turns power switch off if V_{CS} rises above 100mV (referenced to PGND). Connect a 100Ω resistor between CS and the current-sense resistor (Figure 2). Connect CS to PGND if not used.
13	PGND	Power Ground. Connect to AGND.
14	NDRV	Gate Drive for External N-Channel Power FET
15	V_{CC}	Output Driver Power-Rail Decoupling Point. Connect a capacitor to PGND with half the value used for V_{DD} bypass very close to the pin. If synchronizing several controllers, power the fan-out buffer driving the FREQ pins from this pin.
16	V_{DD}	9.75V Internal Linear-Regulator Output. Drive V_{DD} to a voltage higher than 10.75V to bootstrap the chip supply. V_{DD} is also the supply voltage rail for the chip. Bypass to AGND with a 5µF to 10µF capacitor.

Detailed Description

The MAX5003 is a PWM controller designed for use as the control and regulation core of voltage-mode control flyback converters or forward-voltage power converters. It provides the power-supply designer with maximum flexibility and ease of use. The device is specified up to 110V and will operate from as low as 11V. Its maximum operating frequency of 300kHz permits the use of miniature magnetic components to minimize board space. The range, polarity, and range of output voltages and power are limited only by design and by the external components used.

This device works in isolated and nonisolated configurations, and in applications with single or multiple output voltages. All the building blocks of a PWM voltage-mode controller are present in the MAX5003 and its settings are adjustable. The functional diagram is shown on Figure 1.

Modern Voltage-Mode Controllers

The MAX5003 offers a voltage-mode control topology and adds features such as fast input voltage feed forward, programmable maximum duty cycle, and high operating frequencies. It has all the advantages of current-mode control—good control loop bandwidth, same-cycle response to input voltage changes, and pulse-by-pulse current limiting. It eliminates disadvantages such as the need for ramp compensation, noise sensitivity, and the analytical and design difficulties of dealing with two nested feedback loops. In summary, voltage-mode control has inherent superior noise immunity and uses simpler compensation schemes.

Internal Power Regulators

The MAX5003's power stages operate over a wide range of supply voltages while maintaining low power consumption. For the high end of the range (+36V to +110V), power is fed to the V+ pin into a depletion junction FET preregulator. This input must be decoupled with a 0.1µF capacitor to the power ground pin (PGND). To decouple the power line, other large-value capacitors must be placed next to the power transformer connection.

The preregulator drops the input voltage to a level low enough to feed a first low-dropout regulator (LDO) (Figure 1). The input to the LDO is brought out at the ES pin. ES must also be decoupled with a 0.1µF capacitor.

In applications where the maximum input voltage is below 36V, connect ES and V+ together and decouple with a 0.1µF capacitor.

The first LDO generates the power for the V_{DD} line. The V_{DD} line is available at the V_{DD} pin for decoupling. The bypass to AGND must be a 5µF to 10µF capacitor.

When the maximum input voltage is always below 18.75V, power may also be supplied at V_{DD}; in this case, connect V+, ES, and V_{DD} together.

Forcing voltages at V_{DD} above 10.75V (see *Electrical Characteristics*) disables the first LDO, typically reducing current consumption below 50µA (see *Typical Operating Characteristics*).

Following the V_{DD} LDO is another regulator that drives V_{CC}: the power bus for the internal logic, analog circuitry, and external power MOSFET driver. This regulator is needed because the V_{DD} voltage level would be too high for the external N-channel MOSFET gate. The

High-Voltage PWM Power-Supply Controller

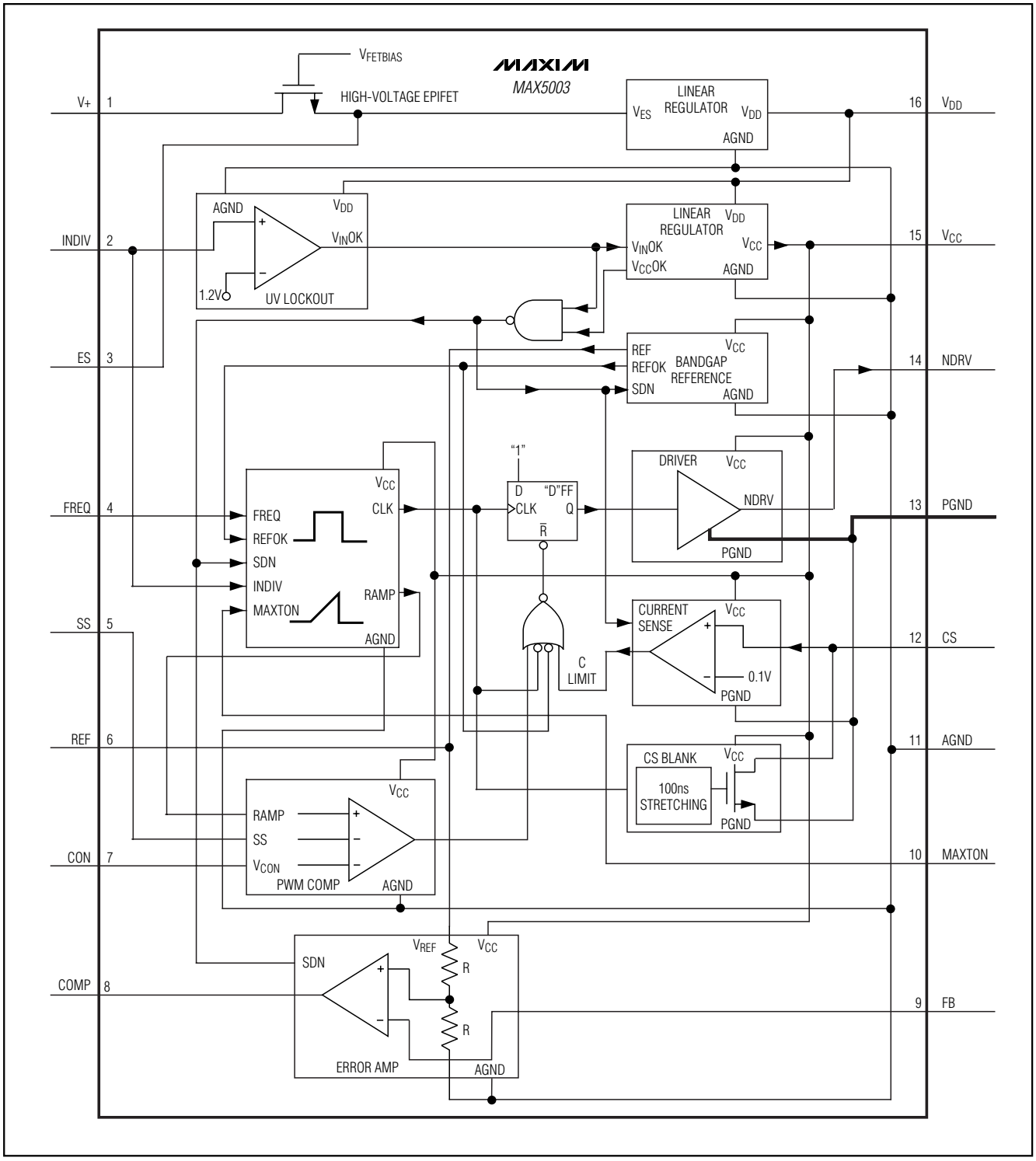


Figure 1. Functional Diagram

V_{CC} regulator has a lockout line that shorts the N-channel MOSFET driver output to ground if the V_{CC} LDO is not regulating. V_{CC} feeds all circuits except the V_{CC} lockout logic, the undervoltage lockout, and the power regulators.

The preferred method for powering the MAX5003 is to start with the high-voltage power source (at V+ or ES, depending on the application), then use a bootstrap source from the same converter with an output voltage higher than the V_{DD} regulator turn-off voltage (10.75V) to power V_{DD}. This will disable the power consumption of the V_{DD} LDO. It is also possible to power the MAX5003 with no bootstrap source from ES or V+, but do not exceed the maximum allowable power dissipation. The current consumption of the part is mostly a function of the operating frequency and the type of external power switch used—in particular, the total charge to be supplied to the gate.

A reference output of 3V nominal is externally available at the REF pin, with a current sourcing capability of 1mA. A lockout circuit shuts off the oscillator and the output driver if REF falls 200mV below its set value.

Minimize loading at REF, since the REF voltage is the source for the FB voltage, which is the regulator set point when the error amplifier is used. Any changes in V_{REF} will be proportionally reflected in the regulated output voltage of the converter.

Undervoltage Lockout, Feed Forward, and Shutdown

The undervoltage lockout feature disables the controller when the voltage at INDIV is below 1.2V (120mV hysteresis). When INDIV rises higher than 1.2V plus the hysteresis (typically 1.32V), it allows the controller to start. An external resistive divider connected between the power line and AGND generates the INDIV signal. INDIV is also used as the signal for the fast input voltage feed-forward circuit.

Always connect INDIV to a voltage divider. It is not a "don't care" condition; the signal is used to set the fast feed-forward circuit (see the *Oscillator and Ramp Generator* section).

Choose R2 (Figure 2) between 25kΩ to 500kΩ and calculate R1 to satisfy the following equation:

$$R1 = R2\left(\frac{V_{SUL}}{V_{INDIVLO}} - 1\right)$$

where V_{SUL} = system undervoltage lockout and $V_{INDIVLO}$ = I_{NDIV} undervoltage lockout.

The undervoltage lockout function allows the use of the INDIV pin as a shutdown pin with an external switch to ground. The shutdown circuit must not affect the resistive divider during normal operation.

Current-Sense Comparator

The current-sense (CS) comparator and its associated logic limit the current through the power switch. Current is sensed at CS as a voltage across a sense resistor between the external MOSFET source and PGND. Connect CS to the external MOSFET source through a 100Ω resistor or RC lowpass filter (Figures 2 and 3). See *CS Resistor* in the *Component Selection* section.

A blanking circuit shunts CS to ground when the power MOSFET switch is turned off, and keeps it there for 70ns after turn-on. This avoids false trips caused by the switching transients. The blanking circuit also resets the RC filter, if used. When V_{CS} > 100mV, the power MOSFET is switched off. The propagation delay from the time the switch current reaches the trip level to the driver turn-off time is 240ns. If the current limit is not used, the CS pin must be connected to PGND.

Error Amplifier

The internal error amplifier is one of the building blocks that gives the MAX5003 its flexibility. Its noninverting input is biased at 1.5V, derived from the internal 3V reference. The inverting input is brought outside (FB pin) and is the regulation feedback connection point. If the error amplifier is not used, connect this pin to ground. The output is available for the frequency compensation network and for connection to the input of the PWM comparator (CON). Unity-gain frequency is 1.2MHz, open-circuit gain is 80dB, and the amplifier is unity-gain stable. To eliminate long overload recovery times, there are clamps limiting the output excursions close to the range limits of the PWM ramp. The voltage at the noninverting input of the error amplifier is the regulator set point, but is not accessible.

Set-point voltage can be measured, if needed, by connecting COMP and FB and measuring that node with respect to ground. The error amplifier is powered from the V_{CC} rail.

PWM Comparator

The pulse-width modulator (PWM) comparator stage transforms the error signal into a duty cycle by comparing the error signal with a linear ramp. The ramp levels are 0.5V min and 2.5V max. The comparator has a typical hysteresis of 5.6mV and a propagation delay of 100ns. The output of the comparator controls the external FET.

Soft-Start

The soft-start feature allows converters built using the MAX5003 to apply power to the load in a controllable soft ramp, thus reducing start-up surges and stresses.

High-Voltage PWM Power-Supply Controller

It also determines power-up sequencing when several converters are used.

Upon power turn-on, the SS pin acts as a current sink to reset any capacitance attached to it. Once REF has exceeded its lockout value, SS sources a current to the external capacitor, allowing the converter output voltage to ramp up. Full output voltage is reached in approximately 0.45s/µF.

The SS pin is an overriding extra input to the PWM comparator. As long as its voltage is lower than V_{CON}, it overrides V_{CON} and SS determines the level at which the duty cycle is decided by the PWM comparator. After exceeding V_{CON}, SS no longer controls the duty cycle. Its voltage will keep rising up to V_{CC}.

Oscillator and Ramp Generator

The MAX5003 oscillator generates the ramp used by the comparator, which in turn generates the PWM digital signal. It also controls the maximum on-time feature of the controller. The oscillator can operate in two modes: free running and synchronized (sync). A single pin, FREQ, doubles as the attachment point for the frequency programming resistor and as the synchronization input. The mode recognition is automatic, based on the voltage level at the FREQ pin.

In free-running mode, a 1.25V source is internally applied to the pin; the oscillator frequency is proportional to the current out of the pin through the programming resistor, with a proportionality constant of 16kHz/µA.

In sync mode, the signal from the external master generator must be a digital rectangular waveform running at four times the desired converter switching frequency. Minimum acceptable signal pulse width is 150ns, positive or negative, and the maximum frequency is 1.2MHz.

When the voltage at FREQ is forced above 2.7V, the oscillator goes into sync mode. If left at or below 1.5V for more than 8µs to 20µs, it enters free-running mode.

The master clock generator cannot be allowed to stop at logic zero. If the system design forces such a situation, an inverter must be used at the FREQ pin.

In sync mode, the oscillator signal is divided by four and decoded. The output driver is blocked during the last phase of the division cycle, giving a hardwired maximum on-time of 75%. In free-running mode, the oscillator duty cycle is 75% on, and the off portion also blocks the output driver. The maximum on-time is then absolutely limited to 75% in either mode. Maximum on-time can be controlled to values lower than 75% by a programming resistor at the MAXTON pin.

The PWM ramp generated goes from 0.5V min to 2.5V max, and the maximum time on is the time it takes from low to high.

MAXTON is internally driven to V_{INDIV} and a resistor must be connected from MAXTON to AGND, to program the maximum on-time.

The ramp slope is directly proportional to V_{INDIV} and inversely proportional to R_{MAXTON}. Since the ramp voltage limits are fixed, controlling the ramp slope sets the maximum time on.

Changing the ramp slope while V_{CON} remains constant also changes the duty cycle and the energy transferred to the load per cycle of the converter. The INDIV signal is a fraction of the input voltage, so the fast input voltage feedforward works by modifying the duty cycle in the same clock period, in response to an input voltage change.

Calculate the maximum duty cycle as:

$$D_{MAX} = \frac{MAXTON}{T} \times 100$$

where:

D_{MAX} = Maximum duty cycle (%)

MAXTON = Maximum on-time

T = Switching period

Then:

$$D_{MAX} = 0.75 \times 100 \left(\frac{R_{MAXTON}}{200k\Omega} \right) \left(\frac{1.25V}{V_{INDIV}} \right) \left(\frac{f_{SW}}{100kHz} \right)$$

where:

R_{MAXTON} = Resistor from the MAXTON pin to ground

V_{INDIV} = Voltage at the INDIV pin

f_{SW} = Output switching frequency

MAXTON can then be calculated as:

$$MAXTON = \frac{0.75 \times R_{MAXTON} \times 1.25V}{200k\Omega \times V_{INDIV} \times 100kHz}$$

N-Channel MOSFET Output Switch Driver

The MAX5003 output drives an N-channel MOSFET transistor. The output sources and sinks relatively large currents, supplying the gate with the charge the transistor needs to switch. These are current spikes only, since after the switching transient is completed the load is a high-value resistance. The current is supplied from the V_{CC} rail and must be sourced by a large-value

capacitor (5µF to 10µF) at the V_{CC} pin, since the rail will not support such a load. It is this current, equivalent to the product of the total gate switching charge (from the N-channel MOSFET data sheet), times the operating frequency, that determines the bulk of the MAX5003 power dissipation.

The driver can source up to 560mA and sink up to 1A transient current with a typical on source resistance of 4Ω. The no-load output levels are V_{CC} and PGND.

Applications Information

Compensation and Loop Design Considerations

The circuit shown in Figure 2 is essentially an energy pump. It stores energy in the magnetic core and the air gap of the transformer while the power switch is on, and delivers it to the load during the off phase. It can operate in two modes: continuous and discontinuous. In discontinuous mode, all the energy is given to the load before the next cycle begins; in continuous mode, some energy is continuously stored in the core.

The system has four operating parameters: input voltage, output voltage, load current, and duty cycle. The PWM controller senses the output voltage and the input voltage, and keeps the output voltage regulated by controlling the duty cycle.

The output filter in this circuit consists of the load resistance and the capacitance on the output.

To study the stability of the feedback system and design the compensation necessary for system stability under all operating conditions, first determine the transfer function. In discontinuous mode, since there is no energy stored in the inductor at the end of the cycle, the inductor and capacitor do not show the characteristic double pole, and there is only a dominant pole defined by the filter capacitor and the load resistance. There is a zero at a higher frequency, defined by the ESR of the output filter capacitor. Such a response is easy to stabilize for a wide range of operating conditions while retaining a reasonably fast loop response.

In continuous mode, the situation is different. The inductor-capacitor combination creates a double pole, since energy is stored in the inductor at all times. In addition to the double pole, a right-half-plane zero appears in the frequency response curves. This response is not easy to compensate. It can result in conditional stability, a complicated compensation network, or very slow transient response.

To avoid the analytical and design problems of the continuous-conduction mode flyback topology and maintain good loop response, choose a design incorporating a discontinuous-conduction mode power stage

To keep the converter in discontinuous mode at all times, the value of the power transformer's primary inductance must be calculated at minimum line voltage and maximum load, and the maximum duty cycle must be limited. The MAX5003 has a programmable duty-cycle limit function intended for this purpose.

Design Methodology

Following is a general procedure for developing a system:

1) Determine the requirements.
2) In free-running mode, choose the FREQ pin programming resistor. In synchronized mode, determine the clock frequency (f_{CLK}).
3) Determine the transformer turns ratio, and check the maximum duty cycle.
4) Determine the transformer primary inductance.
5) Complete the transformer specifications by listing the primary maximum current, the secondary maximum current, and the minimum duty cycle at full power.
6) Choose the MAXTON pin programming resistor.
7) Choose a filter capacitor.
8) Determine the compensation network.

Design Example

1) $36V < V_{IN} < 72V$, $V_{OUT} = 5V$, $I_{OUT} = 1A$, ripple < 50mV, settling time ≈ 0.5ms.
2) Generally, the higher the frequency, the smaller the transformer. A higher frequency also gives higher system bandwidth and faster settling time. The trade-off is lower efficiency. In this example, 300kHz switching frequency is the choice to favor for a small transformer. If the converter will be free running (not externally synchronized), use the following formula to calculate the R_{FREQ} programming resistor:

$$R_{FREQ} = \left(\frac{100kHz}{f_{SW}}\right) 200k = 66.7k\Omega$$

where:

R_{FREQ} = Resistor between FREQ and ground

f_{SW} = Switching frequency (300kHz)

If the converter is synchronized to an external clock, the input frequency will be 1.2MHz. The external clock runs at four times the desired switching frequency.

High-Voltage PWM Power-Supply Controller

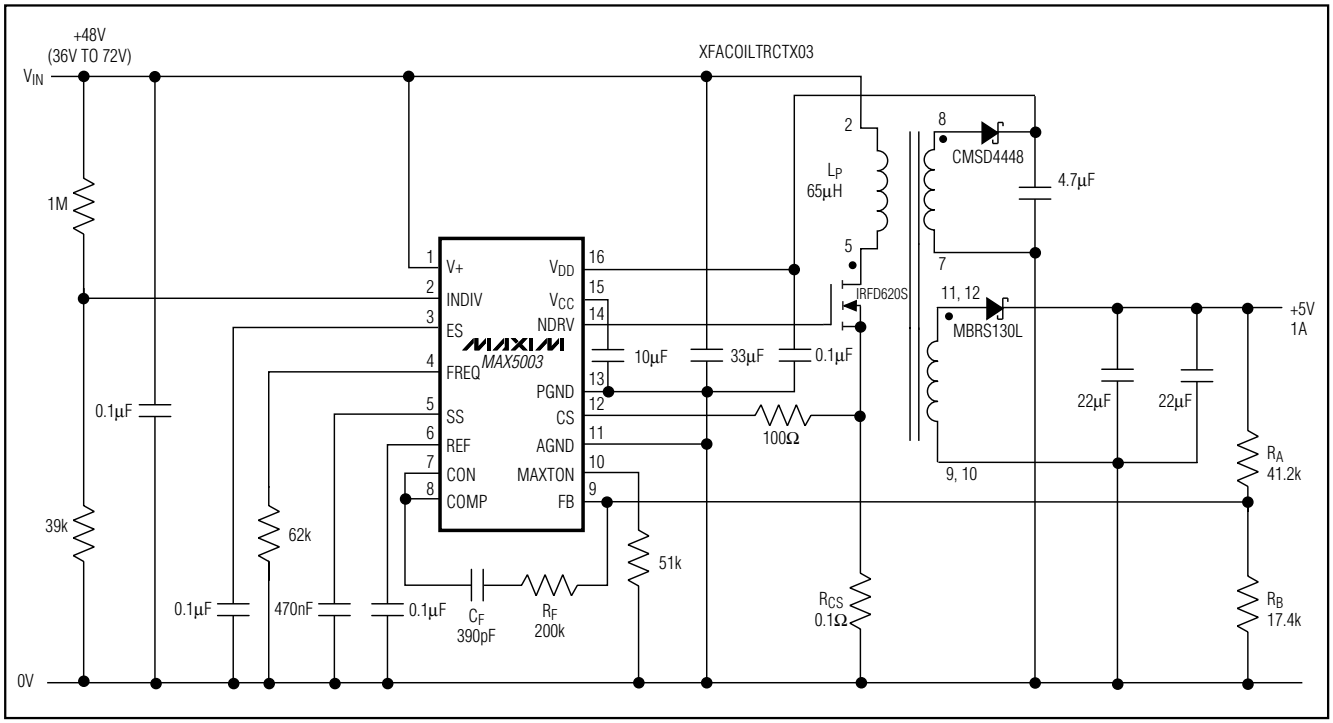


Figure 2. Application Example 1: Nonisolated +48V to +5V Converter

3) The main factors influencing the choice of the turns ratio are the switch breakdown voltage and the duty cycle. With a smaller turns ratio, the secondary reflected voltage and the maximum voltage seen by the switch during flyback are reduced, which is favorable. On the other hand, a smaller turns ratio will shorten the duty cycle and increase the primary RMS current, which can impact efficiency. A good starting figure is the ratio of the input voltage to the output voltage, rounding to the nearest integer. To keep the flyback voltage under control, choose an 8-to-1 ratio for the 48V to 5V system. The maximum duty cycle allowed without putting the device in continuous-conduction mode can be found using the following formula:

$$DC_{MAX} = \frac{1}{\left(\frac{V_{MIN}}{V_{SEC} \times N}\right) + 1}$$

where:

$N = N_P/N_S$ = Turns ratio

V_{SEC} = Secondary voltage

DC_{MAX} = Maximum duty cycle

V_{MIN} = Minimum power-line voltage

For a 48V to 5V system with an 8-to-1 turns ratio, the maximum duty cycle before putting the device in discontinuous mode is 55%. Assume that V_{IN} min is 36V (minimum input voltage, neglecting drops in the power switch and in the resistance of the primary coil) and V_{SEC} is 5.4V (5V plus a Schottky diode drop). The MAX5003 maximum duty cycle is internally limited to 75%. Generally this parameter must fall between 45% to 65% to obtain a balance between efficiency and flyback voltage while staying out of continuous conduction. If the value exceeds these bounds, adjust the turns ratio.

4) Assuming 80% efficiency, a 6.25W input is needed to produce a 5W output. Set an operating duty cycle around 12% below the maximum duty cycle to allow for component variation: 55% - 12% = 43%. Use the following formula to calculate the primary inductance:

$$L_{PRI} = \frac{\left(DC \times V_{MIN}\right)^2}{2 \times PWR_{IN} \times f_{SW}} = \frac{\left(0.43 \times 36V\right)^2}{2 \times 6.25W \times 300kHz} \cong 65\mu H$$

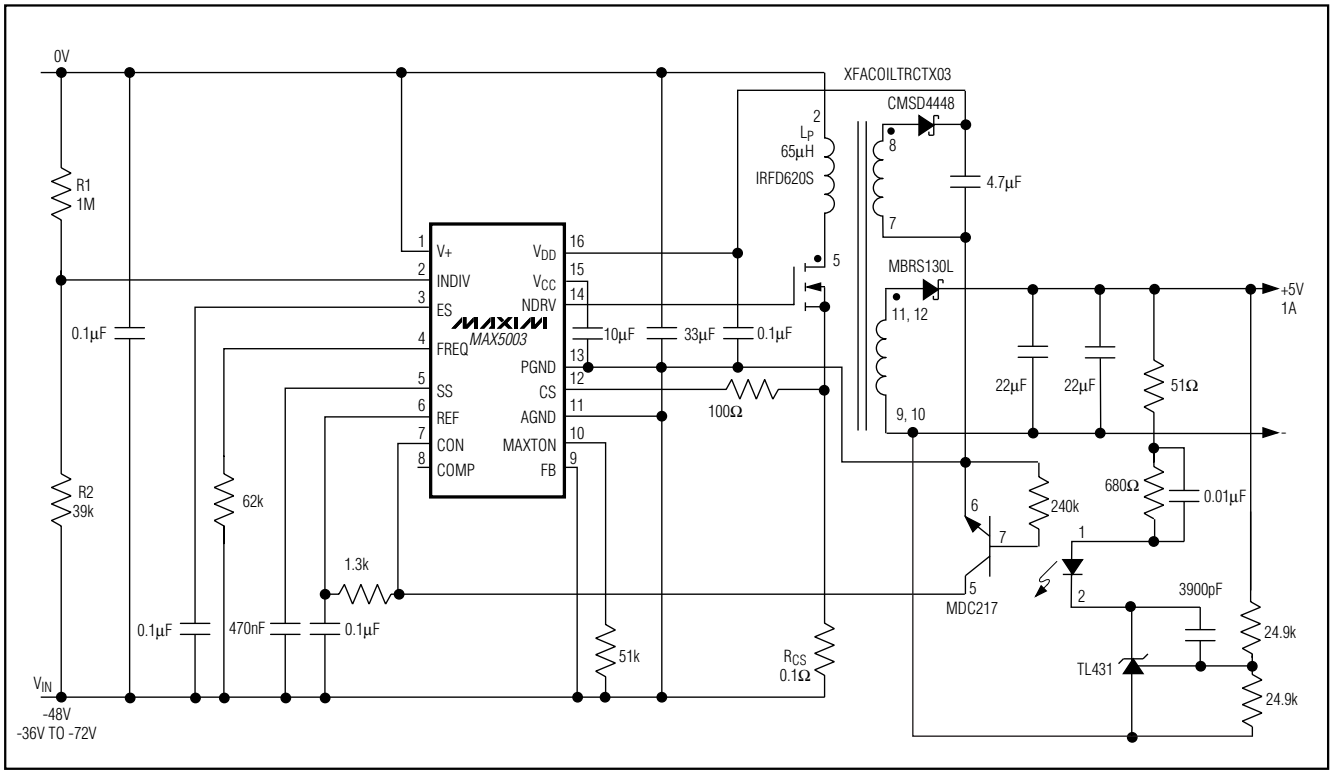


Figure 3. Application Example 2: Isolated -48V to +5V Converter

where:

DC = Duty cycle. Set to calculated minimum duty cycle at V_{MIN}.

PWR_{IN} = Input power, at maximum output power

This gives an inductance value (L_{PRI}) of approximately 65µH.

5) The other parameter that defines the transformer is peak current. This is given by:

$$I_{PRI} = \sqrt{\frac{2 \times PWR_{IN}}{L_{PRI} \times f_{SW}}} = \sqrt{\frac{2 \times 6.25W}{65\mu H \times 300kHz}} = 0.8A$$

The peak secondary current is the peak primary current multiplied by the turns ratio, or 0.8A • 8 = 6.4A. Calculating the minimum duty cycle:

$$DC_{(MIN)} = DC_{(MAX)} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}} = 43\% \times \frac{36V}{72V} =$$

With these numbers, the transformer manufacturer can choose a core.

6) For this application, the MAX5003 must be programmed for a maximum duty cycle of 55% at 36V. The MAX5003 will automatically scale the limit with the reciprocal of the input voltage as it changes. The duty-cycle limit for an input voltage of 72V will be 27% (half of 55%). The duty cycle needed to stay out of continuous conduction at 72V is 37%, so there is a 10% margin. The maximum duty time scales with the voltage at the undervoltage lockout pin, V_{INDIV}. The voltage at INDIV is set by selecting the power line undervoltage lockout trip point. The trip point for this system, running from 36V to 72V, is 32V. Then INDIV must be connected to the center point of a divider with a ratio of 32/1.25, connected between the power line and ground. Then R_{MAXTON} is:

$$R_{MAXTON} = \left(\frac{V_{MIN}}{V_{UVL}}\right)\left(\frac{100kHz}{f_{SW}}\right)\left(\frac{DC_{MAX}(V_{MIN})}{75\%}\right) 200k\Omega$$

$$= \left(\frac{36V}{32V}\right)\left(\frac{100kHz}{300kHz}\right)\left(\frac{55\%}{75\%}\right) 200k\Omega = 55k\Omega$$

High-Voltage PWM Power-Supply Controller

where:

R_{MAXTON} = Resistor between the MAXTON pin and ground

V_{MIN} = Minimum power-line voltage

V_{UVL} = Power-line trip voltage

$DC_{MAX}(V_{MIN})$ = Maximum duty cycle at minimum power-line voltage

For this application circuit, a 10% margin is reasonable, so the value used is 50kΩ. This gives a maximum duty cycle of 50%. The maximum duty cycle can now be expressed as:

$$DC(V_{CON,VIN}) = \left(\frac{V_{CON} - 0.5V}{2.0V}\right)\left(\frac{V_{MIN}}{V_{IN}}\right)\left(\frac{f_{SW}}{f_{NOM}}\right) \times DC_{MAX(VMIN)}$$

$$\approx \left(\frac{V_{CON} - 0.5V}{2.0V}\right)\left(\frac{36V}{V_{IN}}\right)\left(\frac{f_{SW}}{f_{NOM}}\right) 50\%$$

where:

V_{CON} = Voltage at the CON pin, input of the PWM comparator

$DC(V_{CON}, V_{IN})$ = Duty cycle, function of V_{CON} and V_{IN}

0.5V and 2.5V are the values at the beginning and end of the PWM ramp.

The term f_{SW} / f_{NOM} varies from 0.8 to 1.2 to allow for clock frequency variation. If the clock is running at 300kHz and the input voltage is fixed, then the duty cycle is a scaled portion of the maximum duty cycle, determined by V_{CON}.

$$DC(V_{CON}, V_{MIN}) = \left(\frac{V_{CON} - 0.5V}{2.0V}\right) 50\%$$

$$DC(V_{CON}, V_{MAX}) = \left(\frac{V_{CON} - 0.5V}{2.0V}\right) 25\%$$

$DC(2.5V, V_{MIN}) = 50\%$

$DC(2.5V, V_{MAX}) = 25\%$

$DC(0.5V, V_{MIN}) = 0$

$DC(0.5V, V_{MAX}) = 0$

7) Low-ESR/ESL ceramic capacitors were used in this application. The output filter is made by two 22µF ceramic capacitors in parallel. Normally, the ESR of a capacitor is a dominant factor determining the ripple, but in this case it is the capacitor value.

Calculating

$$\frac{I_{OUT}}{f_{SW} \times C} = \frac{1A}{300kHz \times 44\mu F} = 76mV$$

the ripple will be a fraction of this depending on the duty cycle. For a 50% duty cycle, the ripple due to the capacitance is approximately 45mV.

8) The PWM gain can be calculated from:

$$A_{PWM} = \frac{dV_{OUT}}{dV_{CON}} = \sqrt{\frac{R_L}{2 \times L_{PRI} \times f_{SW}}}\left(\frac{V_{MIN}}{2.0V}\right) DC_{MAX(VMI}$$

$$= \sqrt{\frac{R_L}{2 \times L_{PRI} \times f_{SW}}}\left(\frac{36V}{2.0V}\right) 50\% \cong 3$$

Note that while the above formula incorporates the product of the maximum duty cycle and V_{IN}, it is independent of V_{IN}. For 1A output (R_L = 5Ω), the PWM gain is +3.0V/V. For a 10% load (R_L = 50Ω), the gain is multiplied by the square root of 10 and becomes +10V/V. The pole of the system due to the output filter is 1 / 2πRC, where R is the load resistance and C the filter capacitor. Choosing a capacitor and calculating the pole frequency by:

$$f_P = \left(\frac{1}{2\pi \times R_L \times C_L}\right) = \left(\frac{1}{2\pi \times 5\Omega \times 44\mu F}\right)$$

it is 723Hz at full load. At 10% load it will be 72Hz, since the load resistor is then 50Ω instead of 5Ω. The total loop gain is equal to the PWM gain times the gain in the combination of the voltage divider and the error amplifier. The worst case for phase margin is at full load. For a phase margin of 60 degrees, this midband gain (G) must be set to be less than:

$$G < \sqrt{\frac{f_{UErrorAmp}}{\tan(PM) \times A_{PWM} \times f_P}} = \sqrt{\frac{1\,MHz}{1.7 \times 3 \times 723Hz}}$$

where:

f_U = Unity-gain frequency of error amplifier

PM = Phase margin angle

The DC accuracy of the regulator is a function of the DC gain. For 1% accuracy, a DC gain of 20 is required. Since the maximum midband gain for a stable response is 16, an integrator with a flat midband gain given by a zero is used. The midband gain is less than 16, to preserve stability, and the DC gain is much larger than 20, to achieve high DC accuracy.

Optimization on the bench showed that a midband gain of 5 gave fast transient response and settling with no ringing. The zero was pushed as high in frequency as possible without losing stability. The zero must be a factor of two or so below the system unity-gain frequency (crossover frequency) at minimum load. With the

zero at 2kHz, the crossover frequency is 4kHz and the phase margin is 50°.

Given the above considerations, R_A, R_B , R_F, and C_F can be chosen (Figure 2). The sum of R_A and R_B is chosen for low current drain. In the example, R_A plus R_B is 58kΩ and draws 80µA. The following ratio sets the output voltage:

$$R_B / (R_A + R_B) = V_{SET} / V_{OUT}$$

Since V_{SET} = 1.5V and V_{OUT} = 5V, R_A is set to 41.2kΩ and R_B to 17.4kΩ.

The midband gain is the ratio of R_F/R_A. R_B does not affect the gain because it is connected to a virtual ground. For a midband gain of 5, the feedback resistor equals 200kΩ. To set the zero at 2kHz, the capacitor value is:

$$C_F = 1 / (2\pi \times R_F \times f_Z) = 400pF$$

Layout Recommendations

All connections carrying pulsed currents must be very short, be as wide as possible, and have a ground plane behind them whenever possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency switching power converters. In the development or prototyping process, multipurpose boards, wire wrap, and similar constructive practices are not suitable for these type of circuits; attempts to use them will fail. Instead, use milled PC boards with a ground plane, or equivalent techniques

Current loops must be analyzed in any layout proposed, and the internal area kept to a minimum to reduce radiated EMI. The use of automatic routers is discouraged for PC board layout generation in the board area where the high-frequency switching converters are located. Designers should carefully review the layout. In particular, pay attention to the ground connections. Ground planes must be kept as intact as possible. The ground for the power-line filter capacitor and the ground return of the power switch or current-sensing resistor must be close. All ground connections must resemble a star system as much as practical.

“Short” and “close” are dimensions on the order of 0.25in to 0.5in (0.5cm to about 1cm).

Setting the Output Voltage

The output voltage of the converter, if using the internal error amplifier, can easily be set by the value of the FB pin set voltage. This value is 1.5V. A resistive divider must be calculated from the output line to ground, with a dividing ratio such that when the output is at the desired value, the center-point voltage will be 1.5V. The Thevenin equivalent of the resistors must be low enough so the error amplifier bias current will not introduce a division error. The two resistors must have similar temperature coefficients (tempcos), so the dividing ratio will be constant with temperature.

Component Selection

CS Resistor

The CS resistor is connected in series with the source of the N-channel MOSFET and ground, sensing the switch current. Its value can be calculated from the following equation:

$$R_{CS} = \frac{100mV}{I_{LIM(PRI)}} = \frac{100mV}{\sqrt{\frac{2\ PWR_{OUT(MAX)}}{L_{PRI} \times f_{SW} \times \eta}}} \times K_{TOL}$$

where η = efficiency and $0.5 < KT_{OL} < 0.75$.

K_{TOL} includes the tolerance of the sensing resistor, the dispersion of the MAX5003 CS trip point, and the uncertainties in the calculation of the primary maximum current.

The sensing resistor must be of the adequate power dissipation and low tempco. It must also be noninductive and physically short. Use standard surface-mount CS resistors. A 100Ω resistor is recommended between the CS resistor and the CS pin. If the current surge at the beginning of the conduction period is large and disrupts the MAX5003’s operation, add a capacitor between the CS pin and PGND, to form an RC filter.

Power Switch

The MAX5003 will typically drive an N-channel MOSFET power switch. The maximum drain voltage, maximum $R_{DS(ON)}$, and total gate switching charge are the parameters involved in choosing the FET. The maximum gate switching charge is the most important factor defining the MAX5003 internal power consumption, since the product of the switching frequency and the total gate charge is the IC current consumption. $R_{DS(ON)}$ is the parameter that determines the total conduction power losses in the switch, and the choice depends on the expected efficiency and the cooling and mounting method. The maximum drain voltage requirements can be different depending on the topology used. In the flyback configuration, the maximum voltage is the maximum supply voltage plus the reflected secondary voltage, any ringing at the end of the conduction period, and the spike caused by the leakage inductance. In the case of the forward converter, the reset time of the core will set the maximum voltage

High-Voltage PWM Power-Supply Controller

stress on the switch. A FET with the lowest total charge and the lowest $R_{DS(ON)}$ for the maximum drain voltage expected (plus some safety factor) is the best choice. The choice of package is a function of the application, the total power, and the cooling methods available.

Transformer

Transformer parameters, once calculated in the design process, can be used to find standard parts whenever possible. The most important factors are the saturation current, primary inductance, leakage inductance turns ratio, and losses. Packaging and EMI generation and susceptibility are closely connected, and must be considered. In general, parts with exposed air gaps (not contained inside the magnetic structure) will generate the most radiated EMI, and might need external shielding. If the design is in high-voltage power supplies, the insulation specifications are also important. Pay close attention if the circuitry is galvanically connected to the mains at any point, since serious safety and regulatory issues might exist.

Capacitors

As in any high-frequency power circuit, the capacitors used for filtering must meet very low ESR and ESL requirements. At the 300kHz frequency (of which the MAX5003 is capable), the most favorable technologies are ceramic capacitors and organic semiconductor (OS CON) capacitors. The temperature dependence of the capacitance value and the ESR specification is important, particularly if the ESR is used as part of the compensation network for the feedback loop. If using through-hole-mounted parts, keep lead length as short as practical. Components with specifications for switching power converters are preferred. Decoupling capacitors must be mounted close to the IC.

Diodes

The choice of rectifier diodes depends on the output voltage range of the particular application. For low-voltage converters, the diode drop is a significant portion of the total loss, and must be kept to a minimum. In those cases, Schottky diodes are the preferred component for the design. At higher voltages, ultra-fast recovery diodes must be used, since Schottky components will not satisfy the reverse voltage specification.

For all cases, the specifications to be determined before choosing a diode are the peak current, the average current, the maximum reverse voltage, and the maximum acceptable rectification losses. Once a type is identified, a thermal analysis of the diode losses vs. total thermal resistance (from junction to ambient) must be carried out if the total power involved is significant.

Industrial-frequency (60Hz) rectifiers are not recommended for any function in these converters, due to their high capacitance and recovery losses. If using overdimensioned rectifiers, the junction capacitance influence must be reviewed.

Chip Information

TRANSISTOR COUNT: 1050

SUBSTRATE CONNECTED TO GND

Table 1. Component Manufacturers

DEVICE TYPE	MANUFACTURER	PHONE	FAX
Power FETs	International Rectifier	310-322-3333	310-322-3332
	Fairchild	408-822-2000	408-822-2102
Current-Sense Resistors	Dale-Vishay	402-564-3131	402-563-6418
Diodes	Motorola	303-675-2140	303-675-2150
	Central Semiconductor	516-435-1110	516-435-1824
Transistors	Central Semiconductor	516-435-1110	516-435-1824
Capacitors	Sanyo	619-661-6835	619-661-1055
	Taiyo Yuden	408-573-4150	408-573-4159
	AVX	803-946-0690	803-626-3123
Coils	Coiltronics	561-241-7876	561-241-9339

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Maxim Integrated:

MAX5003CEE+ MAX5003CEE+T MAX5003CSE+ MAX5003CSE+T MAX5003EEE+ MAX5003EEE+T MAX5003ESE+ MAX5003ESE+T MAX5003CEE MAX5003CEE-T MAX5003CSE MAX5003CSE-T MAX5003EEE MAX5003EEE-T MAX5003ESE MAX5003ESE-T