

The third function the DS1707/DS1708 performs is pushbutton reset control. The DS1707/DS1708 debounces the pushbutton input and guarantees an active reset pulse width of 130 ms minimum.

## OPERATION

### Power Monitor

The DS1707/DS1708 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When  $V_{CC}$  falls below the minimum  $V_{CC}$  tolerance, a comparator outputs the  $\overline{RST}$  and  $\overline{RST}$  signals.  $\overline{RST}$  and  $\overline{RST}$  are excellent control signals for a microprocessor, as processing is stopped at the last possible moment of valid  $V_{CC}$ . On power-up,  $\overline{RST}$  and  $\overline{RST}$  are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize.

### Pushbutton Reset

The DS1707/DS1708 provides an input pin for direct connection to a pushbutton reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that  $\overline{RST}$  and  $\overline{RST}$  signals of at least 130 ms minimum will be generated. The 130 ms delay commences as the pushbutton reset input is released from the low level. The pushbutton can be initiated by connecting the  $\overline{NMI}$  output to the  $\overline{PBRST}$  input as shown in Figure 3.

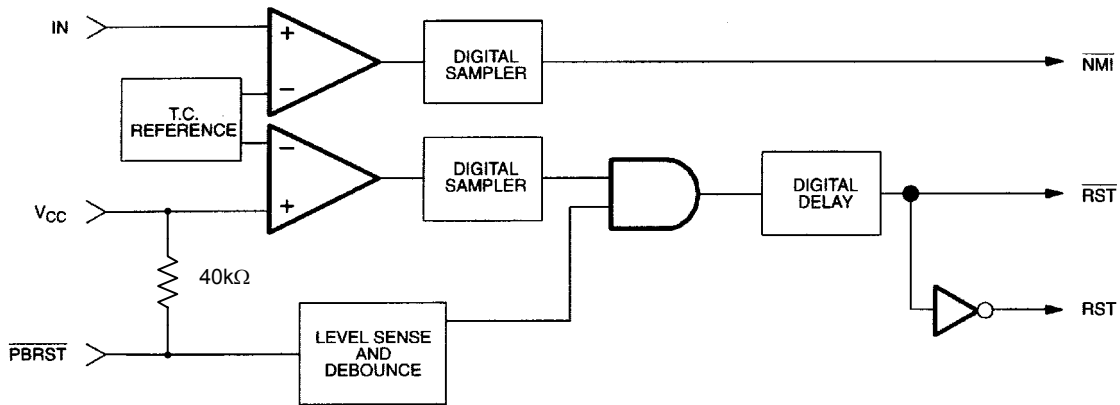
### Non-Maskable Interrupt

The DS1707/DS1708 generates a non-maskable interrupt ( $\overline{NMI}$ ) for early warning of a power failure. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from a regulated supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point  $V_{TP}$  is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1707/DS1708 requires that the voltage at the IN pin be limited to  $V_{CC}$ . Therefore, the maximum allowable voltage at the supply being monitored ( $V_{MAX}$ ) can also be derived as shown in Figure 5. A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shut-down between  $\overline{NMI}$  and  $\overline{RST}/\overline{RST}$ .

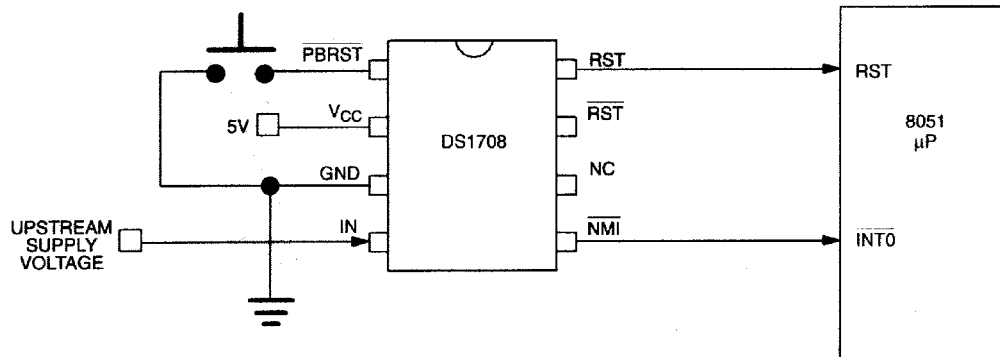
When the supply being monitored decays to the voltage sense point, the DS1707/DS1708 pulses the  $\overline{NMI}$  output to the active state for a minimum 200  $\mu s$ . The  $\overline{NMI}$  power-fail detection circuitry also has built-in hysteresis of 100  $\mu V$ . The supply must be below the voltage sense point for approximately 5  $\mu s$  before a low  $\overline{NMI}$  will be generated. In this way, power supply noise is removed from the monitoring function, preventing false interrupts. During a power-up, any detected IN pin levels below  $V_{TP}$  by the comparator are disabled from generating an interrupt until  $V_{CC}$  rises to  $V_{CCTP}$ . As a result, any potential  $\overline{NMI}$  pulse will not be initiated until  $V_{CC}$  reaches  $V_{CCTP}$ .

Connecting  $\overline{NMI}$  to  $\overline{PBRST}$  would allow the non-maskable interrupt to generate an automatic reset when an out-of-tolerance condition occurred in a monitored supply. An example is shown in Figure 3.

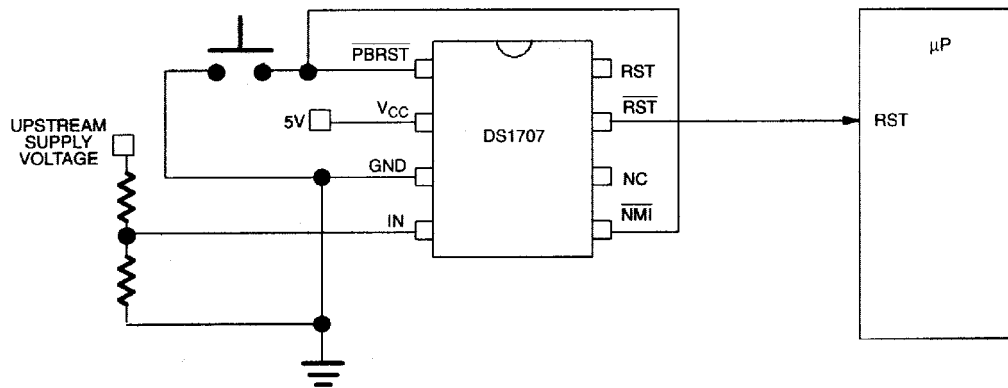
**MICROMONITOR BLOCK DIAGRAM Figure 1**



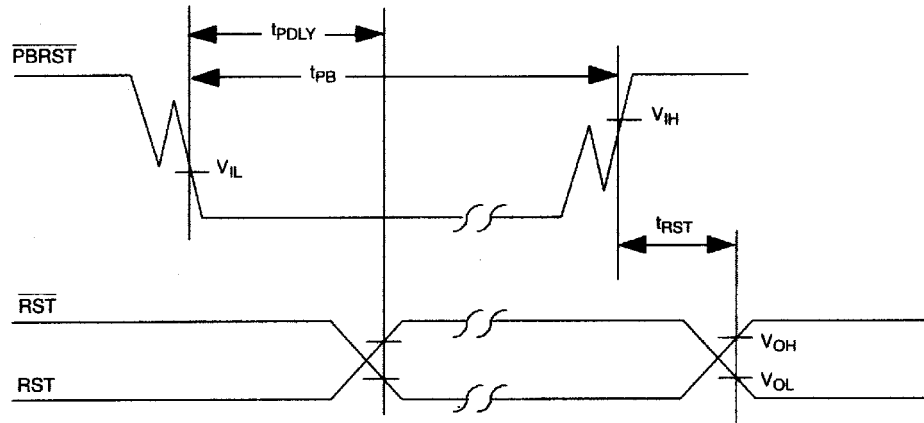
**PUSHBUTTON RESET Figure 2**



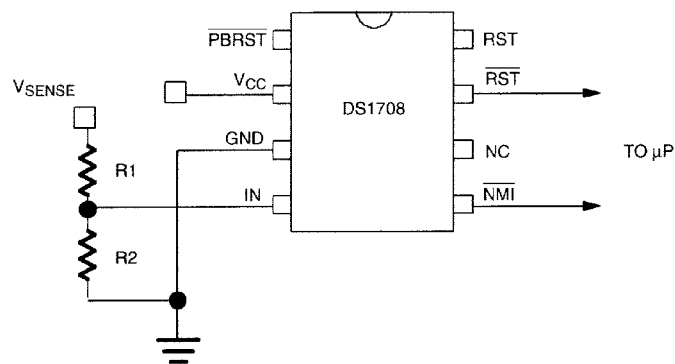
**PUSHBUTTON RESET CONTROLLED BY NMI Figure 3**



## TIMING DIAGRAM: PUSHBUTTON RESET Figure 4



## NON-MASKABLE INTERRUPT CIRCUIT EXAMPLE Figure 5



$$V_{\text{SENSE}} = \frac{R1 + R2}{R2} \times 1.25$$

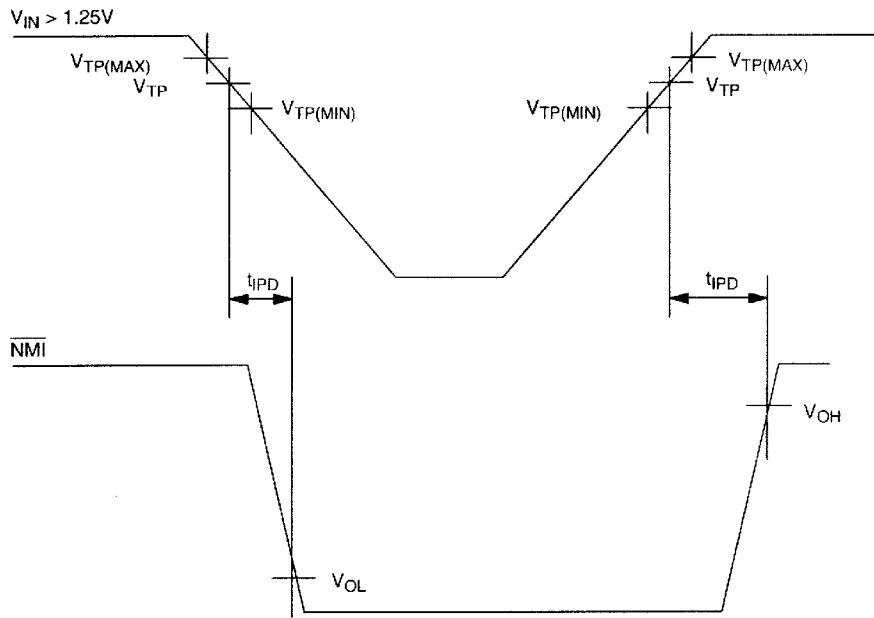
$$V_{\text{MAX}} = \frac{V_{\text{SENSE}}}{V_{\text{TP}}} \times V_{\text{CC}}$$

Example:  $V_{\text{SENSE}} = 4.50\text{V}$  at the trip point  
 $V_{\text{CC}} = 3.3\text{V}$   
 $10\text{ k}\Omega = R2$

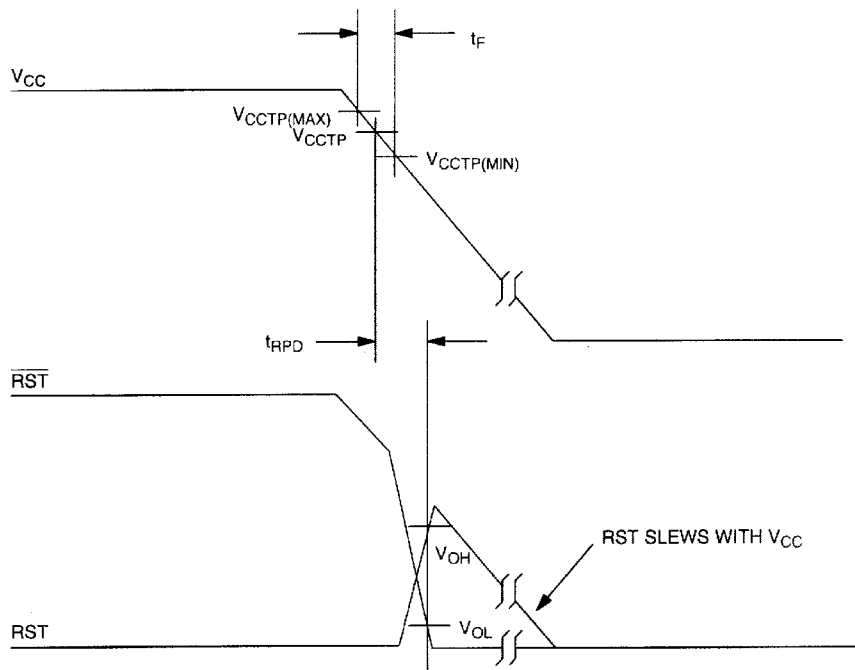
Therefore:  $\frac{4.50}{1.25} \times 3.3 = 11.88\text{V}$  maximum

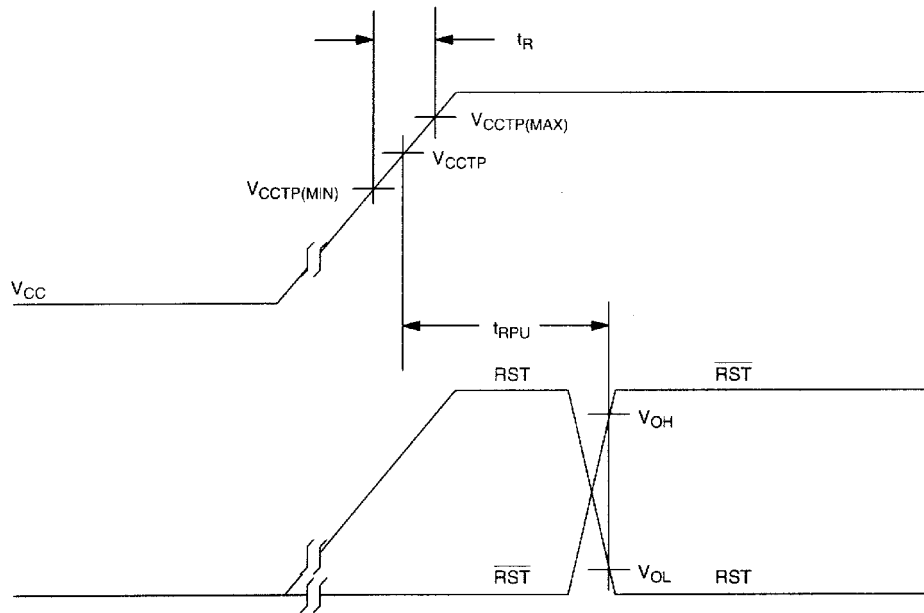
$$4.50 = \frac{R1 + 10\text{k}}{10\text{k}} \times 1.25 \quad R1 = 26\text{ k}\Omega$$

**TIMING DIAGRAM: NON-MASKABLE INTERRUPT Figure 6**



**TIMING DIAGRAM: POWER-DOWN Figure 7**



**TIMING DIAGRAM: POWER UP Figure 8**

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on V <sub>CC</sub> Pin Relative to Ground	-0.5V to +7.0V
Voltage on I/O Relative to Ground**	-0.5V to V <sub>CC</sub> + 0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

\*\* The voltage input limits on IN and  $\overline{\text{PBRST}}$  can be exceeded if the input current is less than 10 mA.

**RECOMMENDED DC OPERATING CONDITIONS** (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	1.2		5.5	V	1
$\overline{\text{PBRST}}$ Input High Level	V <sub>IH</sub>	2.0 V <sub>CC</sub> -0.5		V <sub>CC</sub> +0.3	V	1, 3 1, 4
$\overline{\text{PBRST}}$ Input Low Level	V <sub>IL</sub>	-0.03		+0.5	V	1

**DC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C; V<sub>CC</sub>=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> Trip Point DS1707	V <sub>CC</sub> TP	4.50	4.65	4.75	V	1
V <sub>CC</sub> Trip Point DS1708	V <sub>CC</sub> TP	4.25	4.40	4.50	V	1
V <sub>CC</sub> Trip Point DS1708T	V <sub>CC</sub> TP	3.00	3.08	3.15	V	1
V <sub>CC</sub> Trip Point DS1708S	V <sub>CC</sub> TP	2.85	2.93	3.00	V	1
V <sub>CC</sub> Trip Point DS1708R	V <sub>CC</sub> TP	2.55	2.63	2.70	V	1
Input Leakage	I <sub>IL</sub>	-1.0		+1.0	μA	2
Output Current @ 2.4V	I <sub>OH</sub>		350		μA	3
Output Current @ 0.4V	I <sub>OL</sub>	10			mA	3
Output Voltage @ -500μA	V <sub>OH</sub>	V <sub>CC</sub> -0.3	V <sub>CC</sub> -0.1		V	3
Operating Current @ V <sub>CC</sub> < 5.5V	I <sub>CC</sub>			60	μA	5
Operating Current @ V <sub>CC</sub> < 3.6V	I <sub>CC</sub>			50	μA	5
IN Input Trip Point	V <sub>TP</sub>	1.20	1.25	1.30	V	1

**CAPACITANCE** (t<sub>A</sub>=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			5	pF	
Output Capacitance	C <sub>OUT</sub>			7	pF	

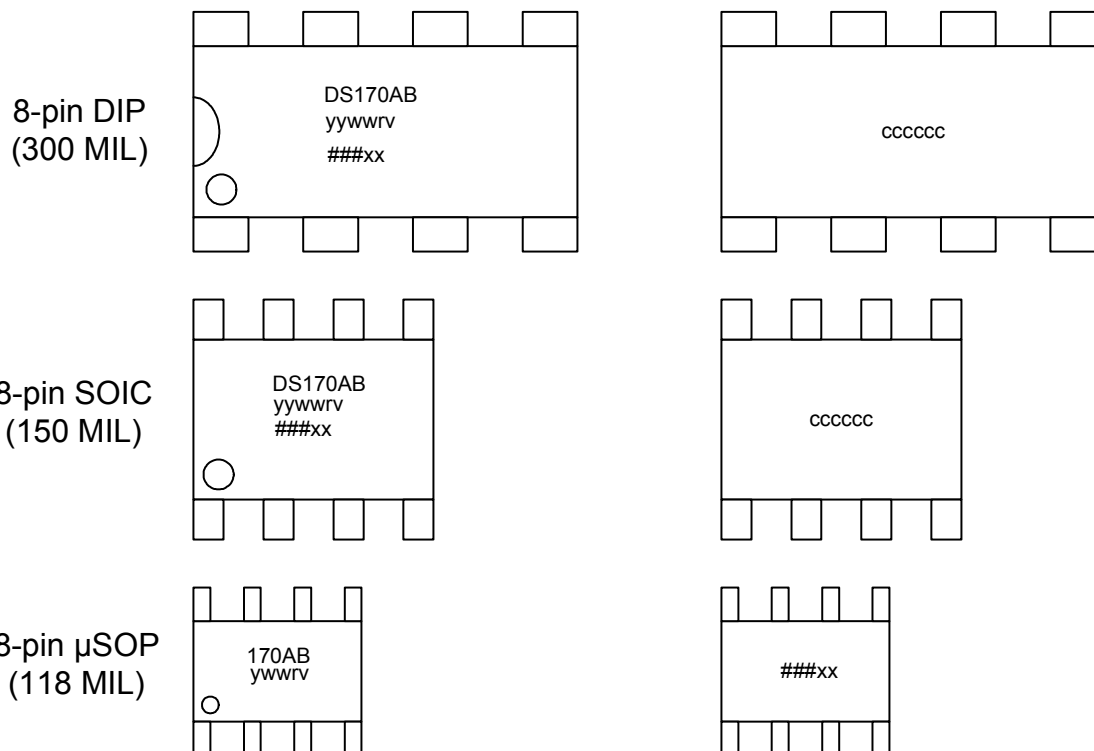
**AC ELECTRICAL CHARACTERISTICS** (-40°C to +85°C;  $V_{CC}=1.2V$  to  $5.5V$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST} = V_{IL}$	$t_{PB}$	150			ns	
Reset Active Time	$t_{RST}$	130	205	285	ms	
$V_{CC}$ Detect to RST and $\overline{RST}$	$t_{RPD}$		5	8	$\mu s$	7
$V_{CC}$ Slew Rate	$t_F$	20			$\mu s$	
$V_{CC}$ Detect to RST and $\overline{RST}$	$t_{RPU}$	130	205	285	ms	6
$V_{CC}$ Slew Rate	$t_R$	0			ns	
$\overline{PBRST}$ Stable Low to RST and $\overline{RST}$	$t_{PDLY}$			250	ns	
VIN Detect to $\overline{NMI}$	$t_{IPD}$		5	8	$\mu s$	7

**NOTES:**

1. All voltages are referenced to ground.
2.  $\overline{PBRST}$  is internally pulled up to  $V_{CC}$  with an internal impedance of 40 k $\Omega$  typical.
3.  $V_{CC} \geq 2.4V$
4.  $V_{CC} < 2.4V$
5. Measured with outputs open and all inputs at  $V_{CC}$  or ground.
6.  $t_R = 5 \mu s$
7. Noise immunity - pulses  $< 2 \mu s$  at  $V_{CCTP}$  minimum will not cause a reset.

## PART MARKING CODES



Brand Codes		
Code	Description	Values
AB	Device type and tolerance	7_, 8_, 8R, 8S, 8T (where '_' is a blank)
yww or yyww	Date Code. Identifies the year and work week the device was assembled.	y, the last digit of the year. yy, the last two digits of the year. ww, the work week (values 01 through 52).
rv	Die Revision	A letter followed by a number (eg. B1)
###xx	Lot Code	Three numbers followed by 2 letters
ccccc	Country of Assembly	Abbreviation of country name.



## ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	OPERATING TEMPERATURE	VERSION
DS1707EPA	8-pin DIP (300mil)	-40°C TO +85°C	5V-5% MONITOR, /RST, RST
DS1707ESA	8-pin SOIC (150 mil)	-40°C TO +85°C	5V-5% MONITOR, /RST, RST
DS1707EUA	8-pin $\mu$ SOP (118 mil)	-40°C TO +85°C	5V-5% MONITOR, /RST, RST
DS1708EPA	8-pin DIP (300mil)	-40°C TO +85°C	5V-10% MONITOR, /RST, RST
DS1708ESA	8-pin SOIC (150 mil)	-40°C TO +85°C	5V-10% MONITOR, /RST, RST
DS1708EUA	8-pin $\mu$ SOP (118 mil)	-40°C TO +85°C	5V-10% MONITOR, /RST, RST
DS1708REPA	8-pin DIP (300mil)	-40°C TO +85°C	3.3V-20% MONITOR, /RST, RST
DS1708RESA	8-pin SOIC (150 mil)	-40°C TO +85°C	3.3V-20% MONITOR, /RST, RST
DS1708REUA	8-pin $\mu$ SOP (118 mil)	-40°C TO +85°C	3.3V-20% MONITOR, /RST, RST
DS1708SEPA	8-pin DIP (300mil)	-40°C TO +85°C	3.3V-10% MONITOR, /RST, RST
DS1708SESA	8-pin SOIC (150 mil)	-40°C TO +85°C	3.3V-10% MONITOR, /RST, RST
DS1708SEUA	8-pin $\mu$ SOP (118 mil)	-40°C TO +85°C	3.3V-10% MONITOR, /RST, RST
DS1708TEPA	8-pin DIP (300mil)	-40°C TO +85°C	3.3V-5% MONITOR, /RST, RST
DS1708TESA	8-pin SOIC (150 mil)	-40°C TO +85°C	3.3V-5% MONITOR, /RST, RST
DS1708TEUA	8-pin $\mu$ SOP (118 mil)	-40°C TO +85°C	3.3V-5% MONITOR, /RST, RST

\*Contact factory for availability of Pb-free versions.

E = -40°C to +85°C temperature range

A = 8 lead device

P = Plastic DIP (300 mil)

S = SOIC (150 mil)

U =  $\mu$ SOP (118 mil)

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