4MHz, 500mA Synchronous Step-Down DC-DC Converters in Thin SOT and TDFN

ABSOLUTE MAXIMUM RATINGS

IN, FB, $\overline{SHDN}$, ODI, ODO to GND .....-0.3V to +6V
LX to GND (Note 1).....-0.3V to (V_{IN} + 0.3V)
PGND to GND .....-0.3V to +0.3V
LX Current.....1.27A
Output Short Circuit to GND
(typical operating circuit).....10s
Continuous Power Dissipation (T_A = +70°C)
5-Pin Thin SOT23 (derate 9.1mW/°C above +70°C)....727mW
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has internal clamp diodes to PGND (GND for MAX8560) and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, $\overline{SHDN}$ = IN, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}			2.7		5.5	V
UVLO Threshold	UVLO	V_{IN} rising, 60mV hysteresis		2.4	2.5	2.6	V
Supply Current	I_{IN}	I_{LOAD} = 0mA, no switching			40	80	µA
		$\overline{SHDN}$ = GND	T_A = +25°C		0.01	0.1	
			T_A = +85°C		0.1		
Output Voltage Range	V_{OUT}			0.6		2.5	V
FB Threshold Voltage	V_{FB}	V_{FB} falling			0.6		V
FB Threshold Line Regulation		V_{IN} = 2.7V to 5.5V			0.3		%/V
FB Threshold Load Regulation		I_{OUT} = 0 to 500mA			-0.001		%/mA
FB Threshold Voltage Accuracy (Falling) (% of V_{FB})		I_{LOAD} = 0mA	T_A = +25°C	-1.5		+1.5	%
			T_A = -40°C to +85°C	-2.5		+2.5	
FB Threshold Voltage Hysteresis (% of V_{FB})	V_{HYS}				1.0		%
FB Bias Current	I_{FB}	$\overline{SHDN}$ = GND, T_A = +25°C, V_{IN} = 5.5V			0.01	0.1	µA
		$\overline{SHDN}$ = GND, T_A = +85°C, V_{IN} = 5.5V			0.1		
		V_{FB} = 0.5V, T_A = +25°C, V_{IN} = 5.5V			0.01	0.1	
		V_{FB} = 0.5V, T_A = +85°C, V_{IN} = 5.5V			0.1		
Logic Input High Voltage ($\overline{SHDN}$, ODI)	V_{IH}	V_{IN} = 2.7V to 5.5V		1.41			V
Logic Input Low Voltage ($\overline{SHDN}$, ODI)	V_{IL}	V_{IN} = 2.7V to 5.5V				0.4	
Logic Input Bias Current	I_{IH}, I_{IL}	V_{IN} = 5.5V, $\overline{SHDN}$ = ODI = GND or IN, T_A = +25°C			0.001	0.1	µA
		V_{IN} = 5.5V, $\overline{SHDN}$ = ODI = GND or IN, T_A = +85°C			0.01		
ODO Output Low Voltage (MAX8562 Only)	V_{OL}	1mA sink current, V_{IN} = 2.7V			0.02	0.1	V

ELECTRICAL CHARACTERISTICS (continued)

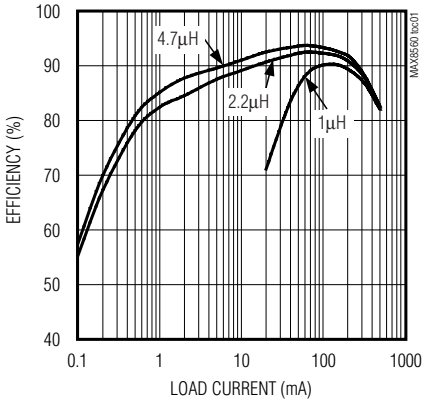
(V_{IN} = 3.6V, $\overline{SHDN}$ = IN, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ODO Pullup to IN (MAX8562 Only)			5	10	20	kΩ
Open-Drain Output Leakage	I_{OHLEAK}	V_{IN} = 5.5V, ODO = IN, T_A = +25°C		0.01	0.1	µA
		V_{IN} = 5.5V, ODO = IN, T_A = +85°C		0.1		
Current Limit	I_{LIMP}	PFET switch	600	990	1500	mA
	I_{LIMN}	NFET rectifier	490	680	900	
On-Resistance	R_{ONP}	PFET switch, I_{LX} = -40mA		0.8	1.5	Ω
	R_{ONN}	NFET rectifier, I_{LX} = +40mA		0.4	0.82	
Rectifier-Off Current Threshold	I_{LXOFF}		0	30	60	mA
LX Leakage Current	I_{LXLKG}	V_{IN} = 5.5V, LX = GND to IN, ODO = IN, T_A = +25°C, $\overline{SHDN}$ = GND		0.1	1	µA
		V_{IN} = 5.5V, LX = GND to IN, ODO = IN, T_A = +85°C, $\overline{SHDN}$ = GND		1		
Minimum On- and Off-Times	$t_{ON(MIN)}$			107		ns
	$t_{OFF(MIN)}$			95		
Thermal Shutdown				+160		°C
Thermal-Shutdown Hysteresis				20		°C

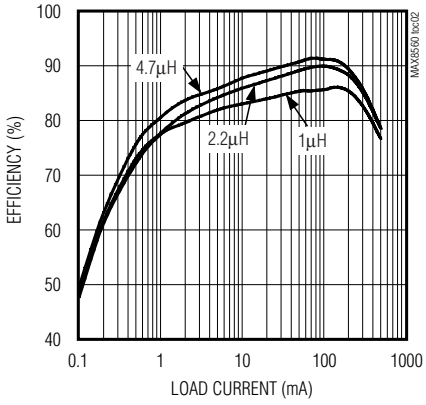
Typical Operating Characteristics

(V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH (LQH32CN1R0M53), C_{OUT} = 2.2µF, T_A = +25°C, unless otherwise noted.)

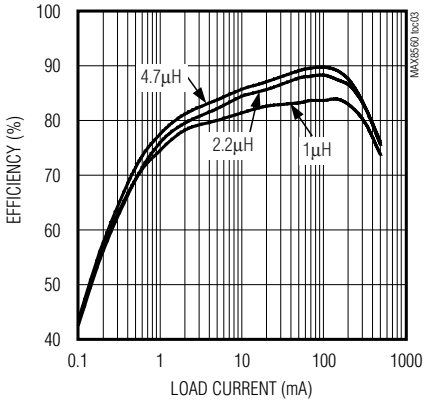
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 2.5V)



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.8V)



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.5V)

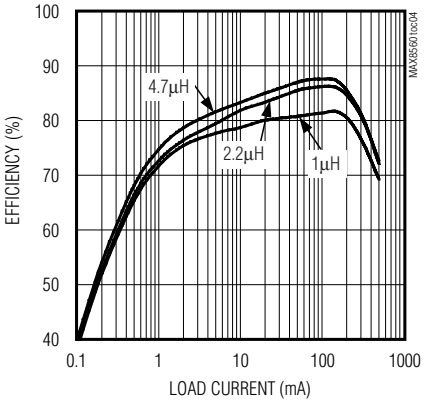


4MHz, 500mA Synchronous Step-Down DC-DC Converters in Thin SOT and TDFN

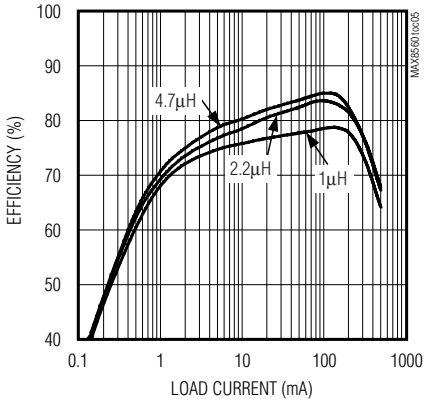
Typical Operating Characteristics (continued)

(V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH (LQH32CN1R0M53), C_{OUT} = 2.2µF, T_A = +25°C, unless otherwise noted.)

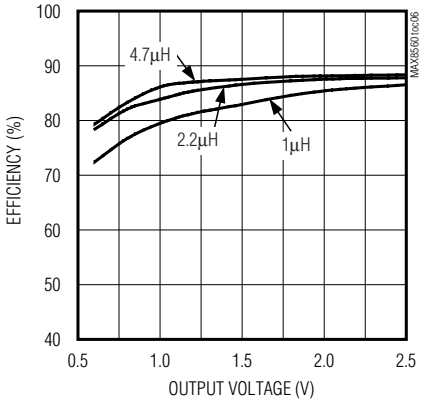
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



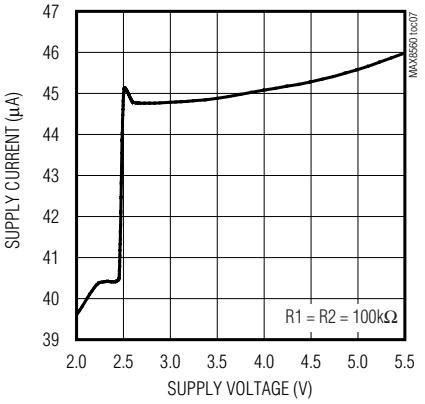
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.9V)



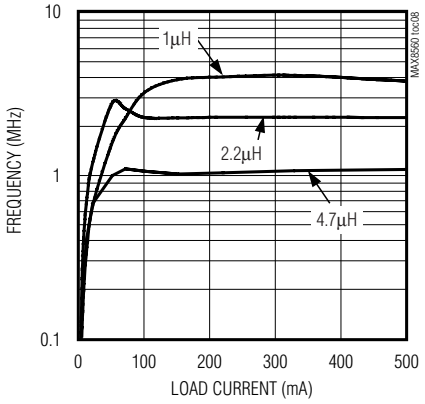
EFFICIENCY vs. LOAD CURRENT (LOAD = 7.5Ω)



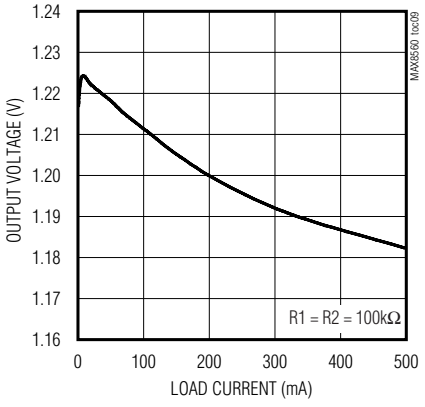
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



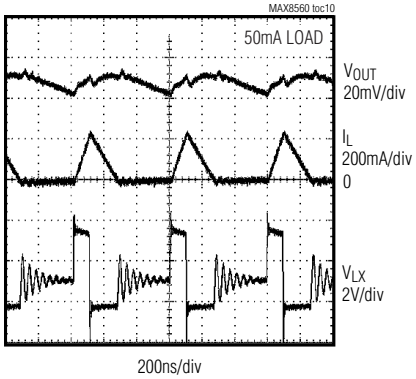
SWITCHING FREQUENCY vs. LOAD CURRENT



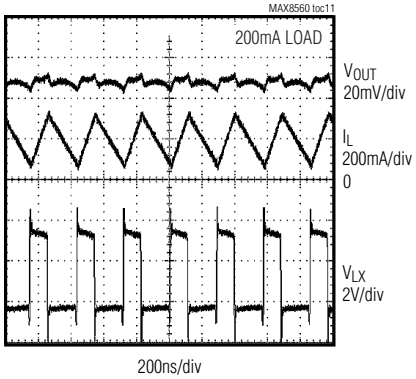
OUTPUT VOLTAGE vs. LOAD CURRENT (VOLTAGE POSITIONING)



LIGHT-LOAD SWITCHING WAVEFORMS



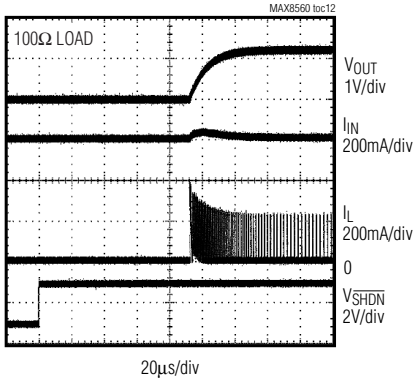
HEAVY-LOAD SWITCHING WAVEFORMS



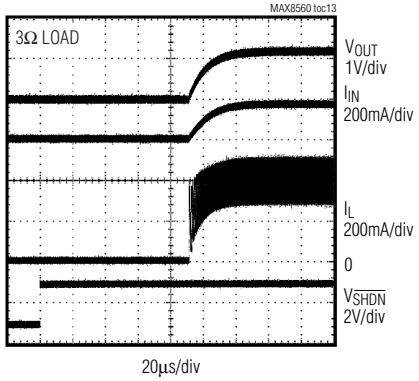
Typical Operating Characteristics (continued)

(V_{IN} = 3.6V, V_{OUT} = 1.2V, L = 1µH (LQH32CN1R0M53), C_{OUT} = 2.2µF, T_A = +25°C, unless otherwise noted.)

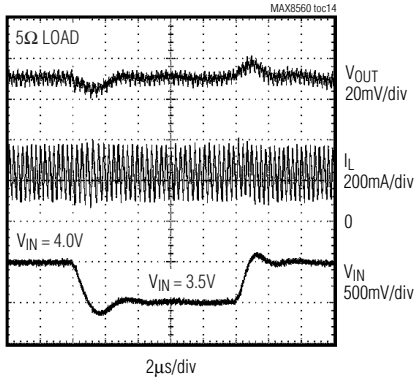
LIGHT-LOAD SOFT-START WAVEFORMS



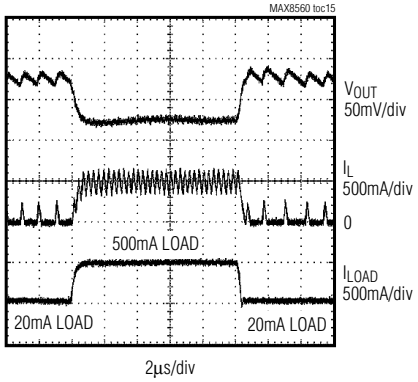
HEAVY-LOAD SOFT-START WAVEFORMS



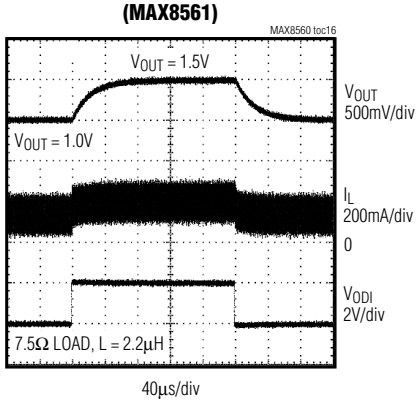
LINE-TRANSIENT RESPONSE



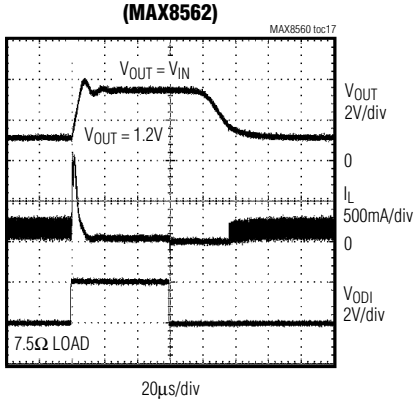
LOAD-TRANSIENT RESPONSE



OUTPUT-VOLTAGE TRANSIENT RESPONSE (MAX8561)



BYPASS-FET TRANSIENT RESPONSE (MAX8562)



4MHz, 500mA Synchronous Step-Down DC-DC Converters in Thin SOT and TDFN

Pin Description

PIN		NAME	FUNCTION
MAX8560	MAX8561 MAX8562		
1	1	IN	Supply Voltage Input. 2.7V to 5.5V. Bypass with a 2.2µF ceramic capacitor as close as possible to the IN and GND pins.
2	7	GND	Ground
3	8	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to IN or logic high for normal operation. Connect to GND or logic low for shutdown mode.
4	6	FB	Voltage Feedback Input. FB regulates to 0.6V nominal. Connect FB to the center of an external resistive divider (see the *Setting the Output Voltage* section).
—	2	PGND	Power Ground. Must connect to GND.
5	3	LX	Inductor connection to the drains of the internal P-channel and N-channel MOSFETs.
—	5	ODO	Auxiliary Open-Drain Output
—	4	ODI	Digital Input for Open-Drain MOSFET. Connect to IN or logic high to internally pull ODO low (and force the MAX8562 into 100% duty cycle). Connect to GND or logic low to force ODO to high impedance (MAX8561) or 10kΩ pullup from ODO to IN (MAX8562).
—	EP	EP	Exposed Pad. Connect to GND.

Detailed Description

The MAX8560/MAX8561/MAX8562 step-down converters deliver a guaranteed 500mA at output levels from 0.6V to 2.5V. They use a proprietary hysteretic-PWM control scheme that switches up to 4MHz, allowing a trade-off between efficiency and tiny external components. At light loads below 100mA, the MAX8560/MAX8561/MAX8562 automatically switch to pulse-skipping mode to keep quiescent supply current as low as 40µA (typ).

Control Scheme

A proprietary hysteretic-PWM control scheme ensures high efficiency, fast switching, fast transient response, low output ripple, and physically tiny external components. This control scheme is simple: when the output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This switch remains on until the minimum on-time expires and the output voltage is in regulation or the current-limit threshold is exceeded. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again, below the regulation threshold. During this period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on again or the inductor current approaches zero. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

As seen in the *Typical Operating Circuit*, the MAX8560/MAX8561/MAX8562 use a unique feedback network. By taking feedback from the LX node through R1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of a very small ceramic output capacitor. This configuration causes the output voltage to shift by the inductor series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients, which effectively halves the peak-to-peak output-voltage excursions compared to traditional step-down converters. See the Load Transient Response graph in the *Typical Operating Characteristics* section.

Shutdown Mode

Connecting $\overline{SHDN}$ to GND or logic low places the MAX8560/MAX8561/MAX8562 in shutdown mode and reduces supply current to 0.1µA. In shutdown, the control circuitry, internal-switching P-channel MOSFET, and synchronous rectifier (N-channel MOSFET) turn off and LX becomes high impedance. Connect $\overline{SHDN}$ to IN or logic high for normal operation.

Soft-Start

The MAX8560/MAX8561/MAX8562 have internal soft-start circuitry that eliminates inrush current at startup, reducing transients on the input source. Soft-start is particularly useful for higher impedance input sources, such as Li+ and alkaline cells. See the Soft-Start and Shutdown Response graphs in the *Typical Operating Characteristics* section.

Open-Drain Output

The 8-pin TDFN versions, the MAX8561 and MAX8562, include an extra, internal, open-drain N-channel MOSFET switch that can save an additional package in space-constrained applications. The open drain is connected to ODO, while the gate is controlled by a digital input at ODI. For the MAX8561, this circuit can be used to toggle between two regulated output voltages, as in Figure 2. For the MAX8562, a 10kΩ resistor pulls ODO up to IN when ODI is low, and the buck converter is forced into 100% duty cycle when ODI is high. This makes the MAX8562 ideal for driving an external bypass PFET for high-power mode in CDMA cell phones, as in Figure 3.

Applications Information

The MAX8560/MAX8561/MAX8562 are optimized for use with tiny inductors and small ceramic capacitors. The correct selection of external components, especially C_{FF}, ensures high efficiency, low output ripple, and fast transient response.

Setting the Output Voltage

Select an output voltage between 0.6V and 2.5V by connecting FB to a resistive voltage-divider between LX and GND (see the *Typical Operating Circuit*). Choose R2 for a reasonable bias current in the resistive divider. A wide range of resistor values is acceptable, but a good starting point is to choose R2 as 100kΩ. Then, R1 is given by:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.6V.

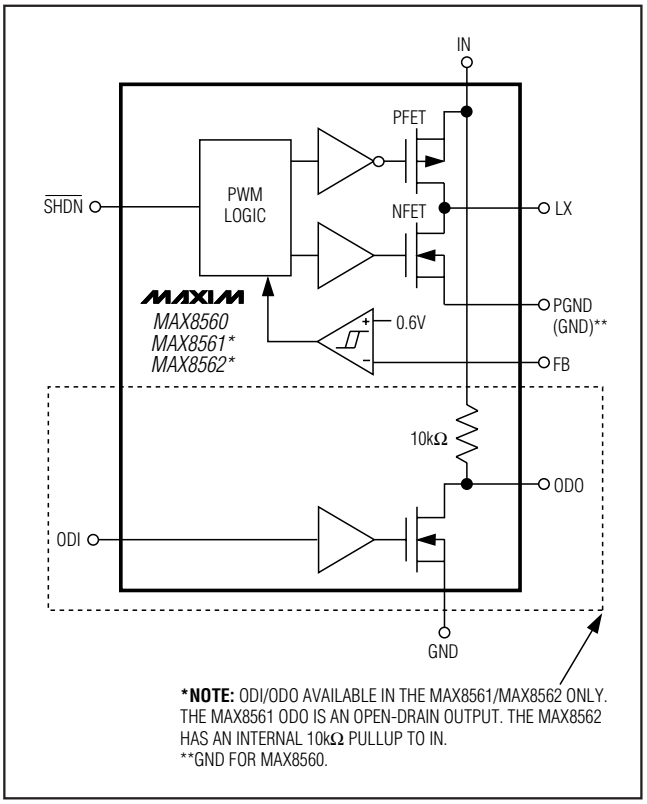


Figure 1. Simplified Functional Diagram

Inductor Selection

The MAX8560/MAX8561/MAX8562 operate with inductors of 1µH to 4.7µH. Low inductance values are smaller but require faster switching, which results in some efficiency loss. See the *Typical Operating Characteristics* section for efficiency and switching frequency vs. inductor value. The inductor's DC current rating only needs to match the maximum load current of the application + 50mA because the MAX8560/MAX8561/ MAX8562 feature zero current overshoot during startup and load transients.

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor is 2.2µH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. For higher efficiency at heavy loads (above 200mA) or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. For light-load applications up to 200mA, much higher resistance is acceptable with very little impact on performance.

4MHz, 500mA Synchronous Step-Down DC-DC Converters in Thin SOT and TDFN

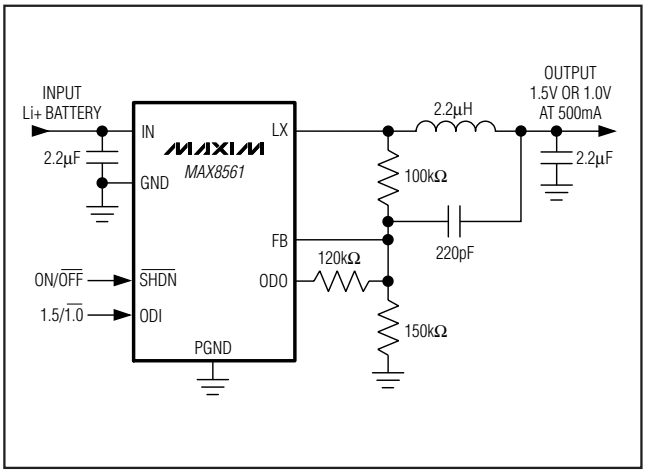


Figure 2. Using ODI/ODO to Obtain Two Output Voltages from the MAX8561

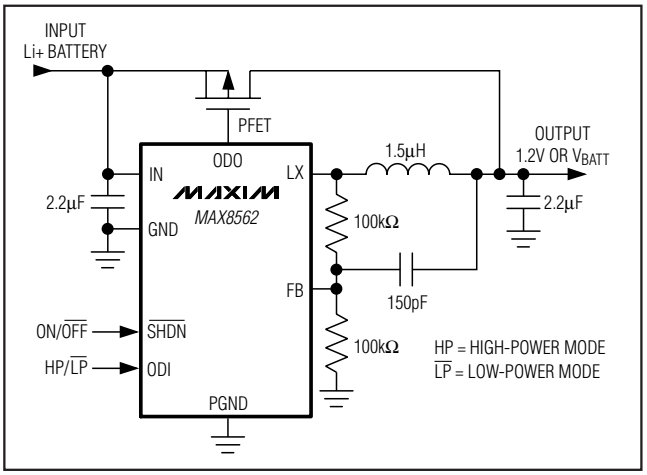


Figure 3. Using the MAX8562 to Control an External Bypass PFET for a Two-Step V_{CC} in CDMA-PA Applications

Capacitor Selection

Output Capacitor

The output capacitor, C_{OUT}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. For most applications, a 2.2µF capacitor is sufficient. For optimum load-transient performance and very low output ripple, the output capacitor value in µFs should be equal to or larger than the inductor value in µHs.

Input Capacitor

The input capacitor, C_{IN}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the MAX8560/MAX8561/MAX8562s' soft-start, the input capacitance can be very low. For most applications, a 2.2µF capacitor is sufficient.

Feed-Forward Capacitor

The feed-forward capacitor, C_{FF}, sets the feedback loop response, controls the switching frequency, and is critical in obtaining the best efficiency possible. Choose a small ceramic X7R capacitor with a value given by:

$$C_{FF} = \frac{L}{R1} \times 10 \text{ Siemens}$$

Select the closest standard value to C_{FF} as possible.

PC Board Layout and Routing

High switching frequencies and relatively large peak currents make the PC board layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect C_{IN} close to IN and GND. Connect the inductor and output capacitor as close to the IC as possible and keep their traces short, direct, and wide. Connect GND and PGND separately to the ground plane. The external feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces, such as the LX node, as short as possible. For the 8-pin TDFN package, connect GND to the exposed paddle directly under the IC. Figure 4 illustrates an example PC board layout and routing scheme.

Table 1. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS
Taiyo Yuden	LB2012	1.0 2.2	0.15 0.23	300 240	2.0 x 1.25 x 1.45 = 3.6mm^3
	LB2016	1.0 1.5 2.2 3.3	0.09 0.11 0.13 0.20	455 350 315 280	2.0 x 1.6 x 1.8 = 5.8mm^3
	LB2518	1.0 1.5 2.2 3.3	0.06 0.07 0.09 0.11	500 400 340 270	2.5 x 1.8 x 2.0 = 9mm^3
	LBC2518	1.0 1.5 2.2 3.3 4.7	0.08 0.11 0.13 0.16 0.20	775 660 600 500 430	2.5 x 1.8 x 2.0 = 9mm^3
Murata	LQH31C_03	1.0	0.28	510	3.2 x 1.6 x 2.0 = 10mm^3
	LQH32C_53	1.0 2.2 4.7	0.06 0.10 0.15	1000 790 650	3.2 x 2.5 x 1.7 = 14mm^3
	LQM43FN	2.2 4.7	0.10 0.17	400 300	4.5 x 3.2 x 0.9 = 13mm^3
TOKO	D310F	1.5 2.2 3.3	0.13 0.17 0.19	1230 1080 1010	3.6 x 3.6 x 1.0 = 13mm^3
	D312C	1.5 2.2 2.7 3.3	0.10 0.12 0.15 0.17	1290 1140 980 900	3.6 x 3.6 x 1.2 = 16mm^3
Sumida	CDRH2D11	1.5 2.2 3.3 4.7	0.05 0.08 0.10 0.14	900 780 600 500	3.2 x 3.2 x 1.2 = 12mm^3

4MHz, 500mA Synchronous Step-Down DC-DC Converters in Thin SOT and TDFN

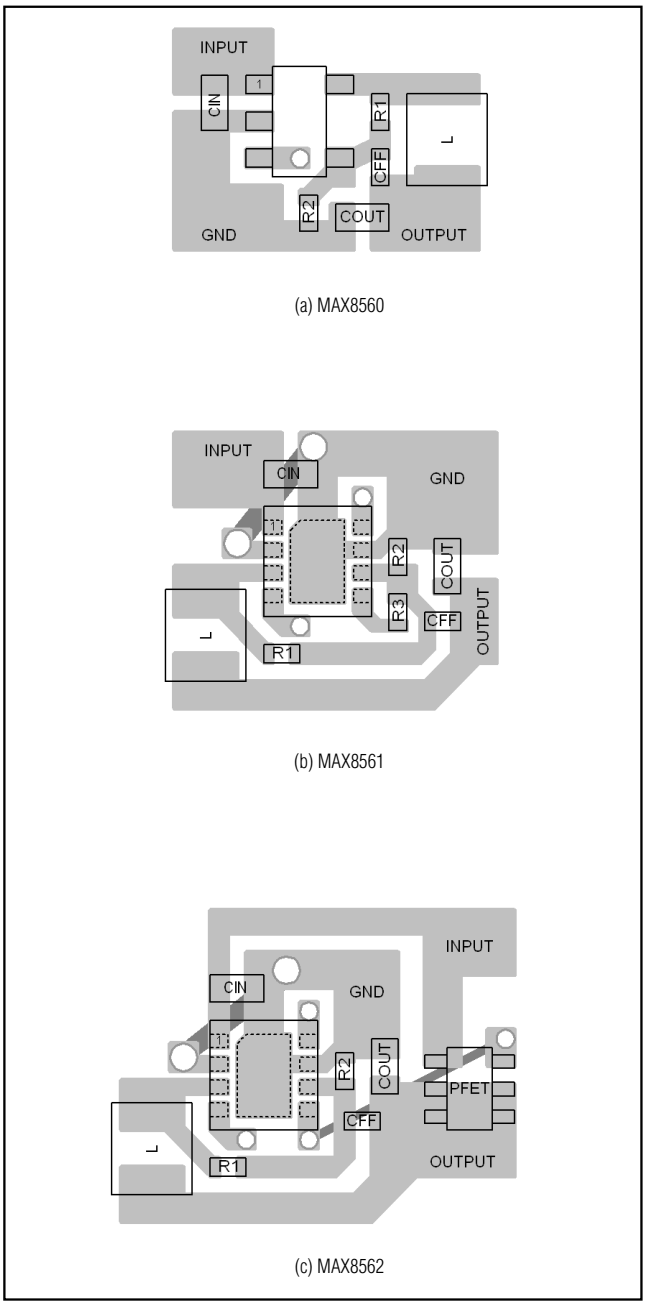


Figure 4. Recommended PC Board Layout

Chip Information

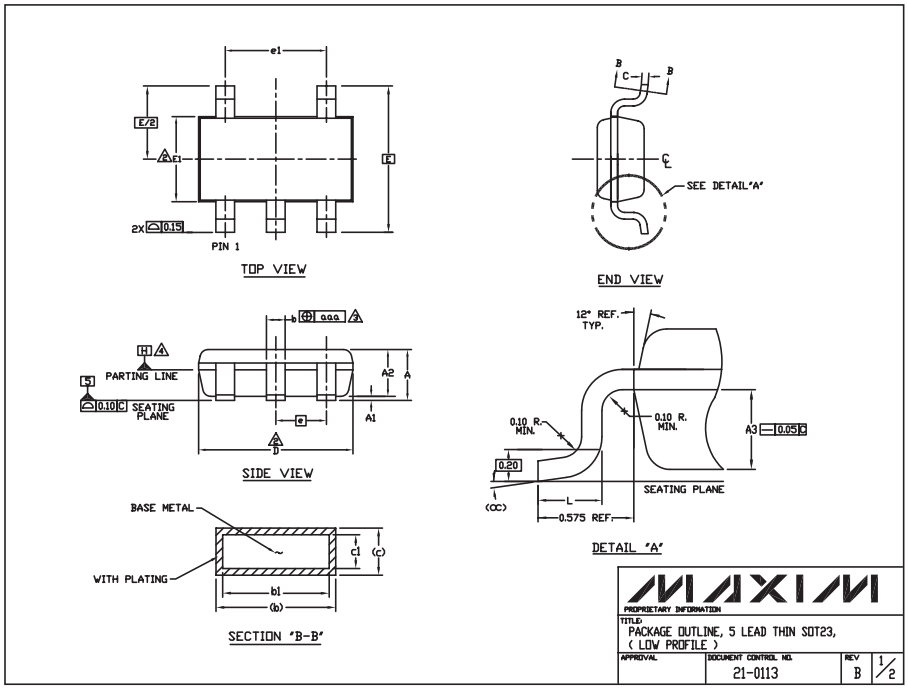
TRANSISTOR COUNT: 1271

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

THIN SOT23.EPS



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.

3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.

5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.

6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95Mmm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.

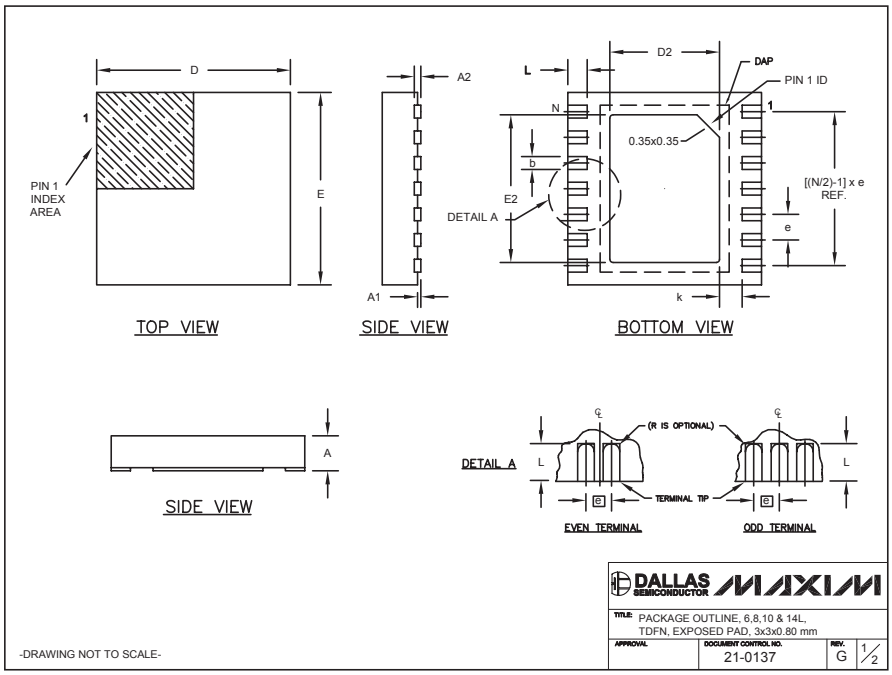
SYMBOLS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.05	0.075	0.10
A2	0.85	0.88	0.90
A3		0.50 BSC	
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
cc	0°	4°	8°
aaa		0.20	

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 5 LEAD THIN SOT23, (LOW PROFILE)
APPROVAL
DOCUMENT CONTROL NO. 21-0113
REV B
2/2

4MHz, 500mA Synchronous Step-Down DC-DC Converters in Thin SOT and TDFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. G
2/2
-DRAWING NOT TO SCALE-

Mouser Electronics

Authorized Distributor

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Maxim Integrated:

MAX8560EZK+T MAX8561ETA+T MAX8560EZK-T