# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

## ABSOLUTE MAXIMUM RATINGS

VP, $\overline{SHDN}$ to GND .....-0.3V to +22V
VP to VL .....-0.3V to +22V
OUT, VL to GND .....-0.3V to +6V
DL, FB, REF to GND .....-0.3V to (VL + 0.3V)
DH to GND .....-0.3V to (VP + 0.3V)
CS to GND .....-2.0V to (VP + 0.3V)
REF Short Circuit to GND .....Continuous

Continuous Power Dissipation ($T_A$ = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) .....444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{VP}$ = 15V, VL enabled, $C_{VL}$ = 1µF, $C_{REF}$ = 0.1µF, **$T_A$ = 0 to +85°C,** unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| VP Input Voltage Range | $V_{VP}$ | | | 5 | | 20 | V |
| VL Input Voltage Range | $V_{VL}$ | VL (overdriven) | | 4.75 | | 5.25 | V |
| OUT Output Voltage (MAX1762, 1.8V Fixed) | $V_{OUT}$ | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = GND, continuous conduction mode | | 1.773 | 1.8 | 1.827 | V |
| OUT Output Voltage (MAX1762, 2.5V Fixed) | $V_{OUT}$ | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = VL, continuous conduction mode | | 2.463 | 2.5 | 2.538 | V |
| OUT Output Voltage (MAX1791, 3.3V Fixed) | $V_{OUT}$ | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = GND, continuous conduction mode | | 3.250 | 3.3 | 3.350 | V |
| OUT Output Voltage (MAX1791, 5V Fixed) | $V_{OUT}$ | $V_{VP}$ = 7V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = VL, continuous conduction mode | | 4.925 | 5 | 5.075 | V |
| OUT Output Voltage (Adj Mode) | | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = OUT, continuous conduction mode | | 1.231 | 1.250 | 1.269 | V |
| Output Voltage Adjust Range | | | | 0.5 | | 5.5 | V |
| OUT Input Resistance | | Adjustable-output mode | | 300 | 800 | 1700 | kΩ |
| FB Input Bias Current | | $V_{FB}$ = 1.3V | | -0.1 | | 0.1 | µA |
| Soft-Start Ramp Time | | Zero to full $I_{LIM}$ | | | 1700 | | µs |
| On-Time (Note 2) | $t_{ON}$ | $V_{OUT}$ = 1.25V, $V_{VP}$ = 6V | | 666 | 740 | 814 | ns |
| | | $V_{OUT}$ = 5V, $V_{VP}$ = 6V | | 2550 | 2830 | 3110 | |
| Minimum Off-Time | $t_{OFF}$ | (Note 2) | | 300 | 400 | 500 | ns |
| VL Quiescent Supply Current | | FB = GND, $V_{VL}$ = 5V, OUT forced above the regulation point | | | 153 | 260 | µA |
| VP Quiescent Supply Current | | FB = GND, OUT forced above the regulation point, $V_{VP}$ = 20V | $V_{VL}$ = float | | 227 | 410 | µA |
| | | | $V_{VL}$ = 5V | | 93 | 200 | |
| VL Shutdown Supply Current | | $V_{VL}$ = 5V, $\overline{SHDN}$ = GND | | | 2 | 15 | µA |
| VP Shutdown Supply Current | | $\overline{SHDN}$ = GND, measured at VP, $V_{VL}$ = 0 or 5V | | | 4 | 12 | µA |
| VL Output Voltage | | $I_{LOAD}$ = 0 to 25mA, $V_{VP}$ = 5V to 20V | | 4.5 | 4.65 | 4.75 | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{VP}$ = 15V, VL enabled, $C_{VL}$ = 1µF, $C_{REF}$ = 0.1µF, **$T_A$ = 0 to +85°C,** unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Reference Voltage | | $V_{VL}$ = 4.75V to 5.25V, no load | 1.98 | 2 | 2.02 | V |
| Reference Load Regulation | | $I_{REF}$ = 0 to 50µA | | | 0.01 | V |
| REF Sink Current | | REF in regulation | 10 | | | µA |
| REF Fault Lockout Voltage | | Falling edge | | 1.6 | | V |
| Output Undervoltage Threshold (Foldback) | | With respect to regulation point, no load | 60 | 70 | 80 | % |
| Output Undervoltage Lockout Time (Foldback) | | From $\overline{SHDN}$ signal going high $V_{OUT}$ < 0.6 x regulation point | 10 | 20 | 42 | ms |
| Current-Limit Threshold | $V_{ILIM}$ | | -90 | -100 | -110 | mV |
| Thermal Shutdown Threshold | | Hysteresis = 10°C | | 160 | | °C |
| VL Undervoltage Lockout Threshold | | Rising edge, hysteresis = 20mV, PWM disabled below this level | 4.1 | | 4.4 | V |
| DH Gate Driver On-Resistance | | $V_{VP}$ = 6V to 20V, measure at 50mA | | 5 | 8 | Ω |
| DL Gate Driver On-Resistance (Pullup) | | DL, high state, measure at 50mA | | 5 | 8 | Ω |
| DL Gate Driver On-Resistance (Pulldown) | | DL, low state, measure at 50mA | | 1 | 5 | Ω |
| DH Gate Driver Source/Sink Current | | $V_{DH}$ = 3V, $V_{VP}$ = 6V | | 0.6 | | A |
| DL Gate Driver Sink Current | | $V_{DL}$ = 2.5V | | 0.9 | | A |
| DL Gate Driver Source Current | | $V_{DL}$ = 2.5V | | 0.5 | | A |
| $\overline{SHDN}$ Logic Input High Threshold Voltage | $V_{IH}$ | | 1.6 | | | V |
| $\overline{SHDN}$ Logic Input Low Threshold Voltage | $V_{IL}$ | | | | 0.6 | V |
| Dual Mode Threshold Voltage | | MAX1762 $V_{OUT}$ = 1.8V fixed | 50 | 100 | 150 | mV |
| | | MAX1791 $V_{OUT}$ = 3.3V fixed | | | | |
| | | MAX1762 $V_{OUT}$ = 2.5V fixed | 2.5 | 3.25 | 4 | V |
| | | MAX1791 $V_{OUT}$ = 5V fixed | | | | |
| $\overline{SHDN}$ Logic Input Current | | $\overline{SHDN}$ = 0 or 5V | -2 | | +2 | µA |

# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

## ELECTRICAL CHARACTERISTICS

($V_{VP}$ = 15V, VL enabled, $C_{VL}$ = 1µF, $C_{REF}$ = 0.1µF, **$T_A$ = -40 to +85°C,** unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| VP Input Voltage Range | $V_{VP}$ | | 5 | | 20 | V |
| VL Input Voltage Range | $V_{VL}$ | VL (overdriven) | 4.75 | | 5.25 | V |
| OUT Output Voltage (MAX1762, 1.8V Fixed) | $V_{OUT}$ | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = GND, continuous conduction mode | 1.773 | | 1.827 | V |
| OUT Output Voltage (MAX1762, 2.5V Fixed) | $V_{OUT}$ | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = VL, continuous conduction mode | 2.463 | | 2.538 | V |
| OUT Output Voltage (MAX1791, 3.3V Fixed) | $V_{OUT}$ | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = GND, continuous conduction mode | 3.250 | | 3.350 | V |
| OUT Output Voltage (MAX1791, 5V Fixed) | $V_{OUT}$ | $V_{VP}$ = 7V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = VL, continuous conduction mode | 4.925 | | 5.075 | V |
| OUT Output Voltage (adj Mode) | | $V_{VP}$ = 5V to 20V, $V_{VL}$ = 4.75V to 5.25V, FB = OUT, continuous conduction mode | 1.231 | | 1.269 | V |
| FB Input Bias Current | | $V_{FB}$ = 1.3V | -0.2 | | 0.2 | µA |
| On-Time (Note 2) | $t_{ON}$ | $V_{OUT}$ = 1.25V, $V_{VP}$ = 6V | 666 | | 814 | ns |
| | | $V_{OUT}$ = 5V, $V_{VP}$ = 6V | 2550 | | 3110 | |
| Minimum Off-Time | $t_{OFF}$ | (Note 2) | 250 | | 550 | ns |
| VL Quiescent Supply Current | | FB = GND, $V_{VL}$ = 5V, OUT forced above the regulation point | | | 260 | µA |
| VP Quiescent Supply Current | | FB = GND, OUT forced above the regulation point $V_{VP}$ = 20V, $V_{VL}$ = float | | | 410 | µA |
| | | FB = GND, OUT forced above the regulation point $V_{VP}$ = 20V, $V_{VL}$ = 5V | | | 200 | |
| VL Shutdown Supply Current | | $V_{VL}$ = 5V, $\overline{SHDN}$ = GND | | | 15 | µA |
| VP Shutdown Supply Current | | $\overline{SHDN}$ = GND, measured at VP, $V_{VL}$ = 0 or 5V | | | 12 | µA |
| VL Output Voltage | | $I_{LOAD}$ = 0 to 25mA, $V_{VP}$ = 5V to 20V | 4.5 | | 4.75 | V |
| Reference Voltage | | $V_{VL}$ = 4.75V to 5.25V, no load | 1.98 | | 2.02 | V |
| Reference Load Regulation | | $I_{REF}$ = 0 to 50µA | | | 0.01 | V |
| REF Sink Current | | REF in regulation | 10 | | | µA |
| Output Undervoltage Threshold (Foldback) | | With respect to regulation point, no load | 60 | | 80 | % |
| Output Undervoltage Lockout Time (Foldback) | | From $\overline{SHDN}$ signal going high, $V_{OUT}$ < 0.6 x regulation point | 10 | | 42 | ms |
| Current-Limit Threshold | $V_{ILIM}$ | | -90 | | -110 | mV |

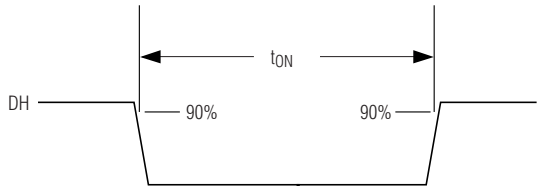
## ELECTRICAL CHARACTERISTICS (continued)

($V_{VP}$ = 15V, VL enabled, $C_{VL}$ = 1µF, $C_{REF}$ = 0.1µF, **$T_A$ = -40 to +85°C,** unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| VL Undervoltage Lockout Threshold | | Rising edge, hysteresis = 20mV, PWM disabled below this level | 4.1 | | 4.4 | V |
| $\overline{SHDN}$ Logic Input High Threshold Voltage | $V_{IH}$ | | 1.6 | | | V |
| $\overline{SHDN}$ Logic Input Low Threshold Voltage | $V_{IL}$ | | | | 0.6 | V |
| Dual Mode Threshold Voltage | | MAX1762 $V_{OUT}$ = 1.8V fixed | 50 | | 150 | mV |
| | | MAX1791 $V_{OUT}$ = 3.3V fixed | | | | |
| | | MAX1762 $V_{OUT}$ = 2.5V fixed | 2.5 | | 4 | V |
| | | MAX1791 $V_{OUT}$ = 5V fixed | | | | |

**Note 1:** Specifications to -40°C are guaranteed by design, not production tested.

**Note 2:** One-shot times are measured at the DH pin (VP = 15V, $C_{DH}$ = 400pF, 90% point to 90% point; see drawing below for measurement details).

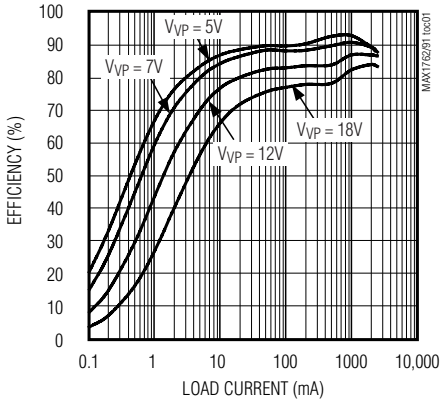


# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

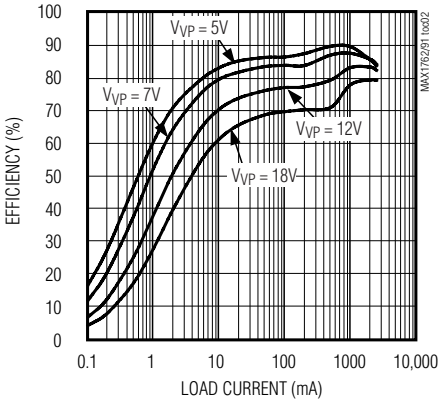
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

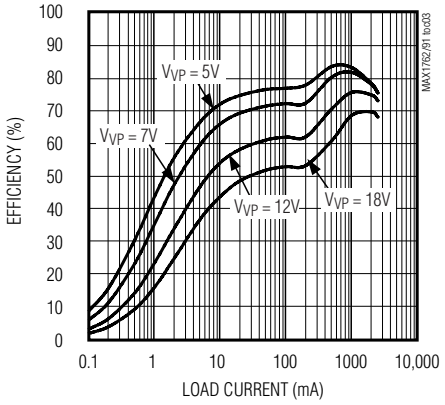
**MAX1762**
**EFFICIENCY vs. LOAD (2.5V)**



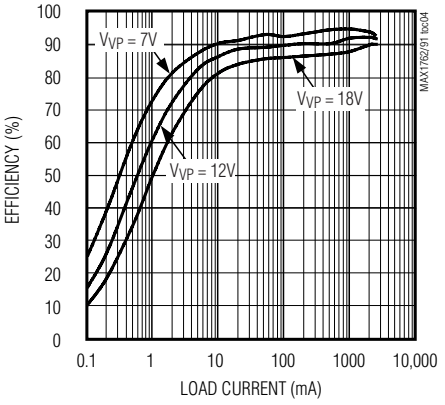

**MAX1762**
**EFFICIENCY vs. LOAD (1.8V)**



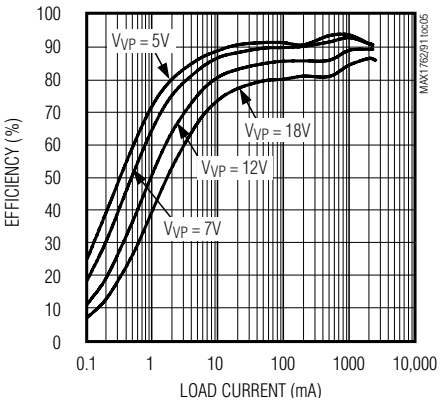

**MAX1762**
**EFFICIENCY vs. LOAD (1V)**



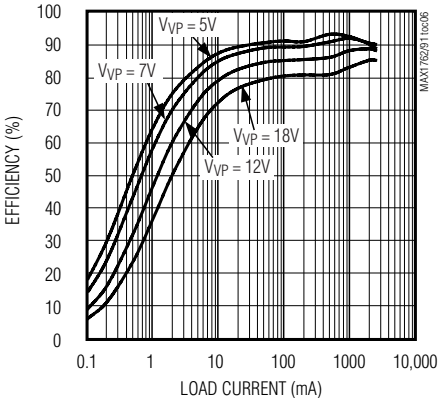

**MAX1791**
**EFFICIENCY vs. LOAD (5V)**



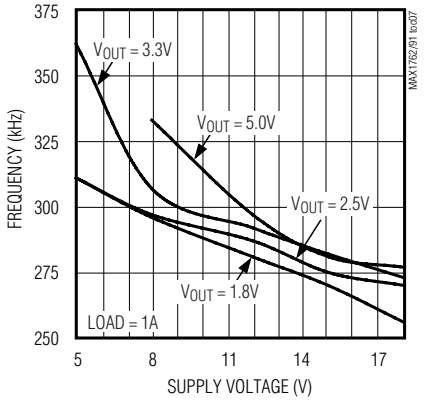

**MAX1791**
**EFFICIENCY vs. LOAD (3.3V)**



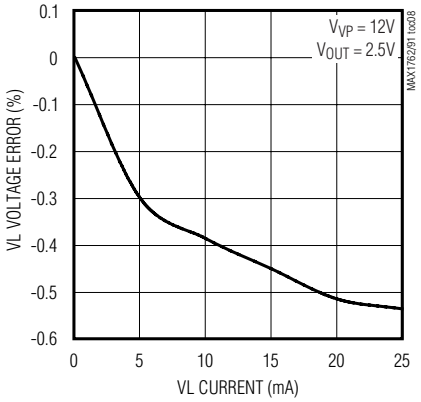

**MAX1791**
**EFFICIENCY vs. LOAD (3.0V)**




**FREQUENCY vs. SUPPLY VOLTAGE**



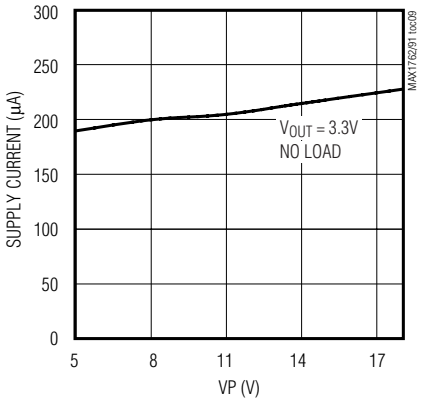

**VL VOLTAGE ERROR vs. OUTPUT CURRENT**



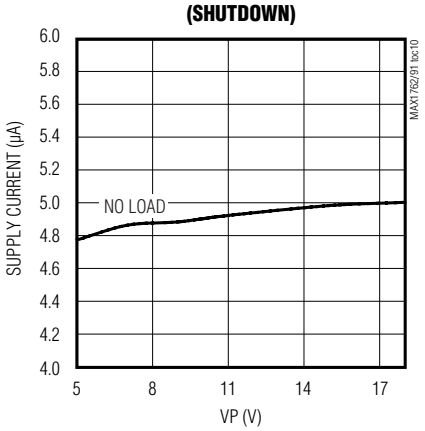
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

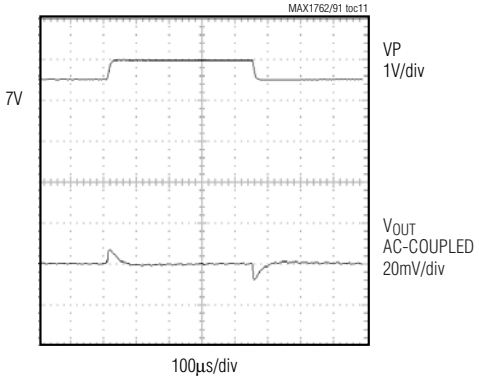
**SUPPLY CURRENT vs. INPUT VOLTAGE**




**SUPPLY CURRENT vs. INPUT VOLTAGE (SHUTDOWN)**

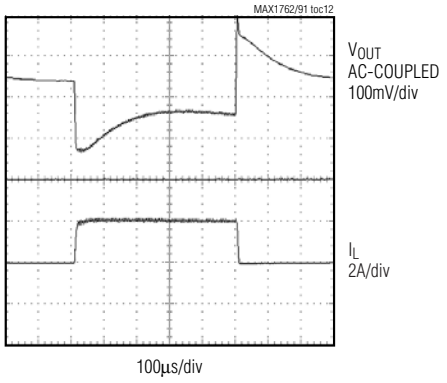



**LINE-TRANSIENT RESPONSE**



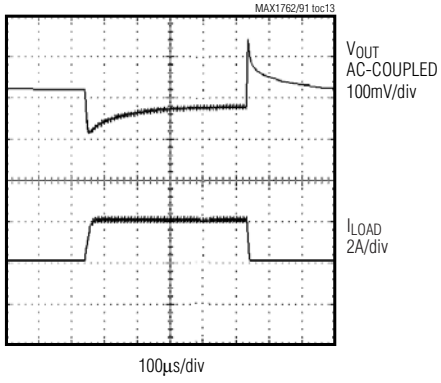

$V_{VP}$ = 7.5V TO 8V, $I_{LOAD}$ = 0, $V_{OUT}$ = 2.5V

**LOAD-TRANSIENT RESPONSE**



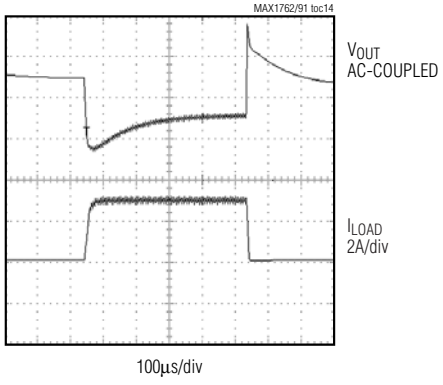

$V_{VP}$ = 12V, $I_L$ = 0 TO 2A, $V_{OUT}$ = 2.5V

**LOAD-TRANSIENT RESPONSE**



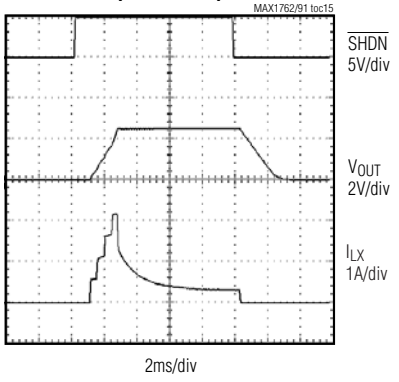

$V_{VP}$ = 12V, $I_{LOAD}$ = 0 TO 2A, $V_{OUT}$ = 1.8V

**OUTPUT OVERLOAD WAVEFORMS**



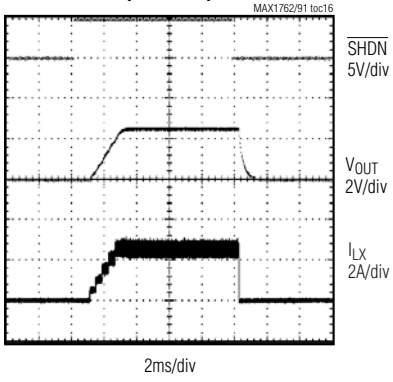

$V_{VP}$ = 12V, $I_{LOAD}$ = 0 TO 3A, $V_{OUT}$ = 2.5V

**SHUTDOWN AND STARTUP WAVEFORMS ($I_L$ = 300mA)**




$V_{VP}$ = 8V, $I_{LOAD}$ = 300mA, $V_{OUT}$ = 2.5V

**SHUTDOWN AND STARTUP WAVEFORMS ($I_L$ = 2.5A)**




$V_{VP}$ = 8V, $I_{LOAD}$ = 2.5A, $V_{OUT}$ = 2.5V

# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | VL | +4.65V Linear Regulator Output. Serves as the supply input for the DL gate driver and supplies up to 25mA to external loads. VL can be overdriven using an external 5V supply. Bypass VL to GND with at least a 1µF ceramic capacitor. |
| 2 | REF | 2V Reference Voltage Output. Bypass to GND with 0.1µF ceramic capacitor. REF can deliver up to 50µA for external loads. |
| 3 | FB | Feedback Input. Connect to an external resistive divider from OUT to GND in adjustable version. Regulates to 1.25V. FB also serves as Dual Mode select pin. Connect FB to GND for a fixed 1.8V (MAX1762) or 3.3V (MAX1791) output, or to VL for a fixed 2.5V (MAX1762) or 5.0V (MAX1791) output. |
| 4 | OUT | Output Voltage Connection. OUT is used for sensing the output voltage to determine the on-time and also serves as the feedback input in fixed-output modes. |
| 5 | $\overline{SHDN}$ | Shutdown Input. Connect to a voltage less than $V_{IL}$ (<0.6V) to shut down the device. Connect to a voltage greater than $V_{IH}$ (>1.6V) for normal operation. |
| 6 | GND | Analog and Power Ground |
| 7 | DL | Low-Side Gate Driver Output. DL swings between VL and GND. |
| 8 | CS | Current-Sense Connection. For lossless current sensing, connect CS to the junction of the MOSFETs and inductor. For more accurate current sensing, connect CS to a current-sense resistor from the source of the low-side switch to GND. |
| 9 | DH | High-Side Gate Driver Output. DH swings between VP and GND. |
| 10 | VP | Battery Voltage Supply Input. Used for PWM one-shot timing and as the input for the VL regulator and DH gate drivers. |

## Standard Application Circuit

The standard application circuit (Figure 1) generates a low-voltage output for general-purpose use in notebook computers (I/O supply, fixed CPU, core supply, and DRAM supply). This DC-DC converter steps down battery voltage from 5V to 20V with high efficiency and accuracy to a fixed voltage of 1.8V/2.5V/adj (MAX1762) or 3.3V/5.0V/adj (MAX1791). Both the MAX1762 and MAX1791 can be configured for adjustable output voltages ($V_{OUT}$ > 1.25V), using a resistive voltage-divider from $V_{OUT}$ to FB to adjust the output voltage (Figure 2). Similarly, Figure 3 shows an application circuit for $V_{OUT}$ < 1.25V, where a resistive voltage-divider from REF to FB is used to set the output voltage. Figure 4 shows how to set the regulator's current limit with an external sense resistor from CS to GND. Table 1 lists the components for each application circuit, and Table 2 contains contact information for the component manufacturers.

## Detailed Description

The MAX1762/MAX1791 step-down controllers are targeted at low-voltage chipsets and RAM power supplies for notebook and subnotebook computers, with additional applications in digital cameras, PDAs, and handy-terminals. Maxim's proprietary Quick-PWM pulse-width modulator (Figure 5) is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency (300kHz) over a wide range of input voltages (5V to 20V). The MAX1762 has fixed 1.8V or 2.5V outputs, while the MAX1791 has fixed 3.3V or 5.0V output voltages. Using an external resistive divider, $V_{OUT}$ can be set between 0.5V and 5.5V on either device. Quick-PWM architecture circumvents the poor load-transient response of fixed-frequency current-mode PWMs. This type of design avoids the problems commonly encountered with conventional constant-on-time and constant-off-time PWM schemes.

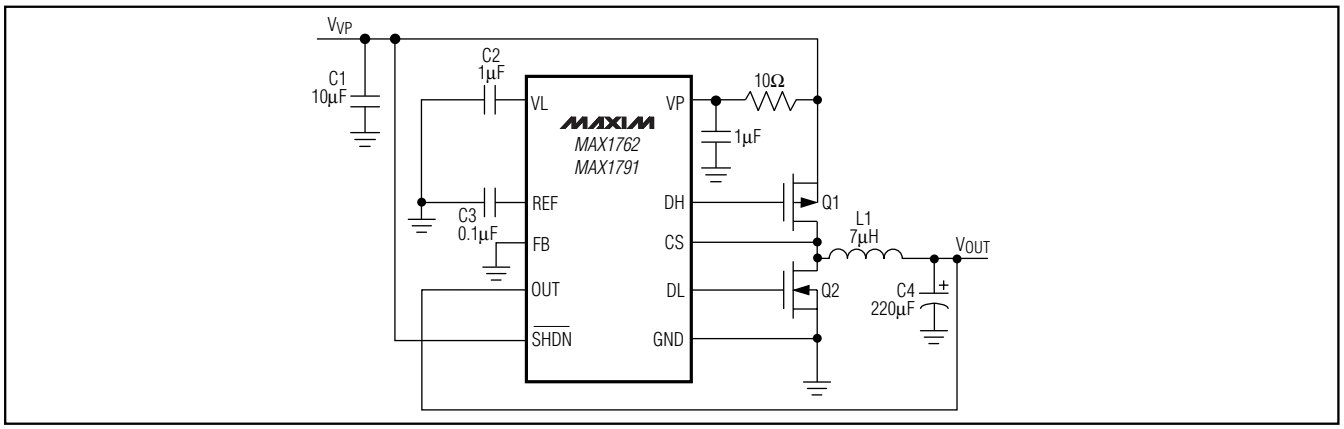



*Figure 1. Typical Application Circuit for Fixed Voltage*

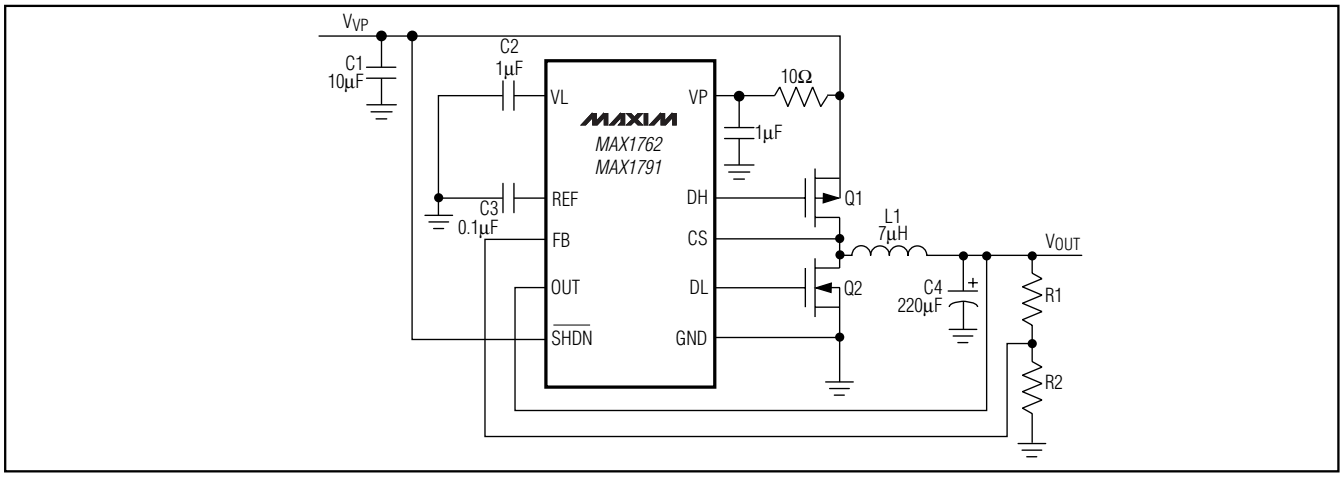



*Figure 2. Typical Application Circuit for Adjustable Output $V_{OUT}$ > 1.25V*

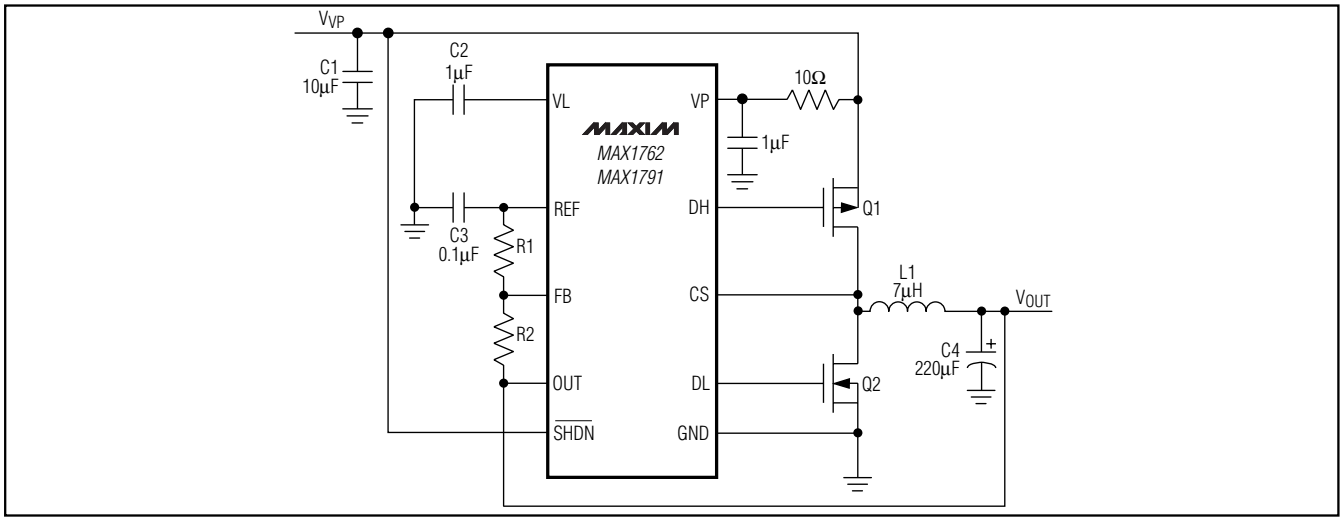



*Figure 3. Typical Application Circuit for $V_{OUT}$ < 1.25V*

# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

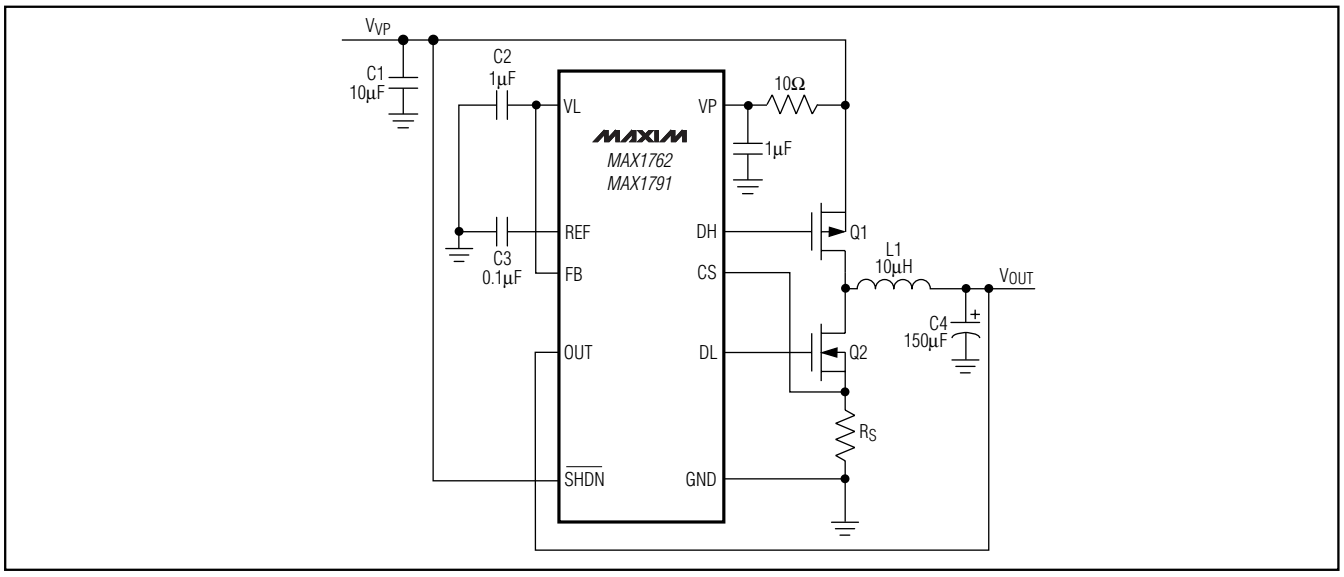



*Figure 4. Operation with External Current-Sense Resistor*

## Table 1. Component Selection for Standard Applications

| COMPONENT | 1.8V/2.5V/3.3V/5.0V AT 2A | 1V AT 2A |
|---|---|---|
| **Input Voltage Range** | **5V to 20V** | **5V to 20V** |
| **Inductor (µH)** | **7** | **5.2** |
| L1 Inductor | CDRH104-7R0NC<br>Sumida | CDRH104-5R2NC<br>Sumida |
| Q1 MOSFETS | NDS8958A<br>Fairchild | SI4539ADY<br>Fairchild |
| C1 Input Capacitor | TMK432BJ106KM<br>Taiyo Yuden | TMK432BJ106<br>Taiyo Yuden |
| C2 VL Cap | EMK3160J105KL<br>Taiyo Yuden | LMK316BJ475<br>Taiyo Yuden |
| C3 REF Cap | UMK316BI104KH<br>Taiyo Yuden | UMK316BI104KH<br>Taiyo Yuden |
| C4 Output Cap | 10TPB220M<br>Sanyo | 6TPB150M<br>Sanyo |

## Table 2. Component Manufacturers

| MANUFACTURER | | USA PHONE | WEBSITE INFO |
|---|---|---|---|
| Coiltronics | | 561-241-7876 | www.coiltronics.com |
| Fairchild Semiconductor | | 408-822-2181 | www.fairchildsemi.com |
| Sanyo | | 619-661-6835 | www.secc.co.jp |
| Sumida | USA | 847-956-0666 | www.sumida.com |
| | Japan | 81-3-3607-5111 | |
| Taiyo Yuden | | 408-573-4150 | www.t-yuden.com |

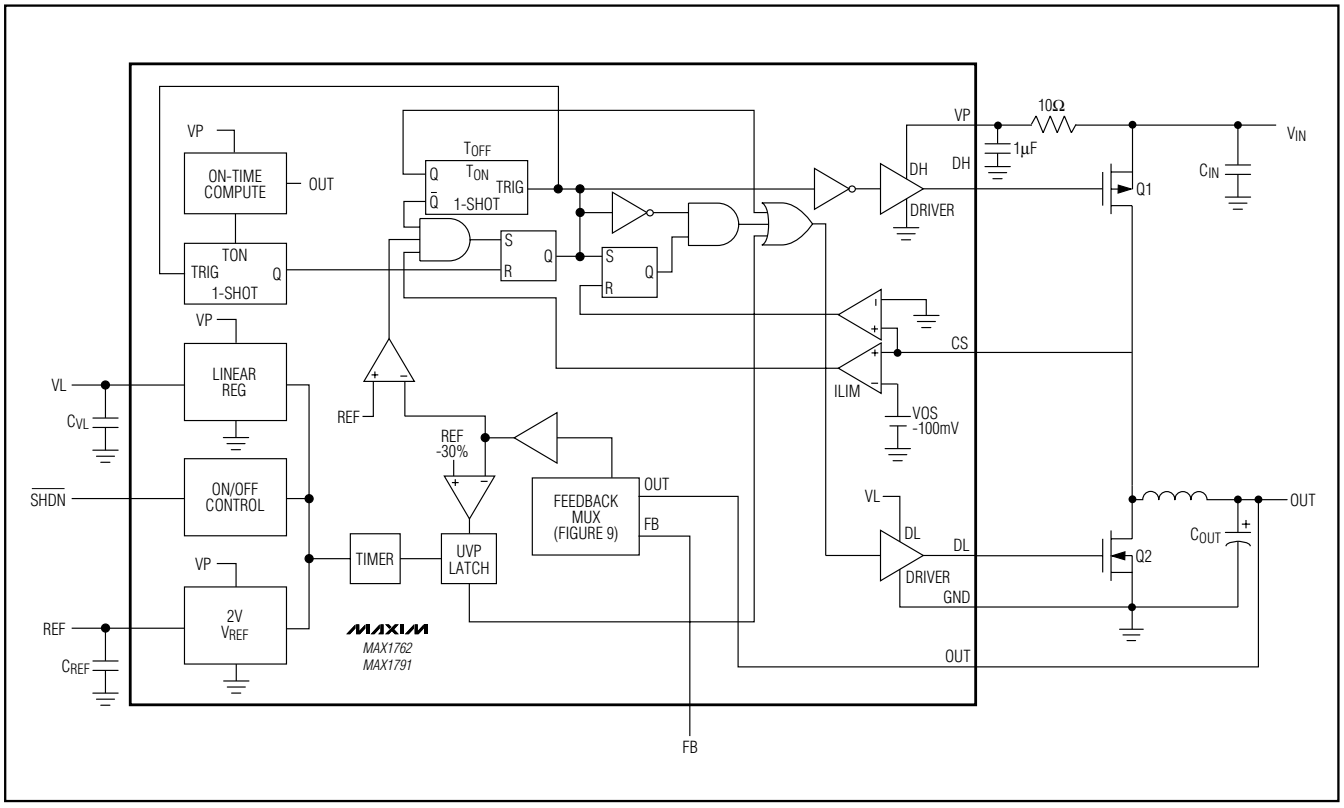



*Figure 5. Functional Diagram*

### VP Input and VL Logic Supply

An internal linear regulator supplied by VP produces the +4.65V supply (VL) that powers the PWM controller, logic, reference, and other blocks within the MAX1762/MAX1791. This +4.65V low-dropout linear regulator can supply up to 25mA for external loads. Bypass VL to GND with at least a 1µF ceramic capacitor. $V_{VP}$ can range between 5V and 20V. VL is turned off when the device is in shutdown and drops by approximately 500mV during a fault condition, such as when the output is short circuited to ground, and recovers when $\overline{SHDN}$ is cycled or power is reset. If VL is not driven externally, then $V_{VP}$ should be at least 5V to ensure operation. If $V_{VP}$ is running from a 5V (±10%) supply, $V_{VP}$ should be externally connected to VL.

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Overdriving the VL regulator with an external 5V supply also increases the MAX1762/MAX1791s' efficiency.

The MAX1762/MAX1791 include an input undervoltage lockout (UVLO) circuit that prevents the device from switching until VL > 4.4V (max). UVLO ensures there is a sufficient drive for the external MOSFETs, prevents the high-side MOSFET from being turned on for near 100% duty cycle, and keeps the output in regulation.

### Voltage Reference (REF)

The 2V reference (REF) is accurate to ±1% over temperature, making REF useful as a precision system reference. Bypass REF to GND with a 0.1µF (min) ceramic capacitor. REF can supply up to 50µA for external loads. However, if tight-accuracy specs for either $V_{OUT}$ or REF are essential, avoid loading REF. Loading slightly reduces the main output voltage by an amount that tracks the reference-voltage load regulation error.

### Free-Running Constant On-Time PWM Controller with Input Feed-Forward

The PWM control architecture is a quasi-fixed-frequency constant on-time current-mode type with voltage feed-forward. This architecture relies on the output ripple voltage to provide the PWM ramp signal; thus, the output filter capacitor's ESR acts as a feedback resistor. The control algorithm is very simple. The high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. There is another one-shot that sets a minimum amount of off-time (500ns max). The on-time one-shot triggers when all of the following conditions are met: the error comparator is low, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

### On-Time One-Shot

The on-time of the one-shot is inversely proportional to the battery voltage as measured by the VP input, and directly proportional to the output voltage sensed at OUT:

$$t_{ON} = K \times \frac{(V_{OUT} + 0.075V)}{V_{BATT}}$$

where K is internally fixed at 3.349µs, and 0.075V is a factor that accounts for the expected drop across the synchronous switch. This arrangement maintains a switching frequency that is nearly constant as $V_{BATT}$, $I_{LOAD}$, and $V_{OUT}$ are changed. Table 3 shows the operating frequency range for the MAX1762/MAX1791.

Note that the output voltage adjust range for continuous-conduction operation is restricted by the non-adjustable 0.5µs (max) minimum off-time. Worst-case dropout performance is determined by the minimum on-time spec. The worst-case duty factor limit is:

$$\frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}} = \frac{2.55\mu s}{2.55\mu s + 0.5\mu s} = 84\%$$

with $V_{BATT}$ = 6V and $V_{OUT}$ = 5V. Therefore, with IR voltage drops in the loop included, the minimum input voltage to achieve $V_{OUT}$ = 5V is about 6.1V, using the step-down transfer function equation for duty cycle (DC = $V_{OUT}/V_{IN}$). Typical units exhibit better performance. Note that transient response is somewhat degraded near dropout, and the circuit may need additional bulk output capacitance to support fast load changes.

### Automatic Pulse-Skipping Switchover

This PWM control algorithm automatically switches over to pulse-skipping operation at light loads. The MAX1762/MAX1791 truncates the low-side switch's on-time when the inductor current drops to zero. The load current level at which pulse-skipping/PWM crossover occurs is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 6):

$$I_{LOAD(SKIP)} = \frac{K \times V_{OUT}}{2L}\left(\frac{V_{VP} - V_{OUT}}{V_{VP}}\right)$$

The inductor current is never allowed to go negative. If the output voltage is above its regulation point and the inductor current reaches zero, the low-side driver is switched off. Once the output voltage falls below its regulation point, the high-side driver is switched on. This causes a dead time in between when the high-side and low-side drivers are on, skipping pulses and resulting in the switching frequency slowing at light loads, thereby improving efficiency.

### MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-size power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment where a large $V_{BATT}$ - $V_{OUT}$ differential exists. The high-side driver (DH) is rated for 0.6A source/sink capability and swings from VP to GND. The low-side driver (DL) is

**Table 3. Operating Frequency**

| DEVICE | K (µs) | MIN (kHz) | TYP (kHz) | MAX (kHz) |
|---|---|---|---|---|
| MAX1762/MAX1791 | 3.349 | 268.7 | 298.5 | 328 |

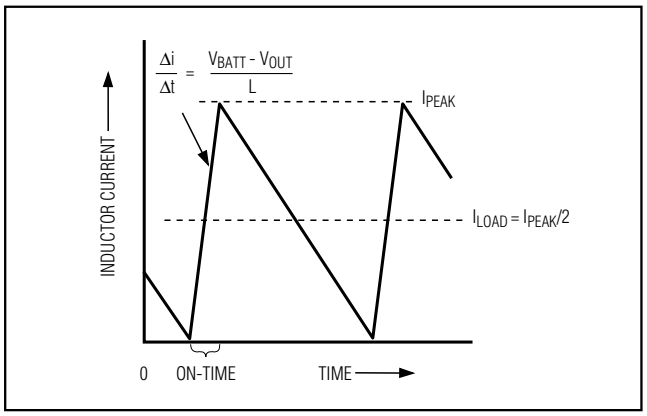


*Figure 6. Pulse-Skipping/Discontinuous Crossover Point*

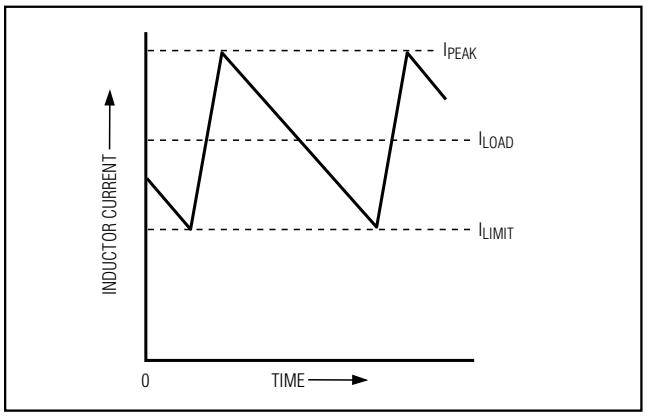


*Figure 7. "Valley" Current-Limit Threshold Point*

rated for +0.5A, -0.9A source/sink capability and swings from VL to GND.

The internal pulldown transistor that drives DL low is robust, with a 1Ω typical on-resistance. This helps prevent DL from being pulled up during the fast rise time of the inductor node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, some combinations of high-and low-side FETS may cause excessive gate-drain coupling, which can lead to poor efficiency, EMI, and shoot-through currents.

An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully turned off. The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay.

### Low-Side Current-Limit Sensing (ILIM)

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-state resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is below the current-limit threshold (-100mV from CS to GND), the PWM is not allowed to initiate a new cycle (Figure 7). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and battery voltage.

If greater current-limit accuracy is desired, CS must be connected to the junction of the low-side switch source and a current-sense resistor to GND. The current limit will be 0.1V/$R_{SENSE}$, and the accuracy will be ±10%.

A resistive voltage-divider from the inductor's switching mode to ground can be used to adjust the current-limit sense voltage that appears at CS (Figure 8). Keep the impedance at this mode low to avoid errors at CS.

### POR and Soft-Start

Power-on reset (POR) occurs when $V_{BATT}$ rises above approximately 2V, resetting the fault latch and soft-start counter and preparing the PWM for operation. UVLO circuitry inhibits switching until $V_{VP}$ rises above 4.1V, whereupon an internal digital soft-start timer begins to ramp up the maximum allowed current limit. The ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%; 100% current is available after approximately 1.7ms.

### Output Undervoltage Protection

The output UVLO function is similar to foldback current limiting but employs a timer rather than a variable current limit. The output undervoltage protection is enabled 20ms after POR or when coming out of shutdown. If the output is under 70% of the nominal value,

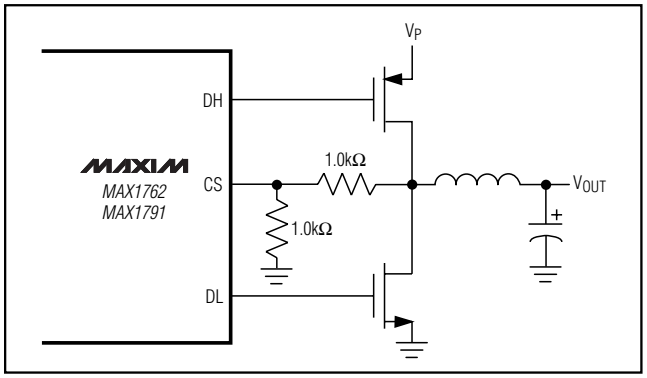


*Figure 8. Using a Resistive Voltage-Divider to Adjust Current-Limit Sense Voltage to 200mV*

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then the PWM is latched off and does not restart until VP power is cycled, or $\overline{SHDN}$ is toggled low then high.

## Design Procedure

Begin by establishing the input voltage range and maximum load current before choosing an inductor and its associated ripple-current ratio (LIR). The following four factors dictate the rest of the design:

1) **Input voltage range.** The maximum value ($V_{VP(MAX)}$) must accommodate the maximum AC adapter voltage. The minimum value ($V_{VP(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
2) **Maximum load current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stress and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current ($I_{LOAD}$) determines the thermal stress and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit, $I_{LOAD} = I_{LOAD(MAX)} \times 0.8$.
3) **Switching frequency.** The MAX1762/MAX1791 have a nominal switching frequency of 300kHz.
4) **Inductor ripple-current ratio (LIR).** LIR is the ratio of the peak-to-peak ripple current to the average inductor current. Size and efficiency trade-offs must be considered when setting the inductor ripple-current ratio. Low inductor values cause large ripple currents, resulting in the smallest size but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at critical conduction (where the inductor current just touches zero with every cycle). Inductor values lower than this grant no further size-reduction benefit.

The MAX1762/MAX1791s' pulse-skipping algorithm initiates skip mode at the critical conduction point. So, the inductor operating point also determines the load-current value at which switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

The inductor ripple current also impacts transient-response performance, especially at low $V_{VP} - V_{OUT}$ difference. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient ($V_{SAG}$) is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L \left( K \frac{V_{OUT}}{V_{VP}} + t_{OFF(MIN)} \right)}{2 \times C_{OUT} \times V_{OUT} \left[ K \left( \frac{V_{VP} - V_{OUT}}{V_{VP}} \right) - t_{OFF(MIN)} \right]}$$

where minimum off-time = 0.5µs (max).

### Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{VP} - V_{OUT})}{V_{VP} \times f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 2A, $V_{VP}$ = 7V, $V_{OUT}$ = 1.6V, f = 300kHz, 35% ripple current or LIR = 0.35:

$$L = \frac{1.6V(7V - 1.6V)}{7 \times 300kHz \times 0.35 \times 2A} = 5.9\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. The core must be large enough not to saturate at the peak inductor current ($I_{PEAK}$):

$$I_{PEAK} = I_{LOAD(MAX)} + [(LIR/2) \times I_{LOAD(MAX)}]$$

### Determining Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current; therefore:

$$I_{VALLEY} > I_{LOAD(MAX)} - [(LIR/2) \times I_{LOAD(MAX)}]$$

where $I_{VALLEY}$ = minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of Q2. For the MAX1762/MAX1791, the minimum current-limit threshold is 90mV. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

Examining the 2A circuit example with a maximum $R_{DS(ON)}$ = 52mΩ at +85°C temperature reveals the following:

$$I_{VALLEY} = 90mV / 52m\Omega = 1.73A$$

Checking the corresponding $I_{LOAD(MAX)}$ reveals:

$$I_{LOAD(MAX)} = \frac{I_{VALLEY}}{1 - 0.5\ LIR} = \frac{1.73A}{1 - 0.5 \times 0.35} = 2.1A$$

A current-sense resistor can be connected from CS to GND to set the current limit for the device. The MAX1762/MAX1791 use the sense resistor instead of the $R_{DS(ON)}$ of Q2 to limit the current. The maximum value of the sense resistor can be calculated with the equation:

$$I_{LIMIT} = 90mV / R_{SENSE}$$

### Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. In CPU $V_{CORE}$ converters and other applications where the output is subject to large load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{DIP}}{f I_{LOAD(MAX)}}$$

where $V_{DIP}$ is the maximum tolerable transient voltage drop. In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \le \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}}$$

where $V_{P-P}$ is the peak-to-peak output voltage ripple. The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalum, SP, POS, and other electrolytic-type capacitors).

When using low-capacity filter capacitors such as ceramics, capacitor size is usually determined by the capacity needed to prevent $V_{SAG}$ and $V_{SOAR}$ from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the $V_{SAG}$ equation in the *Design Procedure* section).

The amount of overshoot due to stored inductor energy can be calculated as:

$$\Delta V \le \frac{L I_{PEAK}^2}{2 C V_{OUT}}$$

where $I_{PEAK}$ is the peak inductor current.

### Stability Considerations

Stability is determined by the value of the ESR zero ($f_{ESR}$) relative to the switching frequency (f). The point of instability is given by the following equation:

$$f_{ESR} \le \frac{f}{\pi}$$

where:

$$f_{ESR} \le \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors in widespread use at the time of publication have typical ESR zero frequencies of 20kHz. In the design example used for inductor selection, the ESR needed to support a specified ripple voltage is found by the equation:

$$R_{ESR} = \frac{V_{RIPPLE(p-p)}}{f LIR \times I_{LOAD}}$$

where LIR is the inductor ripple current ratio, and $I_{LOAD}$ is the average DC load. Using a LIR = 0.35 and an average load current of 2A, the ESR needed to support 50m$V_{P-P}$ ripple is 71mΩ.

Do not use high-value ceramic capacitors directly across the fast feedback inputs (FB to GND) without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the junction of the inductor and FB pin.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This

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"fools" the error comparator into triggering a new cycle immediately after the 500ns minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillations at the output after line or load perturbations that can cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient (refer to the MAX1762/MAX1791 EV kit manual) and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or overshoot.

### Input Capacitor Selection

The input capacitor must meet the ripple-current requirement ($I_{RMS}$) imposed by the switching currents. Nontantalum chemistries (ceramic or OS-CON™) are preferred due to their resilience to power-up surge currents:

$$I_{RMS} = I_{LOAD} \times \left( \frac{\sqrt{V_{OUT}(V_{VP} - V_{OUT})}}{V_{VP}} \right)$$

### Power MOSFET Selection

DC bias and output power considerations dominate the selection of the power MOSFETs used with the MAX1762/MAX1791. Take care not to exceed the device's maximum voltage ratings. In general, both switches are exposed to the supply voltage, so select MOSFETs with $V_{DS}$ (max) greater than VP (max). Gate drives to the n-channel and p-channel MOSFETs are not symmetrical. The n-channel device is driven from ground to the logic supply VL, while the p-channel device is driven from VP to ground. The maximum rating for $V_{GS}$ for the n-channel device is usually not an issue; however, $V_{GS}$ (max) for the p-channel must be at least VP (max). Since $V_{GS}$ (max) is usually lower than $V_{DS}$ (max), gate drive constraints often dictate the required p-channel breakdown rating.

For moderate input-to-output differentials, the high-side MOSFET (Q1) can be sized smaller than the low-side MOSFET (Q2) without compromising efficiency. The high-side switch operates at a very low duty cycle under these conditions, so most conduction losses occur in Q2. For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses ($I^2R$ x duty cycle) equal to the switching losses ($CV_{VP}^2f$). Make sure that the conduction losses at the minimum input voltage do not exceed the package thermal limits or violate the overall thermal budget. Conduction losses plus switching losses at the maximum input voltage should not exceed the package ratings or violate the overall thermal budget (see *MOSFET Power Dissipation*).

In addition to efficiency considerations, the selection of the $R_{DS(ON)}$ of the low-side MOSFET must account for the regulator's required current limit. Choose a MOSFET that has a low enough resistance over the operating temperature range such that the device does not enter current limit during normal operation (see the *Determining Current Limit* section). Conversely, ultra-low $R_{DS(ON)}$ devices may set the current limit too high and may result in only incremental improvements in efficiency. Some large n-channel FETs also have substantial interelectrode capacitance. Verify that the MAX1762/ MAX1791 DL driver can hold the gate off when the high side switch turns on. Cross-conduction problems can occur when the high-side switch turns on due to coupling through the n-channel's parasitic drain-to-gate capacitance.

The MAX1762/MAX1791 have adaptive dead-time circuitry that prevents the high-side and low-side MOSFETs from conducting at the same time (see *MOSFET Gate Drivers*). Even with this protection, it is still possible for delays internal to the MOSFET to prevent one MOSFET from turning off while the other is turned on. The maximum mismatch time that can be tolerated is 60ns. Select devices that have low turn-off times, and make sure that NFET($t_D$(off,max)) - PFET($t_D$(on,min)) < 60ns, and PFET($t_D$(off,max)) - NFET($t_D$(on,min)) < 60ns. Failure to do so may result in efficiency-killing shoot-through currents.

### MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation (PD) due to resistance occurs at minimum battery voltage:

$$PD(Q1\ resistance) = \left( \frac{V_{OUT}}{V_{VP(MIN)}} \right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltage. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-

*OS-CON is a trademark of Sanyo.*

side switching losses do not usually become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum battery voltage is applied, due to the squared term in the $CV^2f$ switching loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{VP(MAX)}$, reconsider your choice of high-side MOSFET.

Calculating the power dissipation in Q1 due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a verification using a thermocouple mounted on Q1:

$$PD\ (Q1\ switching) = \left( \frac{C_{RSS} \times V_{VP(MAX)}^2 \times f \times I_{LOAD}}{I_{GATE}} \right)$$

where $C_{RSS}$ is the reverse transfer capacitance of Q1, and $I_{GATE}$ is the peak gate-drive source/sink current.

For the low-side MOSFET, the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(Q2) = \left( 1 - \frac{V_{OUT}}{V_{VP(MAX)}} \right) \times I_{LOAD}^2 \times R_{DS}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, the circuit must be overdesigned to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + (LIR / 2) \times I_{LOAD(MAX)}$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. This means that the MOSFET must be very well heatsinked. If short-circuit protection without overload protection is enough, a normal $I_{LOAD}$ value can be used for calculating component stresses.

During the period when the high-side switch is off, current circulates from ground to the junction of both FETs and the inductor. As a consequence, the polarity of the switching node is negative with respect to ground. If unchanged, this voltage is approximately 0.7V (a diode drop) at both transition edges while both switches are off. In between the edges, the low-side switch conducts; the drop is $I_L \times R_{DS(ON)}$. If a Schottky clamp is connected across the low-side switch, the initial and final voltage drops is reduced, improving efficiency slightly.

Choose a Schottky diode (D1) having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional and can be removed if efficiency isn't critical.

## Applications Issues

### Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the $t_{ON}$ K-factor. Also, keep in mind that transient response performance of buck regulators operating close to dropout is poor, and bulk output capacitance must often be added.

Dropout design example: $V_{IN}$ = 7V (min), $V_{OUT}$ = 5V, f = 300kHz. The required duty cycle is :

$$DC_{REQ} = \frac{V_{OUT} + V_{SW}}{V_{VP} - V_{SW}} = \frac{5V + 0.1V}{7V - 0.1V} = 0.74$$

The worst-case on-time is:

$$t_{ON(MIN)} = \frac{V_{OUT} + 0.075}{V_{VP}} \times K = \frac{5V + 0.075}{7V} \times 3.35\mu s \times 90\% = 2.18\mu s$$

The maximum IC duty factor based on timing constraints of the MAX1762/MAX1792 is:

$$Duty = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}} = \frac{2.18\mu s}{2.18\mu s + 0.5\mu s} = 0.82,$$

which meets the required duty cycle. Remember to include inductor resistance and MOSFET on-state voltage drops ($V_{SW}$) when doing worst-case dropout duty-factor calculations.

### Fixed Output Voltages

The MAX1762/MAX1791 Dual Mode operation allows the selection of common voltages without requiring external components (Figure 9). Connect FB to GND for

# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

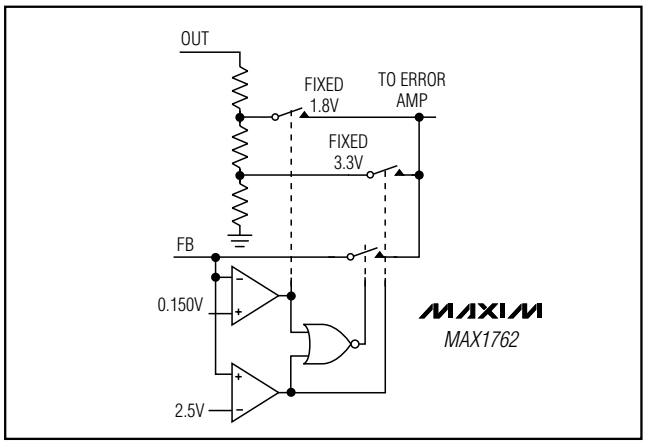



*Figure 9. Feedback MUX*

a fixed +1.8V (MAX1762) or 3.3V (MAX1791) output. Connect FB to VL for a fixed 2.5V (MAX1762) or 5.0V (MAX1791) output. Otherwise, connect FB to a resistive voltage-divider for an adjustable output.

### Setting the Output Voltage

Select $V_{OUT}$ > 1.25V for the MAX1762/MAX1791 by connecting FB to a resistive voltage-divider between $V_{OUT}$ and GND (Figure 2). Choose R2 to be about 10kΩ, and solve for R1 using the equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

where $V_{FB}$ = 1.25V. For a $V_{OUT}$ = 3.0V, R2 = 10kΩ and R1 = 14kΩ.

For a desired $V_{OUT}$ < 1.25V, connect FB to a resistive voltage-divider between REF and OUT (Figure 3). Choose R1 to be about 50kΩ, and solve for R2 using the equation:

$$R2 = \left[\frac{V_{OUT} - V_{FB}}{V_{FB} - V_{REF}}\right] \times R1$$

where $V_{FB}$ = 1.25V and $V_{REF}$ = 2.0V. For a $V_{OUT}$ = 1.0V, R1 = 50kΩ and R2 = 16.5kΩ. Under these conditions, a minimum load of $V_{REF}$ - $V_{FB}$ / R1 >15µA is required.

### PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. This is especially true when multiple converters are on the same PC board where one circuit can affect the other. The switching power stages require particular attention (Figure 10). Refer to the MAX1791 EV kit manual for a specific layout example.

If possible, mount all of the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Isolate the power components on the top side from the sensitive analog components on the bottom side with a ground shield. Use a separate GND plane under OUT. Avoid the introduction of AC currents into the GND ground planes. Run the power plane ground currents on the top side only, if possible.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Inductor and GND connections to the synchronous rectifiers for current limiting must be made using Kelvin sensed connections to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting GND and CS inside (underneath) the µMAX package.
- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Ensure that the OUT connection to $C_{OUT}$ is short and direct. However, in some cases it may be desirable to deliberately introduce some trace length between the OUT connector node and the output filter capacitor (see *Stability Considerations*).
- Route high-speed switching nodes (CS, DH, and DL) away from sensitive analog areas (FB). Use GND as an EMI shield to keep radiated switching noise away from the IC's feedback divider and analog bypass capacitors.

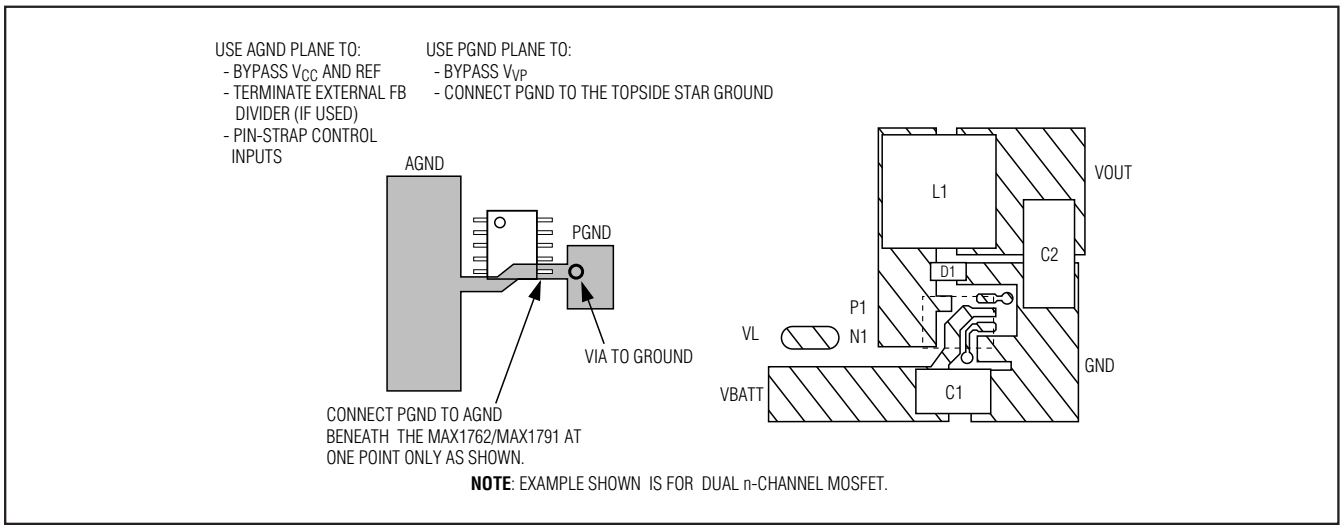



*Figure 10. PC Board Layout Example*

### Layout Procedure

1) Place the power components first, with ground terminals adjacent (Q1 source, $C_{IN}$, $C_{OUT}$). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the synchronous-rectifier MOSFETs, preferably on the back side in order to keep CS, GND, and the DL gate drive lines short and wide. The DL gate trace must be short and wide (measuring 50mils to 100mils wide if the MOSFET is 1in from the controller IC).
3) Place the $V_L$ bypass capacitor near the controller IC.
4) Make the DC-DC controller ground connections as follows: Near the IC, create a small analog ground plane. Connect this plane to GND, and use this plane for the ground connection for the REF and $V_{VP}$ bypass capacitors and FB dividers.
5) On the board's top side (power planes), make a star ground to minimize crosstalk between the two sides. The top-side star ground is a star connection of the input capacitors, side 1 low-side MOSFET. Keep the resistance low between the star ground and the source of the low-side MOSFETs for accurate current limit. Connect the top-side star ground (used for MOSFET, input, and output capacitors) to the small island with a single short, wide connection (preferably just a via).
6) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias.

### Chip Information

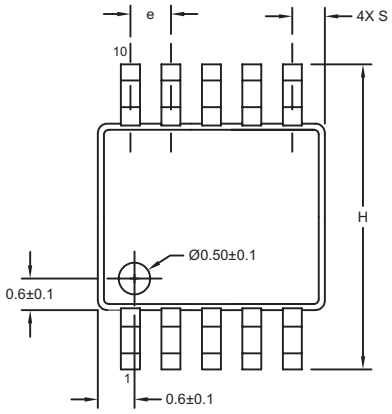
TRANSISTOR COUNT: 3520

PROCESS: S8E1FP

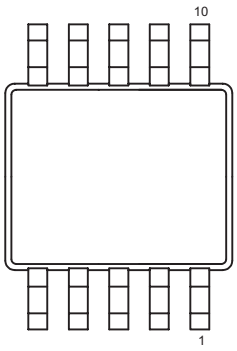
# High-Efficiency, 10-Pin µMAX, Step-Down Controllers for Notebooks

## Package Information

10LUMAX.EPS

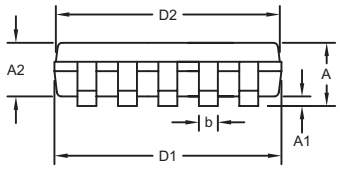



TOP VIEW

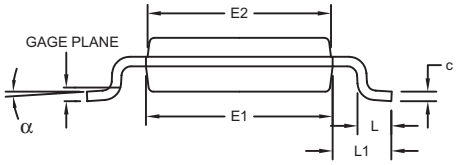



BOTTOM VIEW

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | - | 0.043 | - | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.030 | 0.037 | 0.75 | 0.95 |
| D1 | 0.116 | 0.120 | 2.95 | 3.05 |
| D2 | 0.114 | 0.118 | 2.89 | 3.00 |
| E1 | 0.116 | 0.120 | 2.95 | 3.05 |
| E2 | 0.114 | 0.118 | 2.89 | 3.00 |
| H | 0.187 | 0.199 | 4.75 | 5.05 |
| L | 0.0157 | 0.0275 | 0.40 | 0.70 |
| L1 | 0.037 REF | | 0.940 REF | |
| b | 0.007 | 0.0106 | 0.177 | 0.270 |
| e | 0.0197 BSC | | 0.500 BSC | |
| c | 0.0035 | 0.0078 | 0.090 | 0.200 |
| S | 0.0196 REF | | 0.498 REF | |
| α | 0° | 6° | 0° | 6° |




FRONT VIEW




SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0061 | I | 1/1 |

# Mouser Electronics

Authorized Distributor

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