27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Serializer

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to _GND..-0.5V to +4.0V
Any Ground to Any Ground...................................-0.5V to +0.5V
OUT+, OUT-, CMF to LVDSGND...........................-0.5V to +4.0V
OUT+, OUT- Short Circuit to LVDSGND
or V_{CCLVDS}..Continuous
OUT+, OUT- Short Through 0.125µF (or smaller),
25V Series Capacitor..-0.5V to +16V
RGB_IN[17:0], CNTL_IN[8:0], DE_IN,
RNG0, RNG1, PRE, PCLK_IN,
$\overline{PWRDWN}$ to GND ....-0.5V to (V_{CCIN} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
48-Lead LQFP (derate 20.8mW/°C above +70°C)....1666.7mW
ESD Protection
Machine Model (R_D = 0Ω, C_S = 200pF)
All Pins to GND ....±200V
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND ....±3kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge (OUT+, OUT-) to LVDSGND ....±10kV
Air-Gap Discharge (OUT+, OUT-) to LVDSGND ....±30kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge (OUT+, OUT-) to LVDSGND ....±10kV
Air-Gap Discharge (OUT+, OUT-) to LVDSGND ....±15kV
Storage Temperature Range ....-65°C to +150°C
Junction Temperature..+150°C
Lead Temperature (soldering, 10s)..................................+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, PRE = low, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (RGB_IN[17:0], CNTL_IN[8:0], DE_IN, PCLK_IN, $\overline{PWRDWN}$, RNG_, PRE)							
High-Level Input Voltage	V_{IH}	V_{CCIN} = 1.71V to < 3V (Note 3)		0.65 x V_{CCIN}		V_{CCIN} + 0.3	V
		V_{CCIN} = 3.0V to 3.6V		2		0.3 + V_{CCIN}	
Low-Level Input Voltage	V_{IL}	V_{CCIN} = 1.71V to < 3V (Note 3)		-0.3		0.3 x V_{CCIN}	V
		V_{CCIN} = 3.0V to 3.6V		-0.3		+0.8	
Input Current	I_{IN}	V_{CCIN} = 1.71V to 3.6V, $\overline{PWRDWN}$ = high or low	V_{IN} = -0.3V to 0V (MAX9247ECM), V_{IN} = -0.15V to 0V (MAX9247GCM)	-100		+20	µA
			V_{IN} = 0V to (V_{CCIN} + 0.3V)	-20		+20	
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
LVDS OUTPUTS (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Figure 1		250	335	450	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 1				20	mV
Common-Mode Voltage	V_{OS}	Figure 1		1.125	1.29	1.475	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 1				20	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V or 3.6V		-15	±8	+15	mA
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			5.5	15	mA
Output High-Impedance Current	I_{OZ}	$\overline{PWRDWN}$ = low or $V_{CC\_}$ = 0V	V_{OUT+} = 0V, V_{OUT-} = 3.6V	-1		+1	µA
			V_{OUT+} = 3.6V, V_{OUT-} = 0V				

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PWRDWN}$ = high, PRE = low, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Differential Output Resistance	R_O				78	110	147	Ω
Worst-Case Supply Current	I_{CCW}	R_L = 100Ω ±1%, C_L = 5pF, continuous 10 transition words	2.5MHz	PRE = 0		15	25	mA
				PRE = 1			27	
			5MHz	PRE = 0		18	25	
				PRE = 1			27	
			10MHz	PRE = 0		23	28	
				PRE = 1			30	
			20MHz	PRE = 0		33	39	
				PRE = 1			42	
			35MHz	PRE = 0		50	65	
				PRE = 1			69	
			42MHz	PRE = 0		60	70	
				PRE = 1			75	
Power-Down Supply Current	I_{CCZ}	(Note 4)					50	µA

AC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω ±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, PRE = low, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PCLK_IN TIMING REQUIREMENTS							
Clock Period	t_T	Figure 2	MAX9247ECM	23.8		400.0	ns
			MAX9247GCM	28.6		400.0	
Clock Frequency	f_{CLK}	MAX9247ECM		2.5		42.0	MHz
		MAX9247GCM		2.5		35.0	
Clock Frequency Difference from Deserializer Reference Clock	Δf_{CLK}			-2		+2	%
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T, Figure 2		35	50	65	%
Clock Transition Time	t_R, t_F	Figure 2				2.5	ns
SWITCHING CHARACTERISTICS							
Output Rise Time	t_{RISE}	20% to 80%, V_{OD} ≥ 250mV, Figure 3	PRE = low		280	370	ps
			PRE = high		240	320	
Output Fall Time	t_{FALL}	80% to 20%, V_{OD} ≥ 250mV, Figure 3	PRE = low		280	370	ps
			PRE = high		240	320	
Input Setup Time	t_{SET}	Figure 4		3			ns
Input Hold Time	t_{HOLD}	Figure 4		3			ns

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 100Ω±1%, C_L = 5pF, $\overline{PWRDWN}$ = high, PRE = low, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serializer Delay	t_{SD}	Figure 5	3.10 x t_T + 2.0		3.10 x t_T + 8.0	ns
PLL Lock Time	t_{LOCK}	Figure 6			17,100 x t_T	ns
Power-Down Delay	t_{PD}	Figure 7			1	µs
Peak-to-Peak Output Jitter	t_{JITT}	Measured with PRBS input pattern at 840Mbps data rate			150	ps
Peak-to-Peak Output Offset Voltage	$V_{OS(P-P)}$	840Mbps data rate, CMF open, Figure 8		22	70	mV
		840Mbps data rate, CMF 0.1µF to ground, Figure 8		12	50	

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground, except V_{OD}, ΔV_{OD}, and ΔV_{OS}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

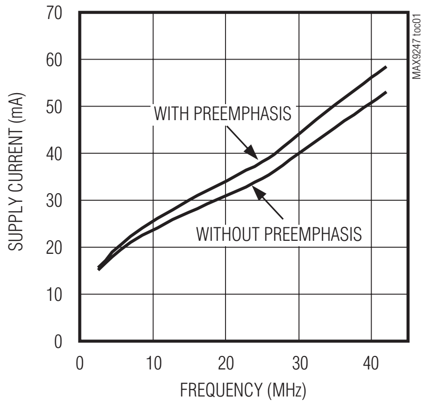
Note 3: Parameters are guaranteed by design and characterization and are not production tested. Limits are set at ±6 sigma.

Note 4: All LVTTL/LVCMOS inputs, except $\overline{PWRDWN}$ at ≤ 0.3V or ≥ V_{CCIN} - 0.3V. $\overline{PWRDWN}$ is ≤ 0.3V.

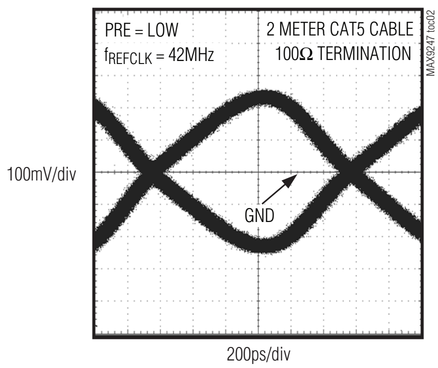
Typical Operating Characteristics

($V_{CC\_}$ = +3.3V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

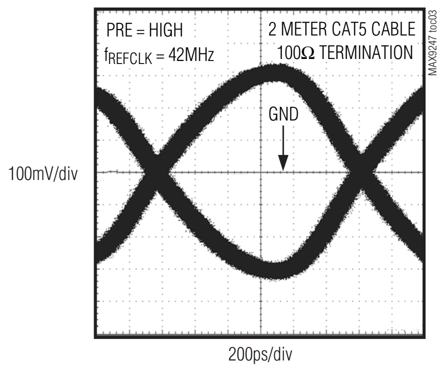
WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY



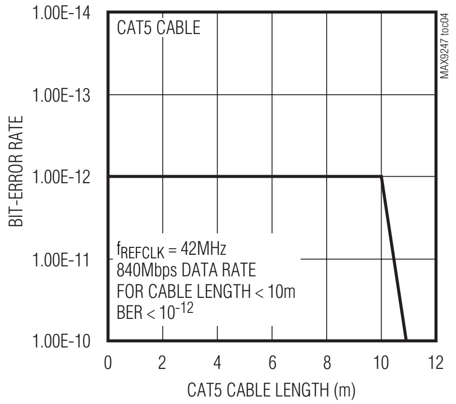
EYE DIAGRAM WITHOUT PREEMPHASIS



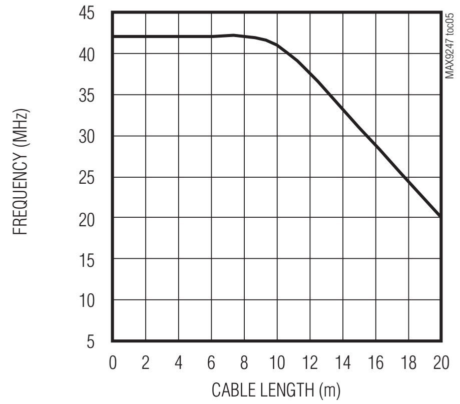
EYE DIAGRAM WITH PREEMPHASIS



BIT-ERROR RATE vs. CABLE LENGTH



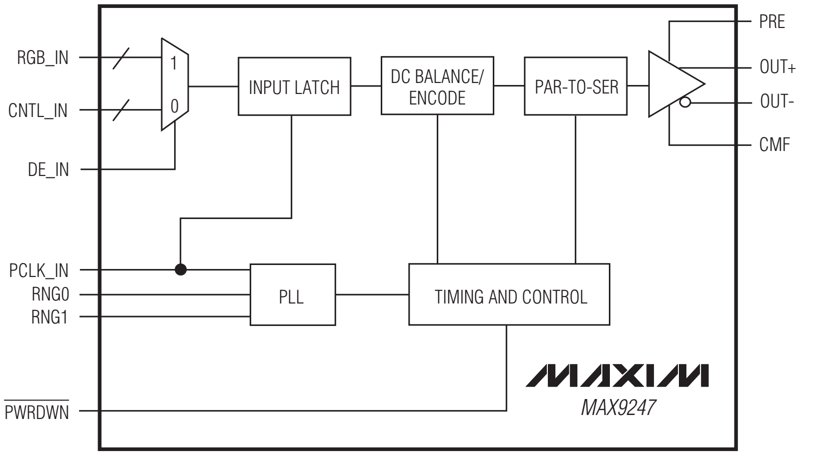
CABLE LENGTH vs. FREQUENCY BIT-ERROR RATE < 10^{-9}



Pin Description

PIN	NAME	FUNCTION
1, 13, 37	GND	Input Buffer Supply and Digital Supply Ground
2	V_{CCIN}	Input Buffer Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
3–10, 39–48	RGB_IN10–RGB_IN17, RGB_IN0–RGB_IN9	LVTTL/LVCMOS Red, Green, and Blue Digital Video Data Inputs. Eighteen data bits are loaded into the input latch on the rising edge of PCLK_IN when DE_IN is high. Internally pulled down to GND.
11, 12, 15–21	CNTL_IN0, CNTL_IN1, CNTL_IN2–CNTL_IN8	LVTTL/LVCMOS Control Data Inputs. Control data are latched on the rising edge of PCLK_IN when DE_IN is low. Internally pulled down to GND.
14, 38	V_{CC}	Digital Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
22	DE_IN	LVTTL/LVCMOS Data-Enable Input. Logic-high selects RGB_IN[17:0] to be latched. Logic-low selects CNTL_IN[8:0] to be latched. DE_IN must be switching for proper operation. Internally pulled down to GND.
23	PCLK_IN	LVTTL/LVCMOS Parallel Clock Input. Latches data and control inputs and provides the PLL reference clock. Internally pulled down to GND.
24	I.C.	Internally Connected. Leave unconnected for normal operation.
25	PRE	Preemphasis Enable Input. Drive PRE high to enable preemphasis.
26	PLLGND	PLL Supply Ground
27	V_{CCPLL}	PLL Supply Voltage. Bypass to PLLGND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
28	$\overline{\text{PWRDWN}}$	LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND.
29	CMF	Common-Mode Filter. Optionally connect a capacitor between CMF and LVDSGND to filter common-mode switching noise.
30, 31	LVDSGND	LVDS Supply Ground
32	OUT-	Inverting LVDS Serial-Data Output
33	OUT+	Noninverting LVDS Serial-Data Output
34	V_{CCLVDS}	LVDS Supply Voltage. Bypass to LVDSGND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
35	RNG1	LVTTL/LVCMOS Frequency Range Select Input. Set to the frequency range that includes the PCLK_IN frequency as shown in Table 3. Internally pulled down to GND.
36	RNG0	LVTTL/LVCMOS Frequency Range Select Input. Set to the frequency range that includes the PCLK_IN frequency as shown in Table 3. Internally pulled down to GND.

Functional Diagram



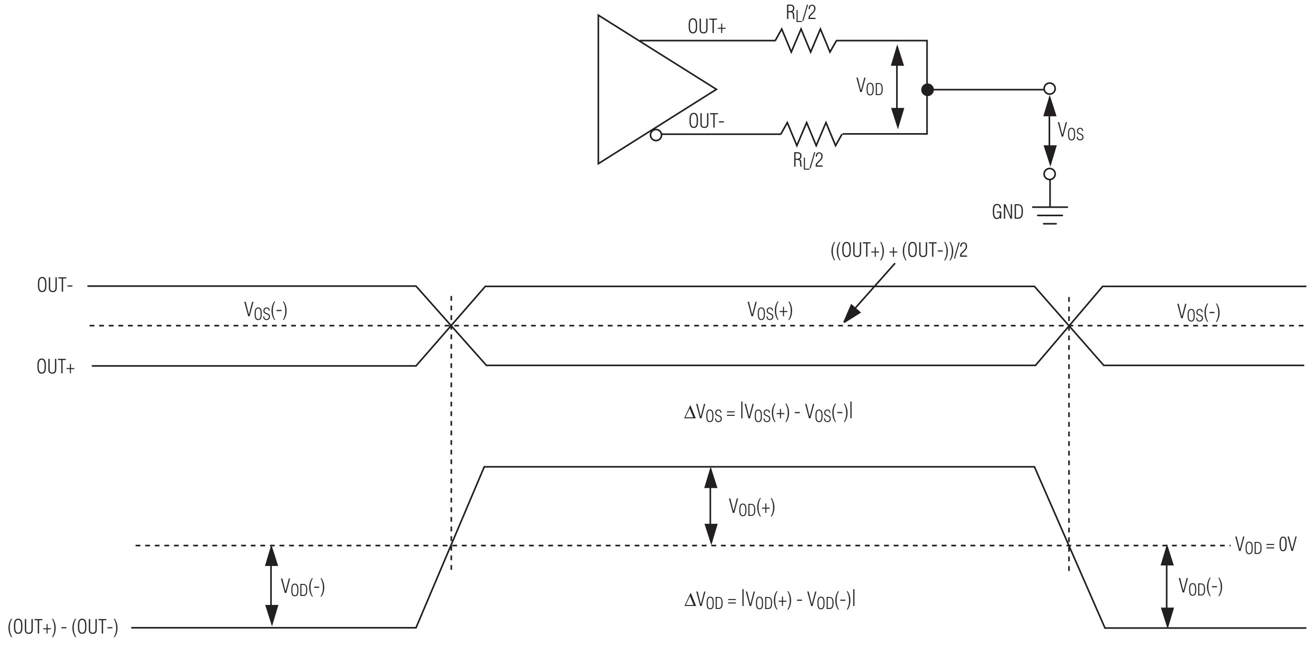


Figure 1. LVDS DC Output Load and Parameters

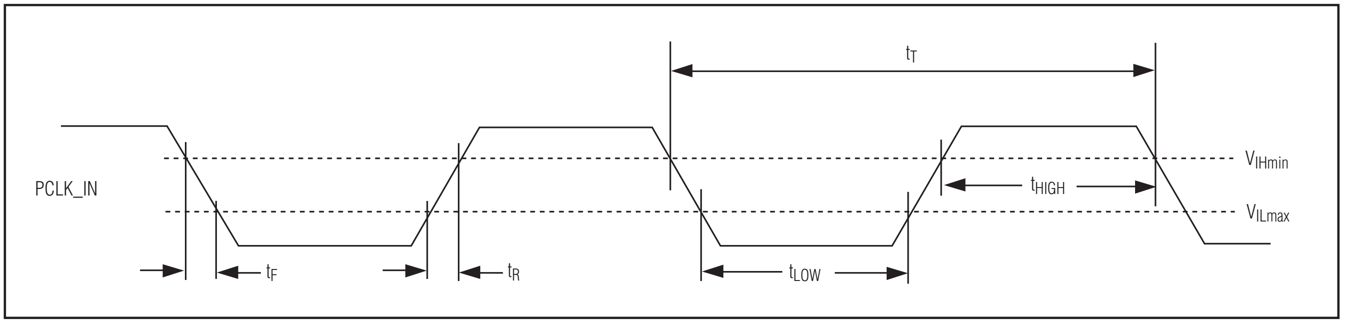


Figure 2. Parallel Clock Requirements

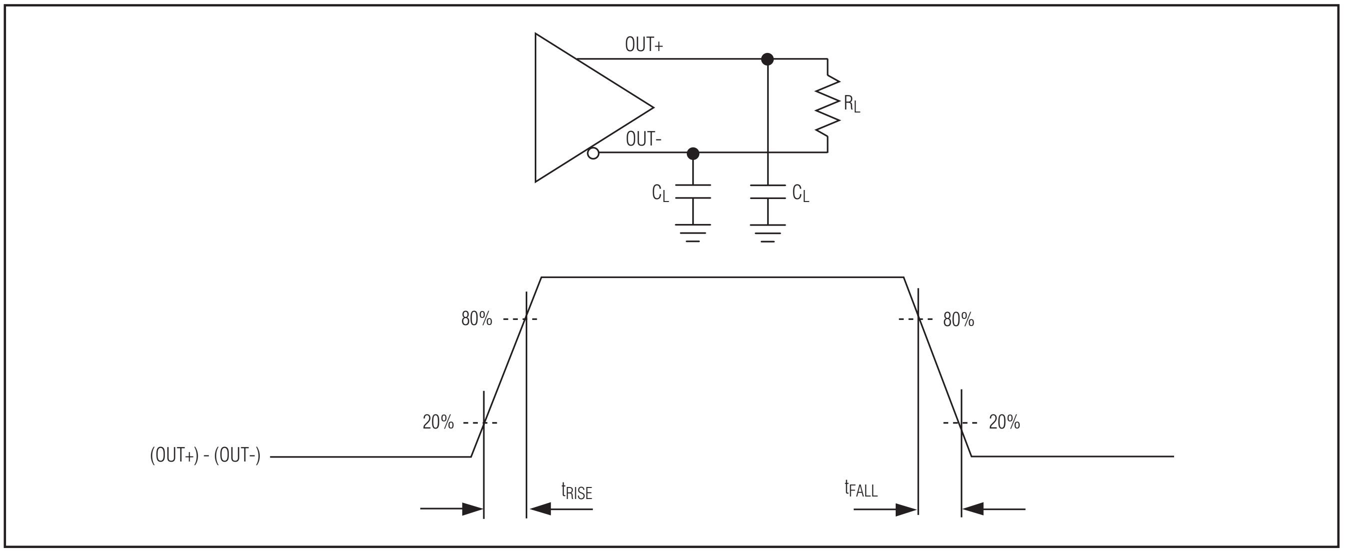


Figure 3. Output Rise and Fall Times

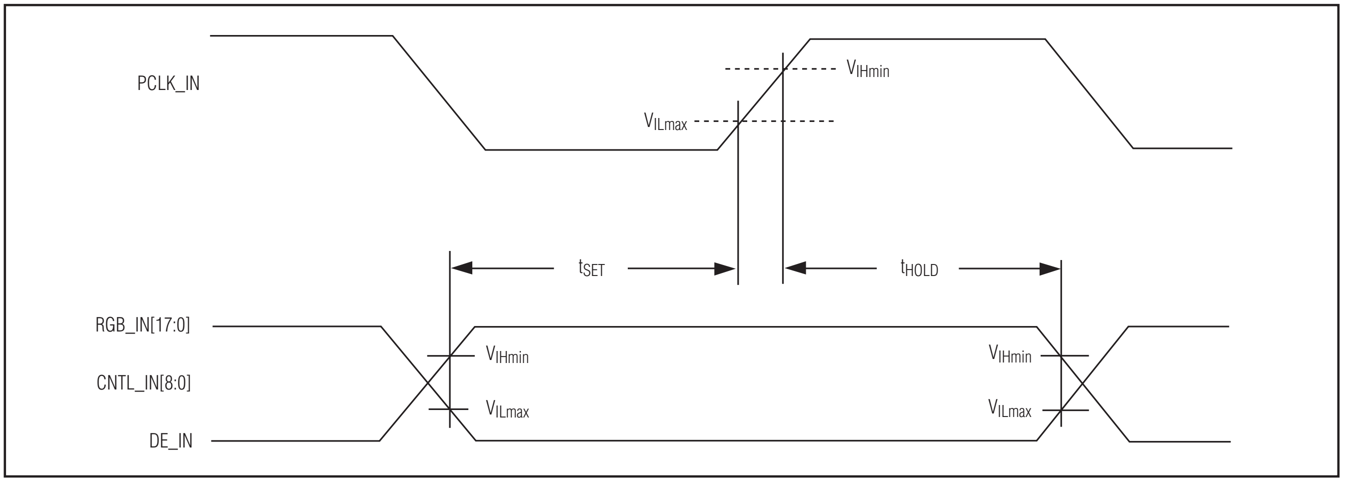


Figure 4. Synchronous Input Timing

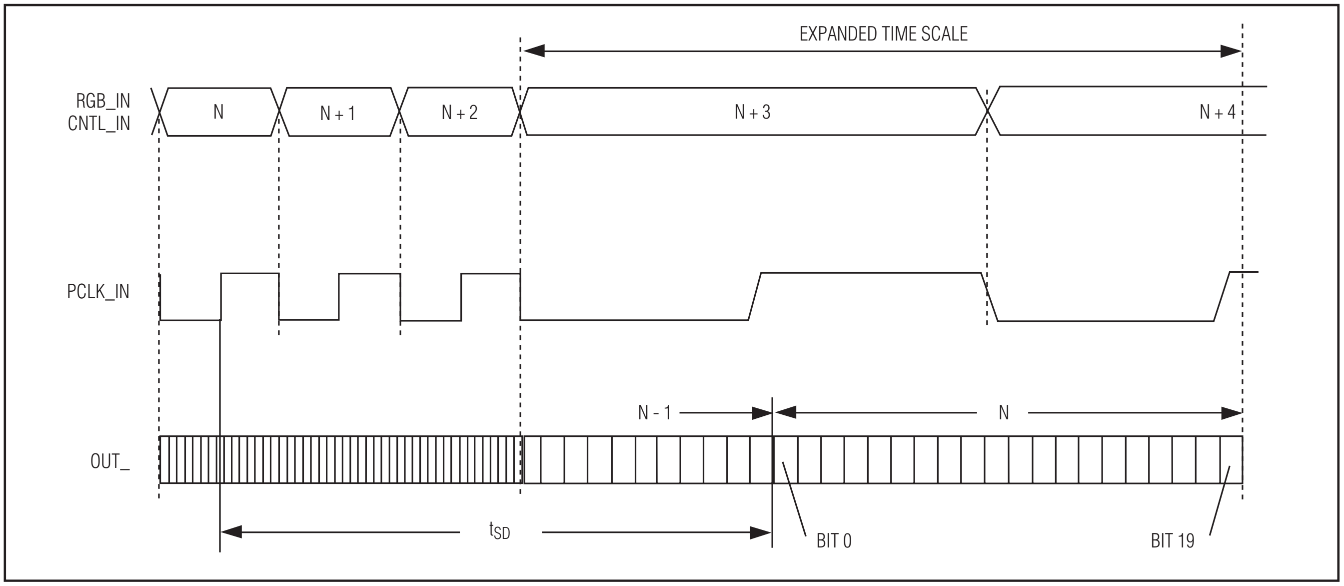


Figure 5. Serializer Delay

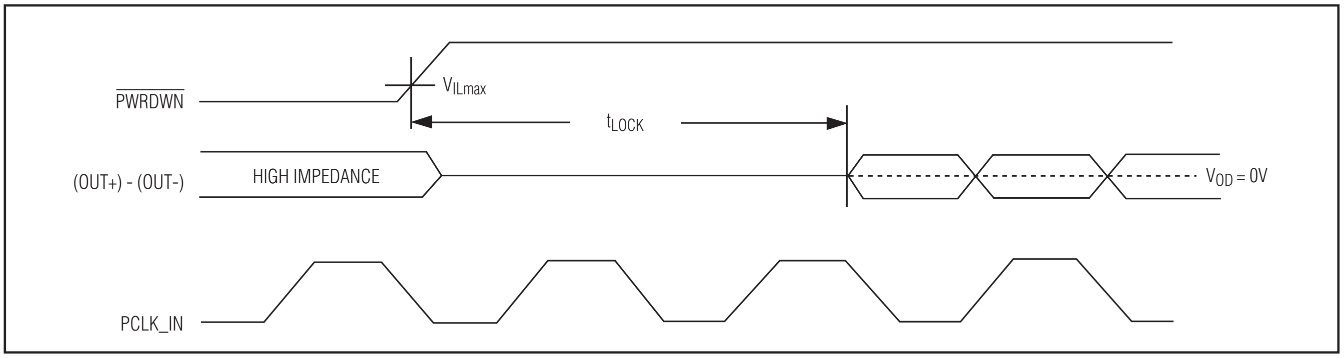


Figure 6. PLL Lock Time

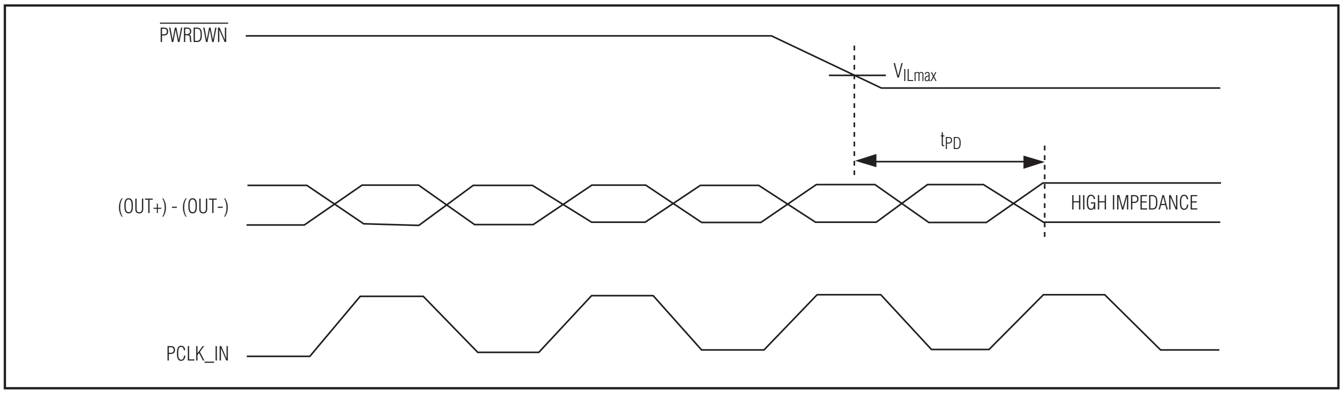


Figure 7. Power-Down Delay

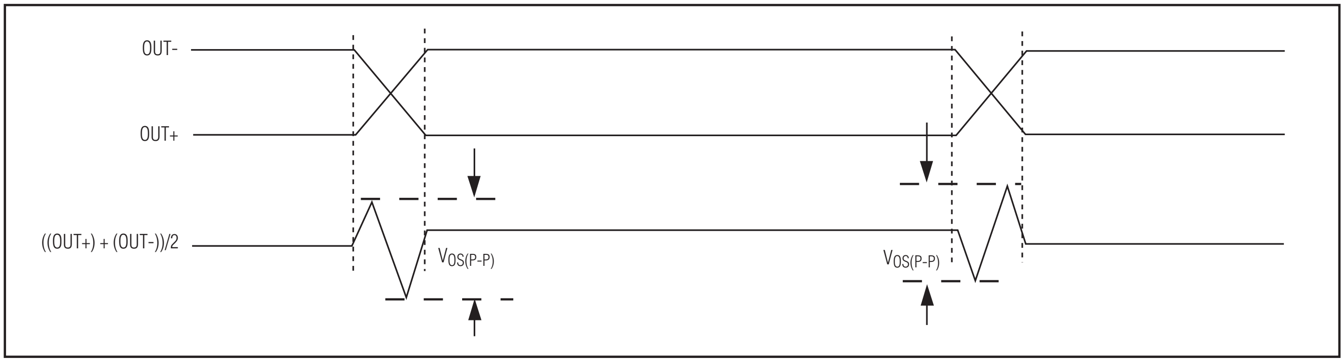


Figure 8. Peak-to-Peak Output Offset Voltage

Detailed Description

The MAX9247 DC-balanced serializer operates at a 2.5MHz-to-42MHz parallel clock frequency, serializing 18 bits of parallel video data RGB_IN[17:0] when the data-enable input DE_IN is high, or 9 bits of parallel control data CNTL_IN[8:0] when DE_IN is low. The RGB video input data are encoded using 2 overhead bits, EN0 and EN1, resulting in a serial word length of 20 bits (see Table 1). Control inputs are mapped to 19 bits and encoded with 1 overhead bit, EN0, also resulting in a 20-bit serial word. Encoding reduces EMI and maintains DC balance across the serial cable. Two transition words, which contain a unique bit sequence, are inserted at the transition boundaries of video-to-control and control-to-video phases.

Control data inputs C0 to C4 are mapped to 3 bits each in the serial control word (see Table 2). At the deserializer, 2 or 3 bits at the same state determine the state of the recovered bit, providing single-bit-error tolerance for C0 to C4. Control data that may be visible if an error occurs, such as VSYNC and HSYNC, can be connected to these inputs. Control data inputs C5 to C8 are mapped to 1 bit each.

Table 1. Serial Video Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	EN1	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17

Bit 0 is the LSB and is serialized first. EN[1:0] are encoding bits. S[17:0] are encoded symbols.

Table 2. Serial Control Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	C0	C0	C0	C1	C1	C1	C2	C2	C2	C3	C3	C3	C4	C4	C4	C5	C6	C7	C8

Bit 0 is the LSB and is serialized first. C[8:0] are the control inputs.

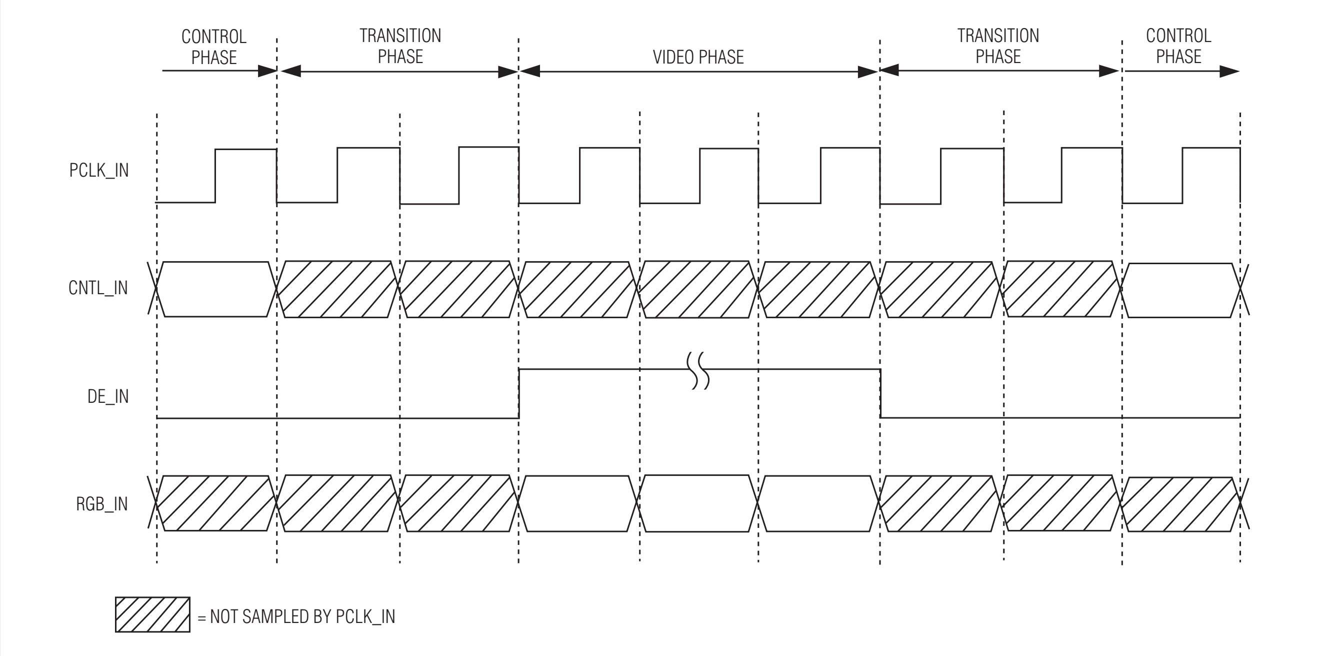


Figure 9. Transition Timing

Transition Timing

The transition words require interconnect bandwidth and displace control data. Therefore, control data is not sampled (see Figure 9):

- Two clock cycles before DE_IN goes high
- During the video phase
- Two clock cycles after DE_IN goes low

The last sampled control data are latched at the deserializer control data outputs during the transition and video phases. Video data are latched at the deserializer RGB data outputs during the transition and control phases.

Applications Information

AC-Coupling Benefits

AC-coupling increases the common-mode voltage to the voltage rating of the capacitor. Two capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise. The MAX9247 serializer can also be DC-coupled to the MAX9248/MAX9250 deserializers.

Figures 10 and 12 show an AC-coupled serializer and deserializer with two capacitors per link. Figures 11 and 13 show the AC-coupled serializer and deserializer with four capacitors per link.

Selection of AC-Coupling Capacitors

See Figure 14 for calculating the capacitor values for AC-coupling depending on the parallel clock frequency. The plot shows capacitor values for two- and four-capacitor-per-link systems. For applications using less than 18MHz clock frequency, use 0.1µF capacitors.

Frequency-Range Setting RNG[1:0]

The RNG[1:0] inputs select the operating frequency range of the MAX9247 serializer. An external clock within this range is required for operation. Table 3 shows the selectable frequency ranges and corresponding data rates for the MAX9247.

Table 3. Parallel Clock Frequency Range Select

RNG1	RNG0	PARALLEL CLOCK (MHz)	SERIAL-DATA RATE (Mbps)
0	0	2.5 to 5	50 to 100
0	1	5 to10	100 to 200
1	0	10 to 20	200 to 400
1	1	20 to 42	400 to 840

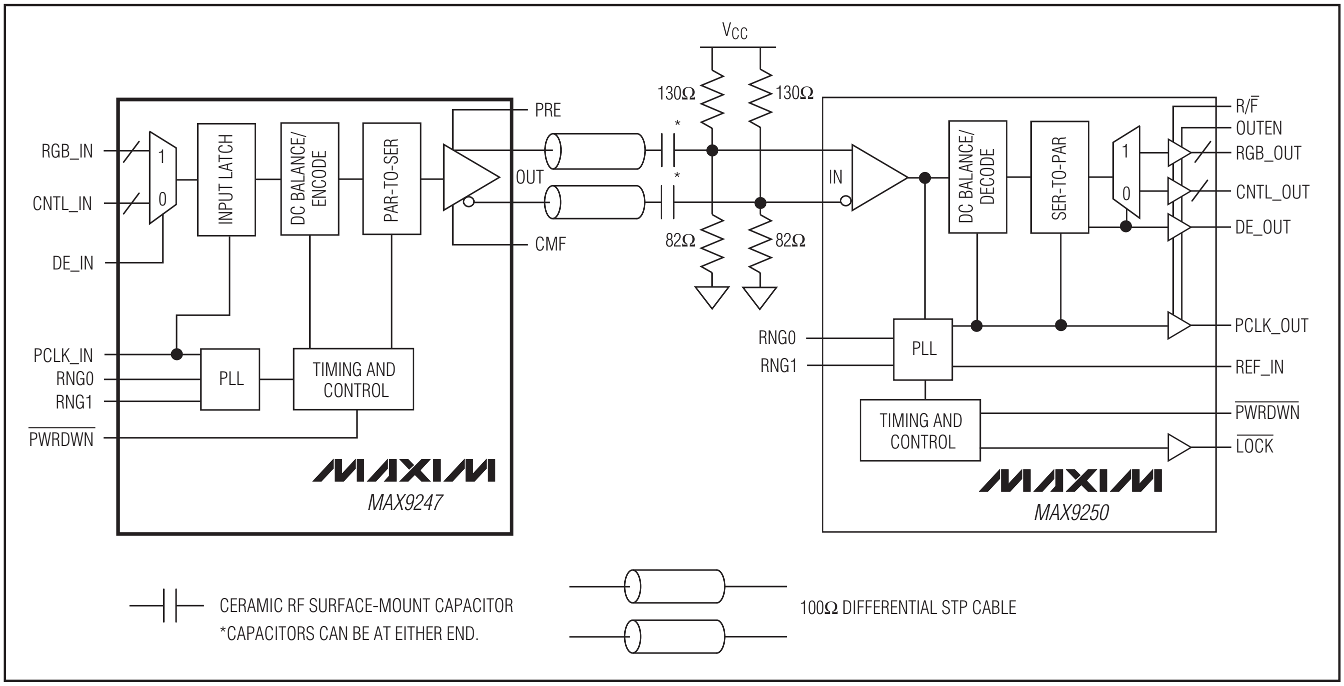


Figure 10. AC-Coupled MAX9247 Serializer and MAX9250 Deserializer with Two Capacitors per Link

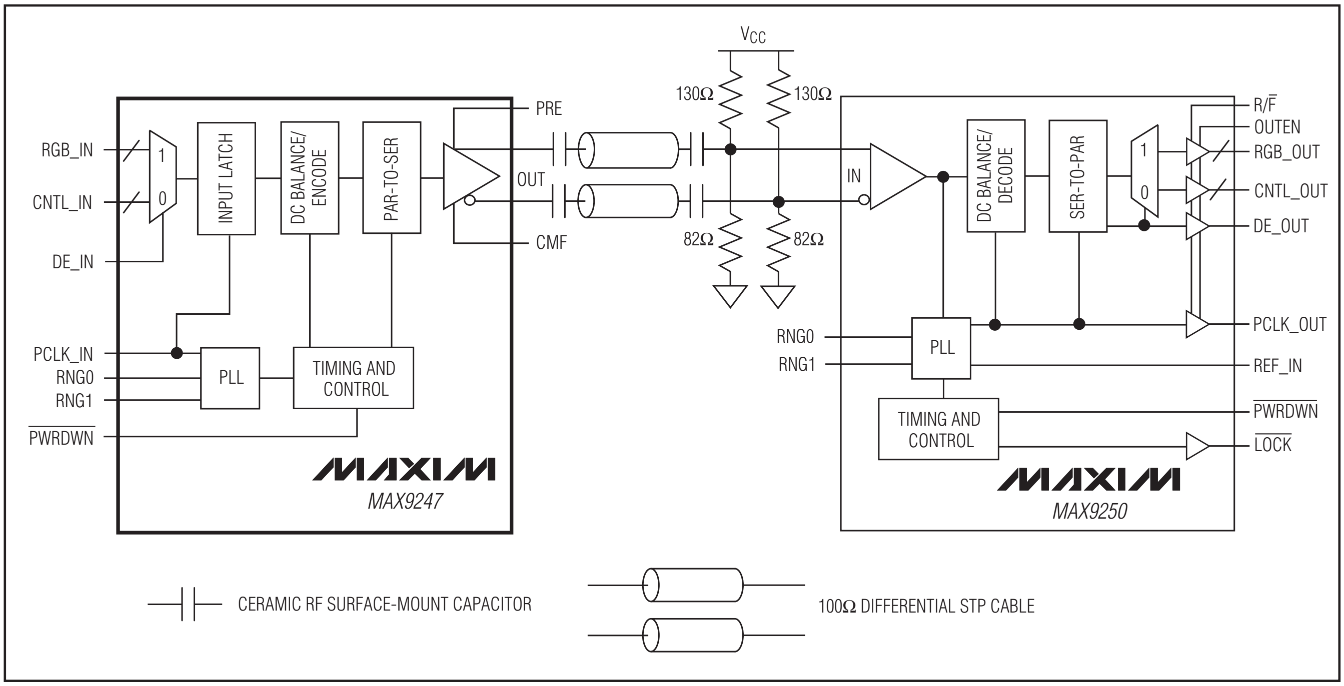


Figure 11. AC-Coupled MAX9247 Serializer and MAX9250 Deserializer with Four Capacitors per Link

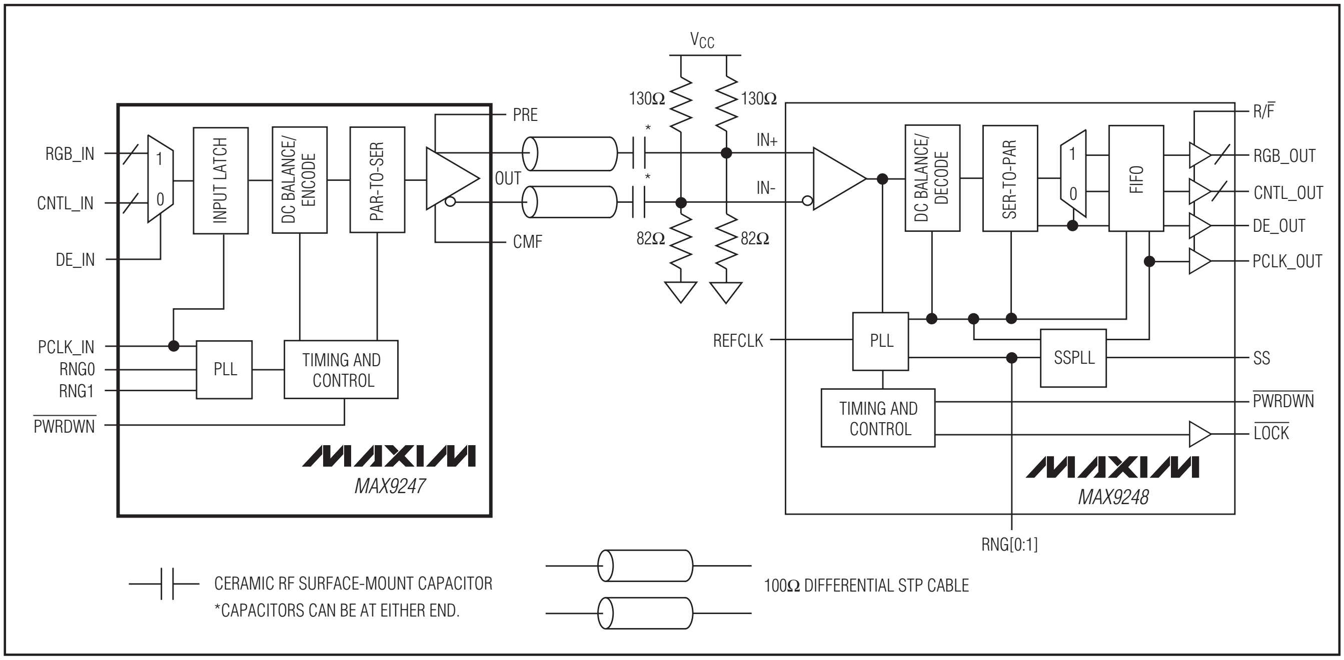


Figure 12. AC-Coupled MAX9247 Serializer and MAX9248 Deserializer with Two Capacitors per Link

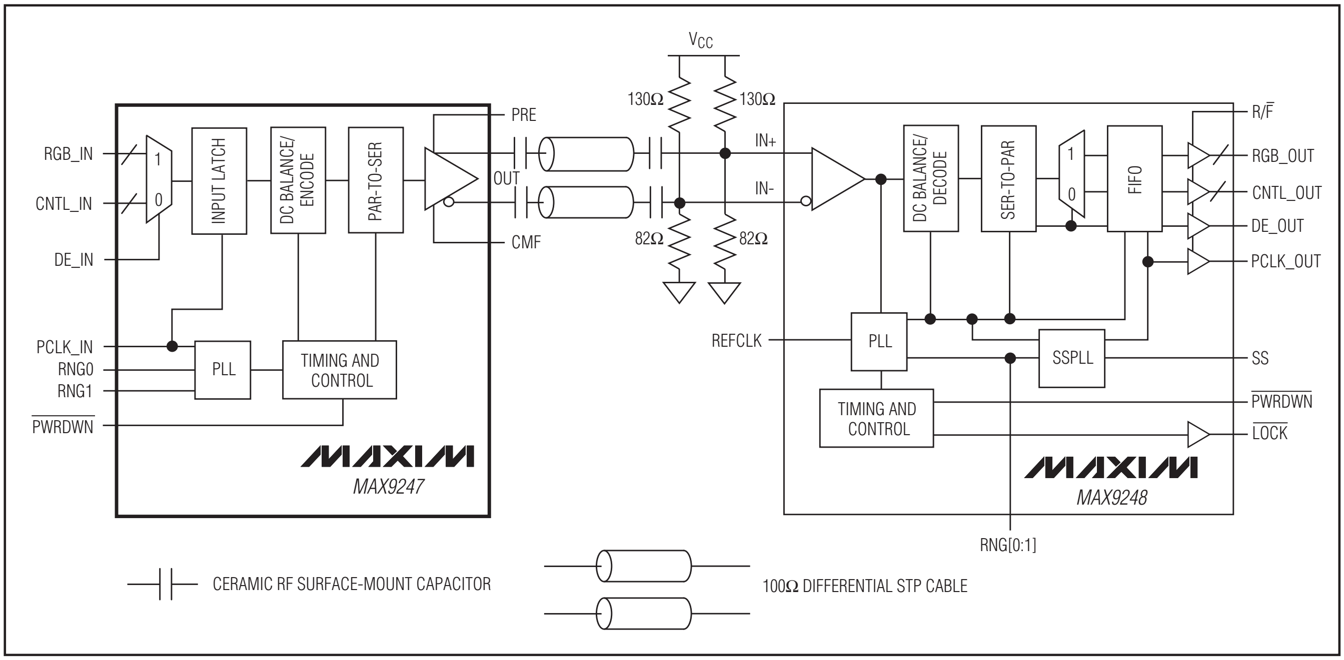


Figure 13. AC-Coupled MAX9247 Serializer and MAX9248 Deserializer with Four Capacitors per Link

27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Serializer

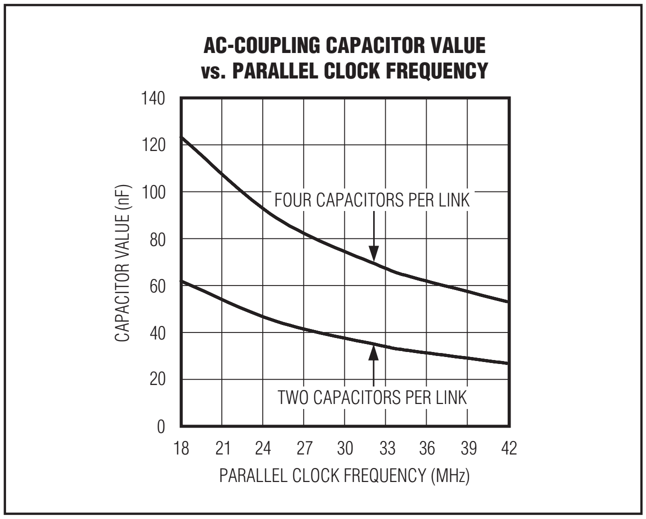


Figure 14. AC-Coupling Capacitor Values vs. Clock Frequency of 18MHz to 42MHz

Termination

The MAX9247 has an integrated 100Ω output-termination resistor. This resistor damps reflections from induced noise and mismatches between the transmission line impedance and termination resistors at the deserializer input. With PWRDWN = low or with the supply off, the output termination is switched out and the LVDS output is high impedance.

Common-Mode Filter

The integrated 100Ω output termination is made up of two 50Ω resistors in series. The junction of the resistors is connected to the CMF pin for connecting an optional common-mode filter capacitor. Connect the filter capacitor to ground close to the MAX9247 as shown in Figure 15. The capacitor shunts common-mode switching current to ground to reduce EMI.

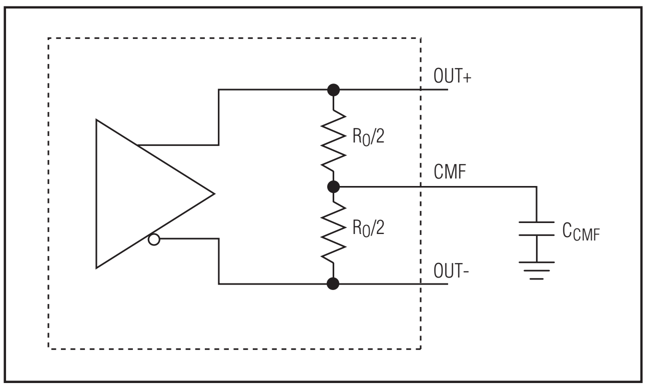


Figure 15. Common-Mode Filter Capacitor Connection

LVDS Output Preemphasis (PRE)

The MAX9247 features a preemphasis mode where extra current is added to the output and causes the amplitude to increase by 40% to 50% at the transition point. Preemphasis helps to get a faster transition, better eye diagram, and improve signal integrity. See the *Typical Operating Characteristics*. The additional current is turned on for a short time (360ps, typ) during data transition, and then turned off. Enable preemphasis by driving PRE high.

Power-Down and Power-Off

Driving PWRDWN low stops the PLL, switches out the integrated 100Ω output termination, and puts the output in high impedance to ground and differential. With PWRDWN ≤ 0.3V and all LVTTL/LVCMOS inputs ≤ 0.3V or ≥ V_{CCIN} - 0.3V, supply current is reduced to 50µA or less.

Driving PWRDWN high starts PLL lock to PCLK_IN and switches in the 100Ω output termination resistor. The LVDS output is not driven until the PLL locks. The LVDS output is high impedance to ground and 100Ω differential. The 100Ω integrated termination pulls OUT+ and OUT- together while the PLL is locking so that V_{OD} = 0V.

If V_{CC} = 0, the output resistor is switched out and the LVDS outputs are high impedance to ground and differential.

PLL Lock Time

The PLL lock time is set by an internal counter. The lock time is 17,100 PCLK_IN cycles. Power and clock should be stable to meet the lock-time specification.

Input Buffer Supply

The single-ended inputs (RGB_IN[17:0], CNTL_IN[8:0], DE_IN, RNG0, RNG1, PRE, PCLK_IN, and PWRDWN) are powered from V_{CCIN}. V_{CCIN} can be connected to a 1.71V to 3.6V supply, allowing logic inputs with a nominal swing of V_{CCIN}. If no power is applied to V_{CCIN} when power is applied to V_{CC}, the inputs are disabled and PWRDWN is internally driven low, putting the device in the power-down state.

Power-Supply Sequencing of MAX9247 and MAX9248/MAX9250 Video Link

The MAX9247 and MAX9248/MAX9250 video link can be powered up in several ways. The best approach is to keep both MAX9247 and MAX9248 powered down while supplies are ramping up and PCLK_IN of the MAX9247 and REFCLK of the MAX9248/MAX9250 are stabilizing. After all of the power supplies of the MAX9247 and MAX9248/MAX9250 are stable, including PCLK_IN and REFCLK, do the following:

1) Power up the MAX9247 first

2) Wait for at least t_{LOCK} of MAX9247 (or 17100 x t_T) to get activity on the link
3) Power up the MAX9248

Power-Supply Circuits and Bypassing

The MAX9247 has isolated on-chip power domains. The digital core supply (V_{CC}) and single-ended input supply (V_{CCIN}) are isolated but have a common ground (GND). The PLL has separate power and ground (V_{CCPLL} and PLLGND) and the LVDS input also has separate power and ground (V_{CCLVDS} and LVDSGND). The grounds are isolated by diode connections. Bypass each V_{CC}, V_{CCIN}, V_{CCPLL}, and V_{CCLVDS} pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

LVDS Output

The LVDS output is a current source. The voltage swing is proportional to the termination resistance. The output is rated for a differential load of 100Ω ±1%.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Separate the LVTTL/LVCMOS inputs and LVDS output to prevent crosstalk. A four-layer PCB with separate layers for power, ground, and signals is recommended.

ESD Protection

The MAX9247 ESD tolerance is rated for IEC 61000-4-2, Human Body Model, Machine Model, and ISO 10605 standards. IEC 61000-4-2 and ISO 10605 specify ESD tolerance for electronic systems. The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 16). For IEC 61000-4-2, the LVDS outputs are rated for ±8kV Contact Discharge and ±15kV Air-Gap Discharge. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 17). For the Human Body Model, all pins are rated for ±3kV Contact Discharge. The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 18). For ISO 10605, the LVDS outputs are rated for ±10kV contact and ±30kV air discharge. The Machine Model discharge components are C_S = 200pF and R_D = 0Ω (Figure 19).

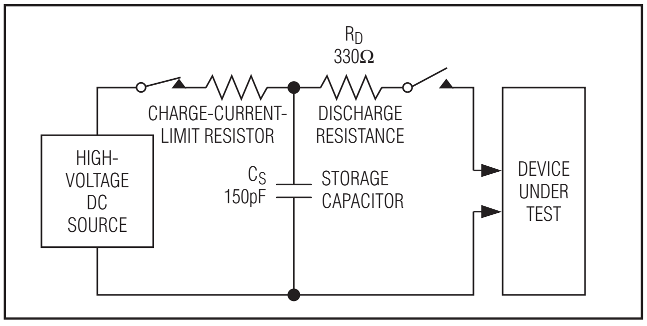


Figure 16. IEC 61000-4-2 Contact Discharge ESD Test Circuit

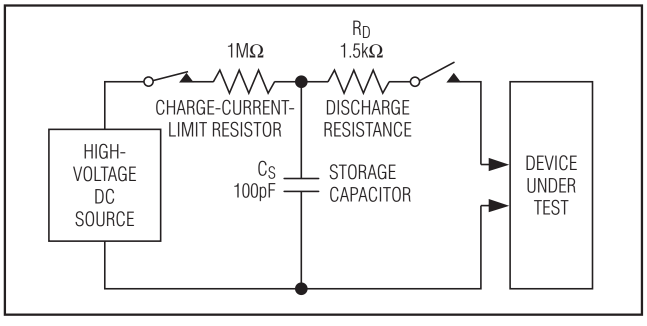


Figure 17. Human Body ESD Test Circuit

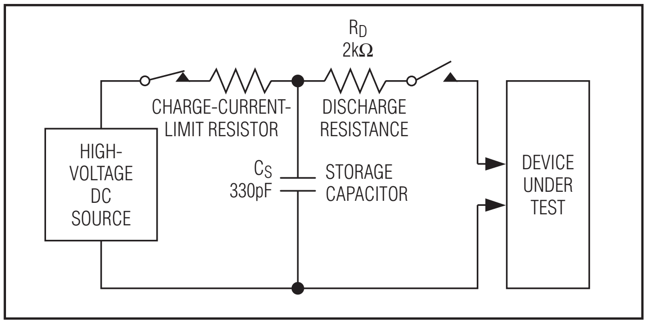


Figure 18. ISO 10605 Contact Discharge ESD Test Circuit

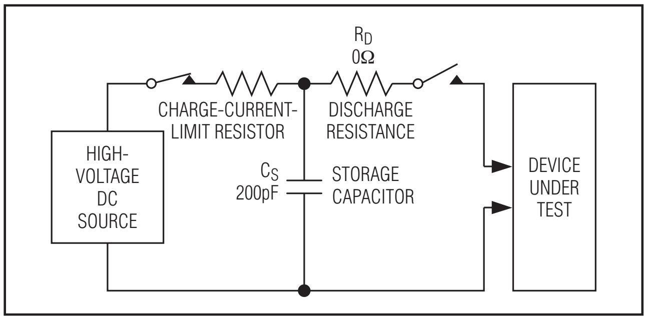


Figure 19. Machine Model ESD Test Circuit

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 LQFP	C48+5	**21-0054**	**90-0093**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	5/08	Corrected LQFP package, added +105°C part, changed temperature limits for +105°C rated part, and added Machine Model ESD text and diagram	1–6, 15–19
3	4/09	Added /V parts in the *Ordering Information* table and added new *Power-Supply Sequencing of MAX9247 and MAX9248/MAX9250 Video Link* section	1, 14
4	4/12	Corrected errors in *Absolute Maximum Ratings* and *Pin Description* sections	2, 6