Combi PFC/ PWM Controller
ICE1CS02
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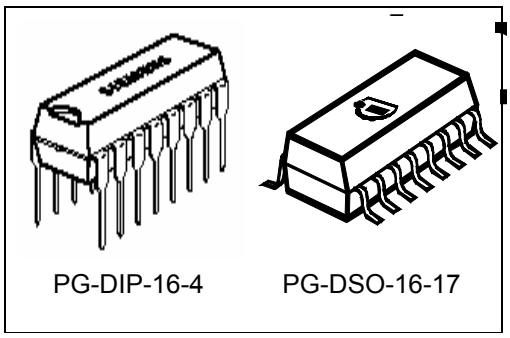
Combi PFC/ PWM Controller

ICE1CS02

Off-Line SMPS Current Mode PFC/ PWM Combinational Controller

Product Highlights

- **Internal Synchronization**
- **External Synchronization**
- **Pre-short Protection**
- **AC brownout feature**
- **Pb-free lead plating, RoHS compilant**
- **Enhanced Dynamic Response**



PG-DIP-16-4 PG-DSO-16-17

Features

- Fast, soft switching totem pole gate drive (2 A)
- Tolerance of Trimmed Reference Voltage ±2.5% (±2% at 25°C)
- BiCMOS technology provides wide VCC Range

PFC Section

- 65 kHz fixed switching frequency synchronized with PWM switching frequency
- Ease of Use with Few External Components
- Supports Wide Range
- Average Current Control
- External Current and Voltage Loop Compensation for Greater User Flexibility
- Max Duty Cycle of 95% (typ)
- Fulfills Class D Requirements of IEC 1000-3-2
- Enhanced Dynamic Response
- Unique Soft-Start to Limit Start Up Current
- Over-Voltage Protection

PWM Section

- 130 kHz fixed Switching Frequency synchronizable externally
- Built in Soft Start
- Minimum of external Components required
- Max Duty Cycle 47% or 60%
- Overall Tolerance of Current Limiting < ±5%
- Internal Leading Edge Blanking
- Extended Hold-up Time with PWM input voltage protection
- Slope Compensation

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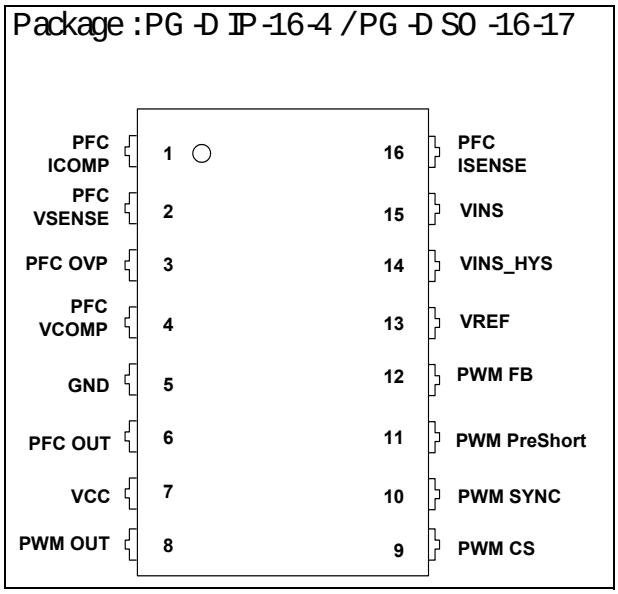
1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	PFC ICOMP	Current Loop Compensation
2	PFC VSENSE	V_{BUS} Sense Input
3	PFC OVP	V_{BUS} Overvoltage Sense Input
4	PFC VCOMP	Voltage Loop Compensation
5	GND	Controller Ground
6	PFC OUT	GATE OUT
7	VCC	Controller Supply Voltage
8	PWM OUT	GATE OUT
9	PWM CS	Current Sense
10	PWM SYNC/ Duty Cycle	Dual function pin: SYNC and Duty Cycle Setting
11	PWM Preshort	Adjustable Blanking Time Input
12	PWM FB	Feedback
13	VREF	5V reference voltage
14	VINS HYS	Input Voltage Hystersis
15	VINS	Input Voltage Brown out
16	PFC ISENSE	Current Sense Input

Figure 1 Pin Configuration(top view)



1.2 Pin Functionality

PFC ICOMP (Current Loop Compensation)

Low pass filter and compensation of the current control loop. The capacitor which is connected at this pin integrates the output current of OTA2 and averages the current sense signal.

PFC VSENSE (Voltage Sense/Feedback)

The output bus voltage is sensed at this pin via a resistive divider. The reference voltage for this pin is 3V.

PFC OVP (Overvoltage Sense Input)

The output bus overvoltage is sensed at this pin via a resistive divider. The reference voltage for this pin is 3V.

PFC VCOMP (Voltage Loop Compensation)

This pin provides the compensation of the output voltage loop with a compensation network to ground (see Figure 2). This also gives the soft start function which controls an increasing AC input current during start-up.

GND (Ground)

The GND pin is the ground of the controller.

PFC OUT (PFC Gate Output)

This pin is the output of the internal driver stage, which has a capability of 1.5A source and 2.0A sink current.

Its gate drive voltage is clamped at 15V (typically).

VCC (Power Supply)

The VCC pin is the positive supply of the IC and should be connected to an external auxiliary supply. The operating range is between 11V and 26V. The turn-on threshold is at 12V and under voltage occurs at 11V. There is no internal clamp for a limitation of the power supply.

PWM OUT (PWM Gate Output)

This pin is the output of the internal driver stage, which has a capability of 1.5A source and 2.0A sink current.

Its gate drive voltage is clamped at 15V (typically).

PFC ISENSE (Current Sense Input)

The ISENSE Pin senses the voltage drop at the external sense resistor (R1). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block.

VINS (Input Voltage Sensing)

The VINS pin can sense the rectified AC main line signal. When the signal drops below the voltage set externally, the gate signal will stop and it would resume with soft-start when the signal exceeds the voltage externally set.

VINS HYS (Input Voltage Sensing hystersis)

This pin is the output of a comparator. Putting a resistor between VINS and VINS HYS will set the hystersis of PFC Brown Out protection.

VREF (Reference Voltage)

This pin is the output of buffer, which has a capability of supplying 5V with a 12mA sourcing current (minimum).

When the output is pulled to low, the PWM portion will stop switching and when the output is released, the PWM will resume switching with soft-start.

PWM FB (PWM Feedback)

The IC will obtain the output information through his pin. The internal Protection Unit and the internal PWM-Comparator will then control the duty cycle.

PWM Pre-short

This pin set the blanking time the IC will enter into Output Pre-short protection mode by connecting a capacitor.

PWM SYNC (External Sychronization) and Duty Cycle (Duty Cycle Selection)

This pin allows 2 functions: 1)synchronization of external oscillator with internal PWM clock and 2) Duty Cycle selection. The frequency range is from 70kHz to 150kHz while PFC frequency range is from 35kHz to 75kHz respectively and the duty cycle is set according to resistor tied to the pin, setting the max duty cycle to either to 47% or 60%. If Vsense is greater than 2.6V (Vout is greater than 330V), the max duty cycle will still be set back to 47%.

PWM CS (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the MOS switch. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is used for Current Mode control. Slope compensation is activated when Vsync is less than 3.0V.

2 Representative Blockdiagram

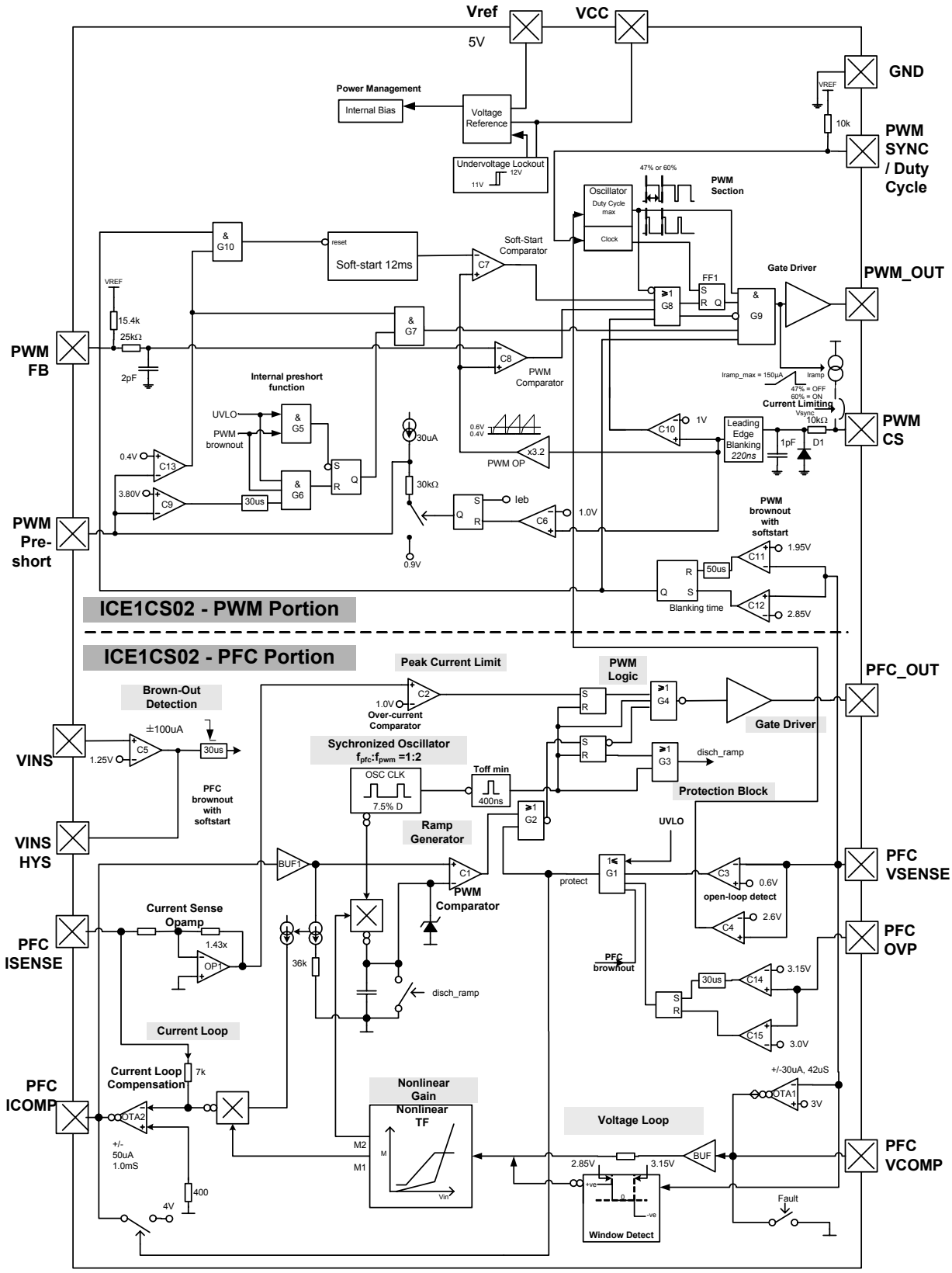


Figure 2 Representative Blockdiagram

3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 Introduction

The ICE1CS02 comprises the complete control for power factor controlled switched mode power supplies. With its PFC and PWM section being internally synchronized, applies for off-line converters with input voltages ranging from 90 V to 270 V.
The topology of the PFC preconverter is boost.
The minimal line current gaps for the maximum duty cycle of the PFC is about 95%. The selectable maximum duty of the PWM, however, is limited to 47% or 60% to prevent transformer saturation.
The external RC-filter in the feedback line after the optocoupler is integrated into the IC in order to reduce the external component count.
The Soft-Start function is integrated into the IC.
An internal precise peak current control is integrated into the IC. With this function, the costs of the power transformer and the secondary rectifier diode can be reduced and the max power can also be limited. The maximum power is almost independent from the input voltage. Hence, it can avoid to over-size the critical components of the SMPS such as the power transformer or the secondary rectifier diode.

3.2 Power Management

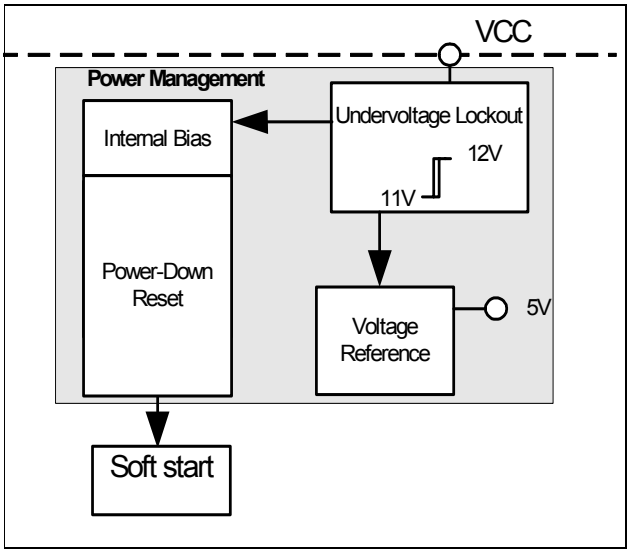


Figure 3 Power Management

The Undervoltage Lockout monitors the external supply voltage V_{VCC}. When the V_{VCC} exceeds the on-threshold V_{CCon}=12V, the internal bias circuit is switched on. A hysteresis sequence is implemented to avoid the uncontrolled rings during switch-on. The switch-off of the controller will take place when V_{VCC} falls below 11V. The maximum current consumption before the controller is activated is around 1.3mA.

When V_{VCC} falls below the off-threshold; V_{CCoff}=11.0V, the internal bias circuit is switched off .

3.3 Internal Synchronization

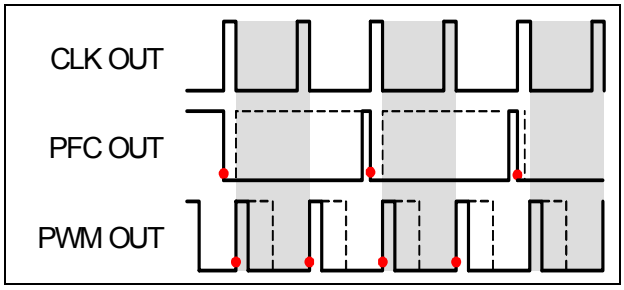


Figure 4 Internal Synchronisation between PFC and PWM Out

The clock rising edge will trigger a turn-off of PFC OUT and falling edge will trigger a turn-on of PWM OUT.

3.4 PFC Section

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM). In DCM, the average current waveform will be distorted but the resultant harmonics are still low enough to meet the Class D requirement of IEC 1000-3-2.

The outer voltage loop controls the output bus voltage. Depending on the load condition, OTA1 establishes an appropriate voltage at VCOMP pin which controls the amplitude of the average input current.

The IC is equipped with various protection features to ensure safe operating condition for both the system and device. Important protection features are namely Brown-out protection, Current Limitation and Output Under-voltage Protection.

3.4.1 Power Supply

An internal under voltage lockout (UVLO) block monitors the VCC power supply. As soon as it exceeds 12V and the voltage at pin 2 (PFC VSENSE) is >0.6V, the IC begins operating its gate drive and performs its Startup as shown in Figure 5.

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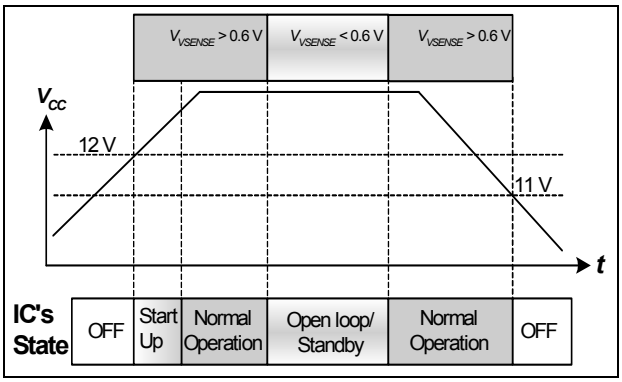


Figure 5 State of Operation respect to VCC

If VCC drops below 11V, the IC is off. The IC will then be consuming typically 1.3mA. The IC can be turned off and forced into standby mode by pulling down the voltage at pin 2 (PFC VSENSE) to lower than 0.6V.

3.4.2 Start-up

Figure 6 shows the operation of voltage loop's OTA1 during startup. The VCOMP pin is pull internally to ground via switch S1 during UVLO and other fault conditions (see later section on "System Protection").

During power up when V_{OUT} is less than 83% of the rated level, it sources a constant 30µA into the compensation network at VCOMP pin, causing the voltage at this pin to rise linearly. This results in a controlled linear increase of the input current from 0A thus reducing the stress on the external component.

When V_{OUT} is within 83% and 95% of the rated value, VCOMP voltage is level-shifted by the Enhance Dynamic Response function, to ensure there is no long period of low or no current.

When V_{OUT} approaches its rated value, OTA1's sourcing current drops and so does the level shift of the window detect block. The normal voltage loop then takes control.

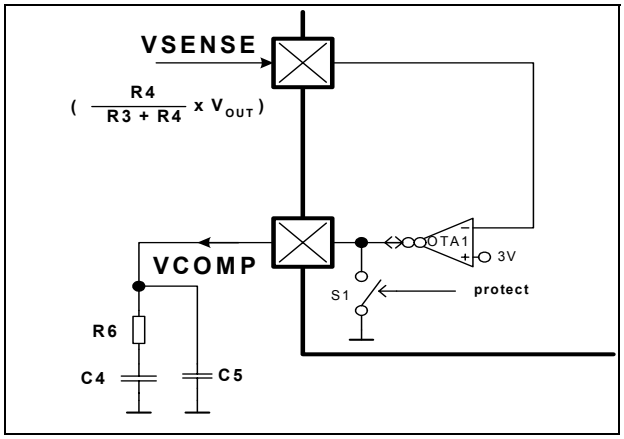


Figure 6 Start-up

3.4.3 System Protection

The IC provides several protection features in order to ensure the PFC system in safe operating range. Depending on the input line voltage (V_{IN}) and output bus voltage (V_{OUT}), Figure 7 and 8 show the conditions when these protections are active.

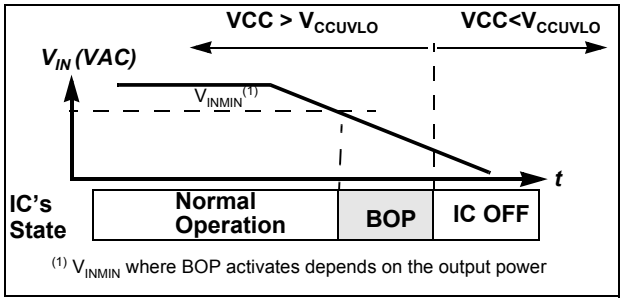


Figure 7 V_{IN} Related Protection Features

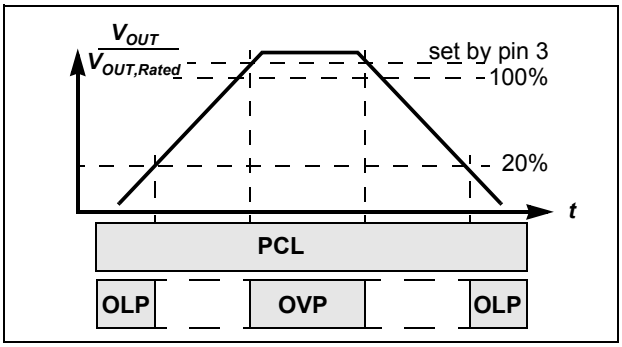


Figure 8 V_{OUT} Related Protection Features

The following sections describe the functionality of these protection features.

3.4.4 Brown-Out Protection (BOP)

Brown-out occurs when the input voltage V_{IN} falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the VCC has not entered into the V_{CCUVLO} level yet. For a system without BOP, the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current. When the input voltage V_{IN} fall below a voltage with hystersis, both set externally by resistor/ capacitor/diode network as shown in Figure 9, the PFC portion will stop switching. When the input voltage V_{IN} exceeds the voltage set externally. The hysteresis prevents the system to oscillate between normal and standby mode.

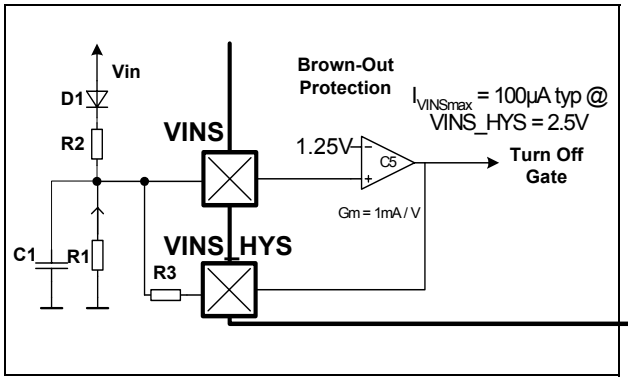


Figure 9 PFC Brown Out Protection (BOP)

3.4.5 Peak Current Limit (PCL)

The IC is designed **not** to support any output power that corresponds to a voltage lower than -0.68V at the ISENSE pin. A further increase in the inductor current, which results in a lower ISENSE voltage, will activate the Peak Current Limitation (PCL) protection.

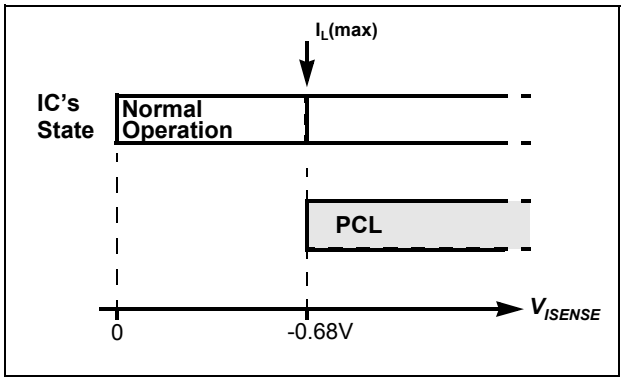


Figure 10 PCL Protection as function of V_{ISENSE}

Due to the internal parameter tolerance, the maximum inductor current is

$$I_{L(max)} = \frac{0.68}{R1}$$

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin 16 (PFC ISENSE) reaches -0.68V. This voltage is amplified by OP1 by a factor of -1.43 and connected to comparator C2 with a reference voltage of 1.0V as shown in Figure 11. The overall time delay for PCL is about 200ns ~ 500ns depending on the Isense voltage level.

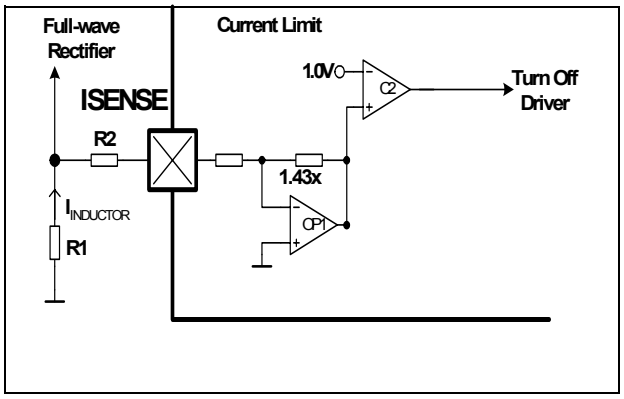


Figure 11 Peak Current Limit (PCL)

3.4.6 Open Loop Protection / Input Under Voltage Protect (OLP)

Whenever VSENSE voltage falls below 0.6V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected) or an insufficient input voltage V_{IN} for normal operation. In this case, most of the blocks within the IC will be shutdown. It is implemented using comparator C3 with a threshold of 0.6V as shown in the IC block diagram in Figure 2.

3.4.7 Over-Voltage Protection (OVP)

Whenever V_{OUT} exceeds the value set by pin 3 (PFC OVP), higher than 3.15V, the over-voltage protection OVP is active as shown in Figure 8, turning off gate. In addition, a VSENSE voltage higher than 3.15V will immediately reduce the output duty cycle, bypassing the normal voltage loop control. This results in a lower input power to reduce the output voltage V_{OUT}.

3.4.8 Complete Current Loop

The complete system current loop is shown in Figure 13.

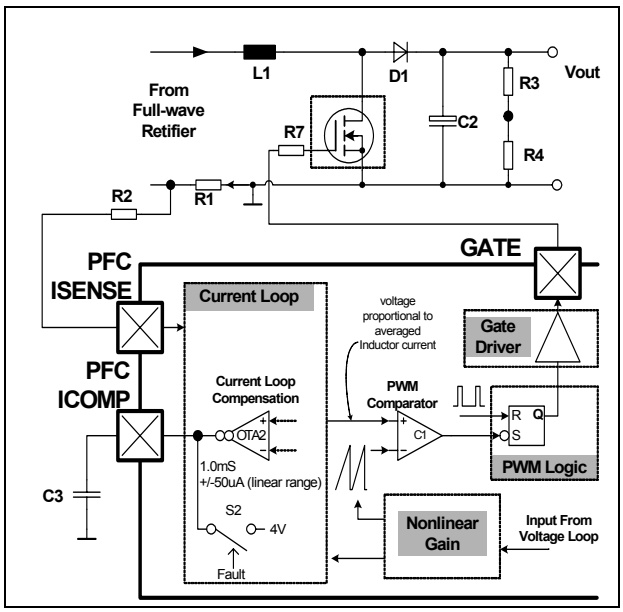


Figure 12 Complete System Current Loop

It consists of the current loop block which averages the voltage at pin 16 (PFC ISENSE), resulted from the inductor current flowing across R1. The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C1 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

3.4.9 Current Loop Compensation

The compensation of the current loop is done at the pin 1 (PFC ICOMP). This is the OTA2 output and a capacitor C3 has to be installed at this node to ground (see Figure 13). Under normal mode of operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 4V in the event of IC shuts down when OLP and UVLO occur.

3.4.10 Pulse Width Modulation (PWM)

The IC employs an average current control scheme in continuous conduction mode (CCM) to achieve the power factor correction.

Assuming the voltage loop is working and output voltage is kept constant, the off duty cycle D_{OFF} for a CCM PFC system is given as

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

From the above equation, D_{OFF} is proportional to V_{IN}.

The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle D_{OFF}, and thus to the input voltage V_{IN}. Figure 14 shows the scheme to achieve the objective.

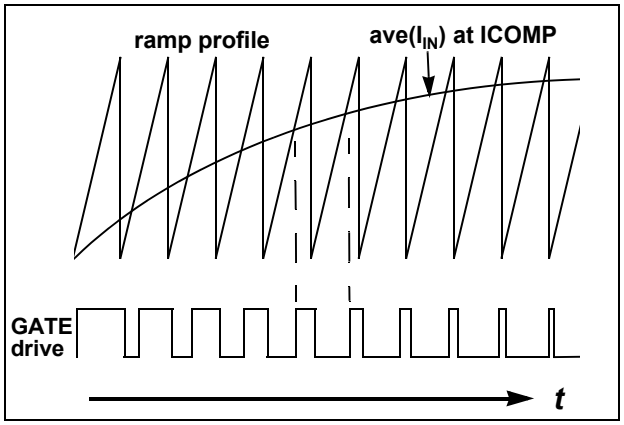


Figure 13 Average Current Control in CCM

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 1 (PFC ICOMP). The PWM cycle starts with the Gate turn off for a duration of T_{OFFMIN} (400ns typ.) and the ramp is kept discharged. The ramp is then allowed to rise after T_{OFFMIN} expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle D_{OFF}.
Figure 15 shows the timing diagrams of T_{OFFMIN} and the PWM waveforms.

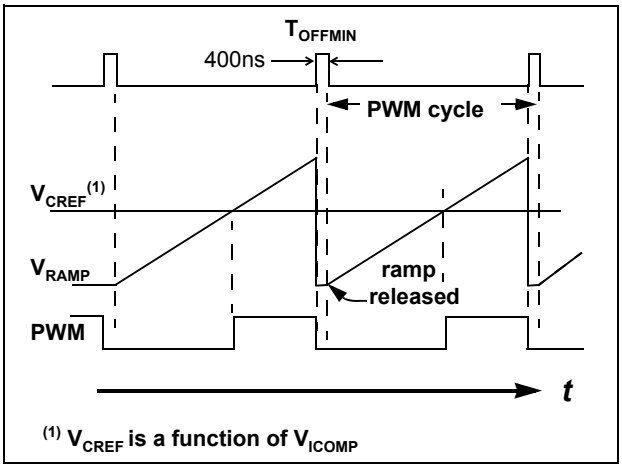


Figure 14 Ramp and PWM waveforms

3.4.11 Nonlinear Gain Block

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the voltage at pin 4 (PFC VCOMP). This block has been designed to support the wide input voltage range (85-265VAC).

3.4.12 PWM Logic

The PWM logic block prioritizes the control input signals and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse T_{OFFMIN}, are designed to meet a maximum duty cycle D_{MAX} of 95% at the GATE output under 65kHz of operation.

In case of high input currents which result in Peak Current Limitation, the GATE will be turned off immediately and maintained in off state for the current PWM cycle. The signal Toffmin resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Figure 16.

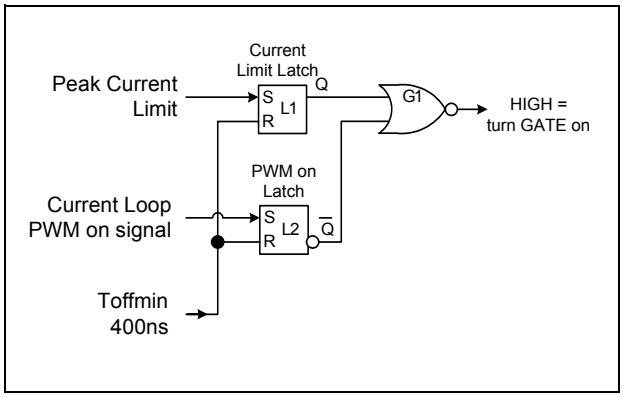


Figure 15 PWM Logic

3.4.13 Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage V_{OUT}. This loop is closed by the feedback sensing voltage at VSENSE which is a resistive divider tapping from V_{OUT}. The pin VSENSE is the input of OTA1 which has an internal reference of 3V. Figure 17 shows the important blocks of this voltage loop.

3.4.14 Voltage Loop Compensation

The compensation of the voltage loop is installed at the pin 4 (PFC VCOMP) (see Figure 17). This is the output of OTA1 and the compensation must be connected at this pin to ground. The compensation is also responsible for the soft start function which controls an increasing AC input current during start-up.

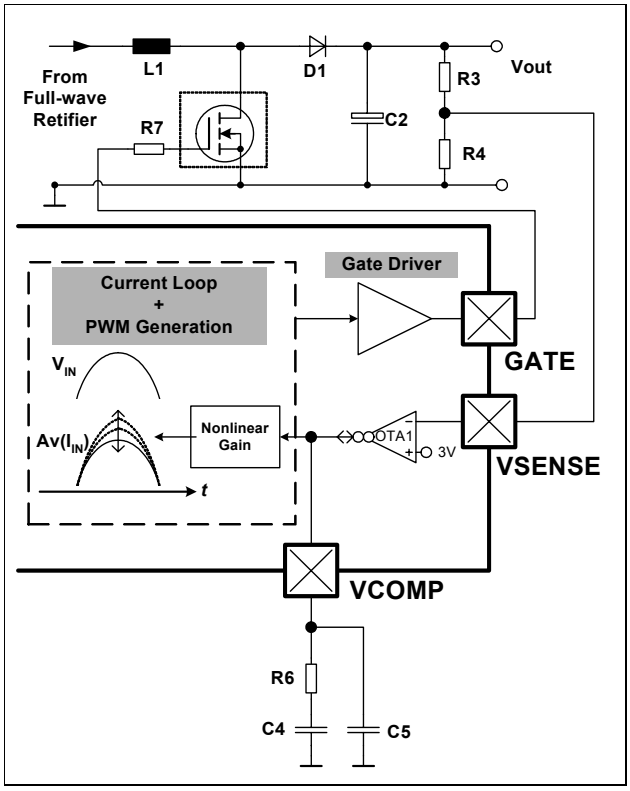


Figure 16 Voltage Loop

3.4.15 Enhanced Dynamic Response

Due to the low frequency bandwidth of the voltage loop, the dynamic response is slow and in the range of about several 10ms. This may cause additional stress to the bus capacitor and the switching transistor of the PFC in the event of heavy load changes.

The IC provides therefore a “window detector” for the feedback voltage V_{VSENSE} at pin 2 (PFC VSENSE). Whenever V_{VSENSE} exceeds the reference value (3V) by $\pm$5%, it will act on the nonlinear gain block which in turn affect the gate drive duty cycle directly. This change in duty cycle is bypassing the slow changing VCOMP voltage, thus results in a fast dynamic response of V_{OUT}.

3.4.16 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 18) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 6 (PFC OUT) is typically clamped at 15V.

The output is active HIGH and at VCC voltages below the under voltage lockout threshold VCCUVLO, the gate drive is internally pull low to maintain the off state.

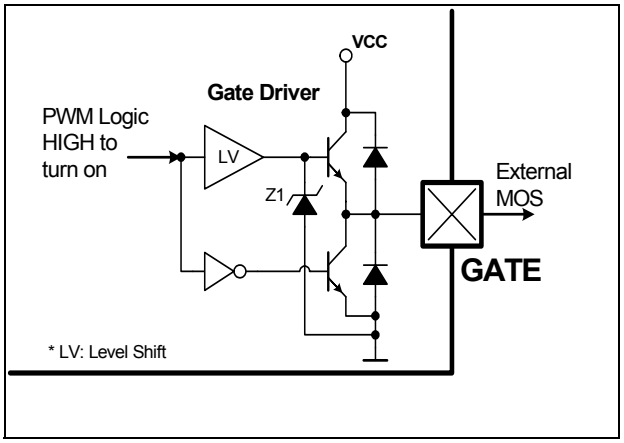


Figure 17 Gate Driver

3.5 PWM Section

3.5.1 Startup Phase

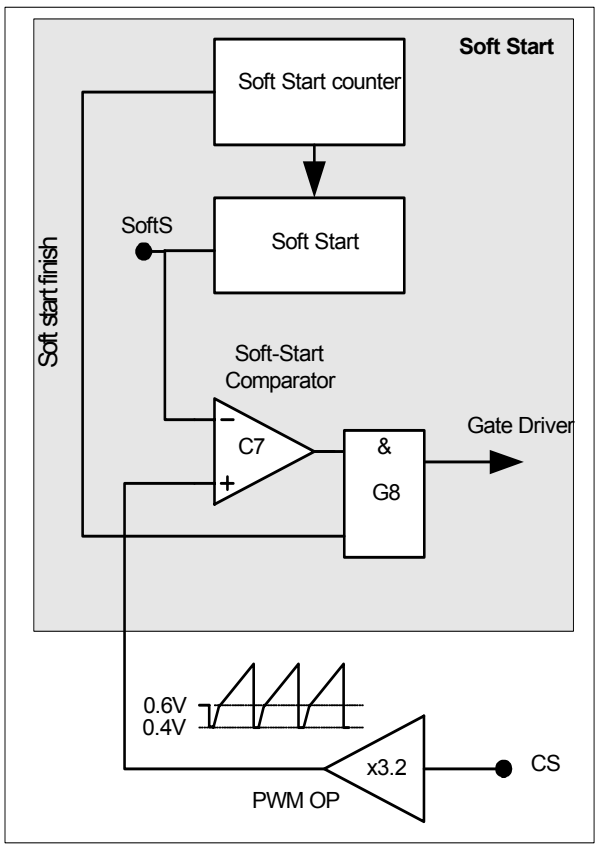


Figure 18 Soft Start

In the Startup Phase, the IC provides a Soft Start period to control the maximum primary current by means of a duty cycle limitation. The Soft start function

is a built-in function and it is controlled by an internal counter.

When the V_{sense} exceeds the on-threshold voltage 2.85V, the IC starts the soft start mode. The function is realized by an internal soft start resistor, an internal current sink and a internal counter. The amplitude of the current sink is controlled by a timer.

The V_{SoftS} voltage is set by the current sinks, a resistor and a counter such that the voltage will increase step wisely with the increase of the counts. Every 0.8ms, the soft start counter would send a signal to the current sink control such that the current sink will decrease gradually and thus the V_{FB} will increase gradually. The soft start will be finished in 12msec. At the end of the soft start period, the current sink will be switched off.

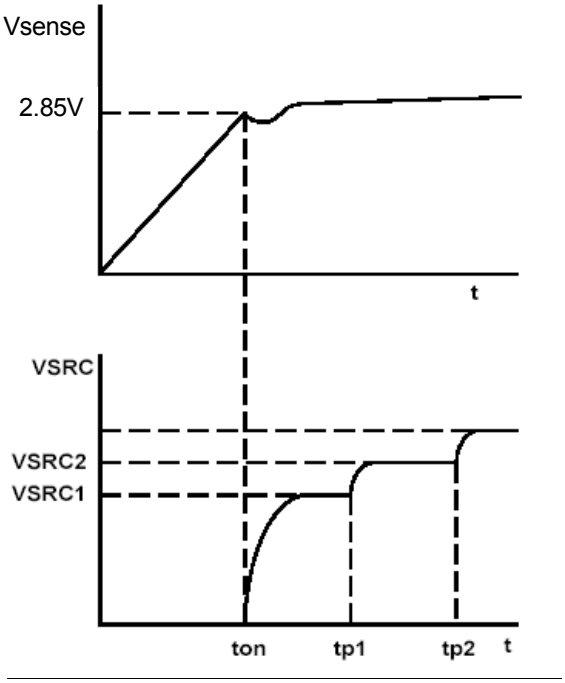


Figure 19 Softstart Phase

During Soft Start phase, the voltage at pin 12 (PWM FB) follows the soft start level with an offset, V_{SoftS} + V_{offset}.

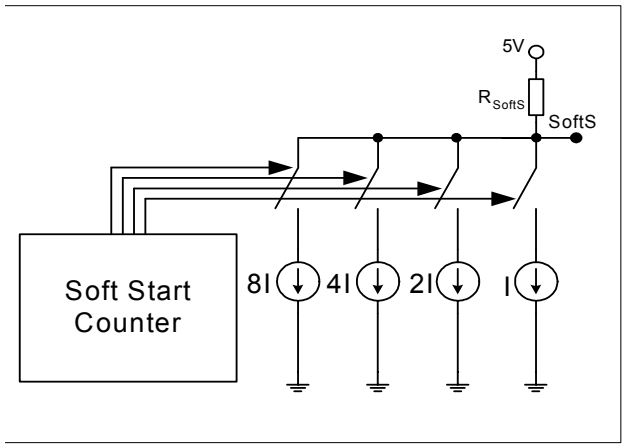


Figure 20 Softstart Circuit

3.5.2 PWM Section

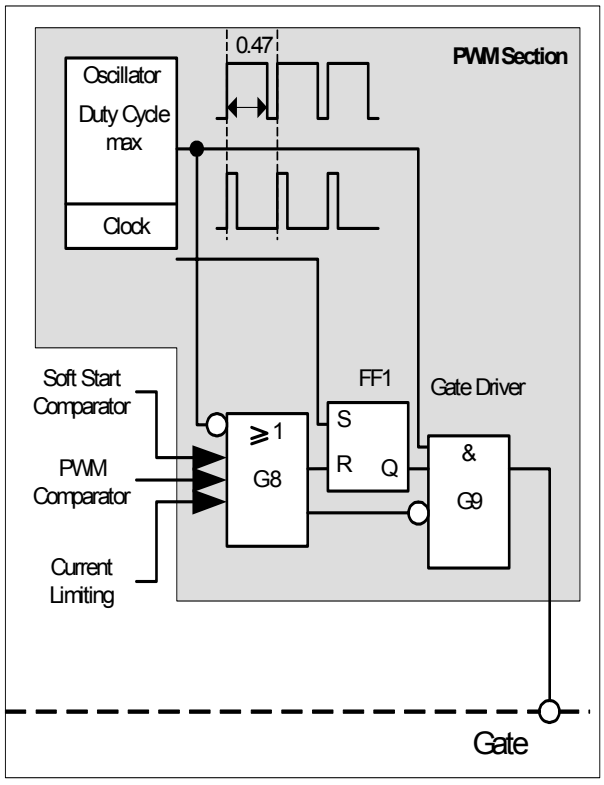


Figure 21 PWM Section

3.5.3 Oscillator

The switching frequency is generated by an oscillator which composes of resistor, capacitor, current source and current sink. The charging and discharging current for the oscillator capacitor are internally trimmed and it can provide a very accurate switching frequency. The ratio of the controlled charge to discharge current is adjusted to a maximum duty cycle of D_{max}=0.47 or 0.60.

If Vout is 330V, the duty cycle will be set back to 0.47.The switching frequency is set to f_{switch} = 130kHz.

3.5.4 PWM-Latch FF1

The output of the oscillator clock will provide continuous pulse to the PWM-Latch which would turn on the external MOS switch. After the PWM-Latch is set, it can be reset by the PWM comparator, the Soft Start comparator or the Current-Limit comparator. When it is in reset mode, the output of the driver is down immediately.

3.5.5 PWM Brown out

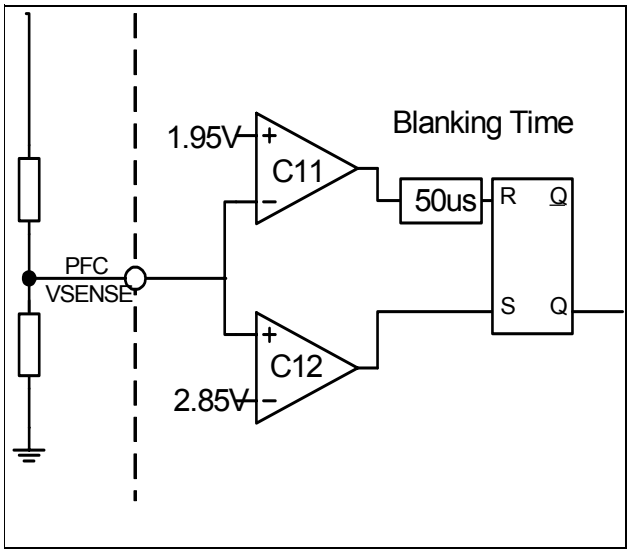


Figure 22 PWM brown out circuit

The voltage of the bus voltage is sensed through the pin 2 (PFC VSENSE). When V_{SENSE} drops to lower than 1.95V, the gate signal will stop. When the V_{SENSE} rises to higher than 2.85V, gate signal will resume again with soft-start (see Figure 23). The blanking time of 50us is added in order to avoid the noise interruption.

3.5.6 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 23) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 8 (PWM OUT) is typically clamped at 15V.

The output is active HIGH and at VCC voltages below the under voltage lockout threshold VCCUVLO, the gate drive is internally pull low to maintain the off state.

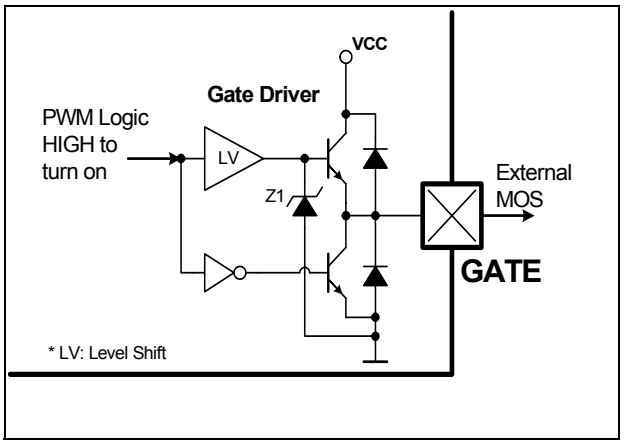


Figure 23 Gate Driver

3.5.7 Current Limiting

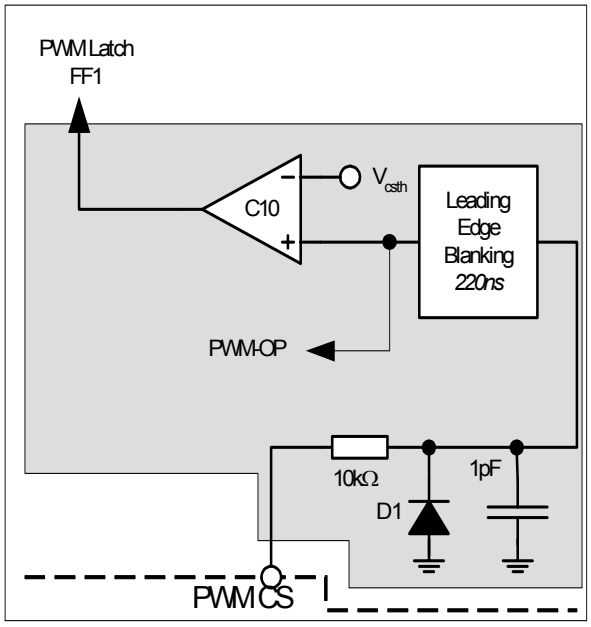


Figure 24 Current Limiting

There is a cycle by cycle peak current limiting operation realized by the Current-Limit comparator C10. The source current of the MOS switch is sensed via an external sense resistor R_{Sense}. By means of R_{Sense} the source current is transformed to a voltage V_{cur_sense} which is fed into the PWM CS pin. If this voltage exceeds the internal threshold voltage V_{csth} the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1.

In order to prevent the current limit from distortions caused by leading edge spikes, a Leading Edge Blanking is integrated into the current sense path before connecting to the PWM-OP.

3.5.8 Leading Edge Blanking

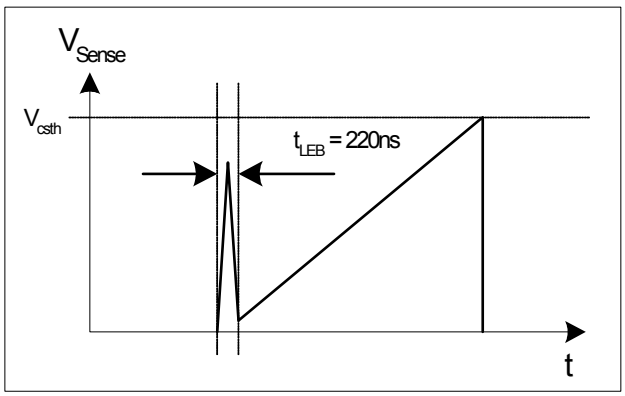


Figure 25 Leading Edge Blanking

Whenever MOS switch is switched on, a leading edge spike is generated due to the primary-side capacitances and the reverse recovery time of secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid a premature termination of the switching pulse, this spike is blanked.

3.5.9 Pre-short Protection

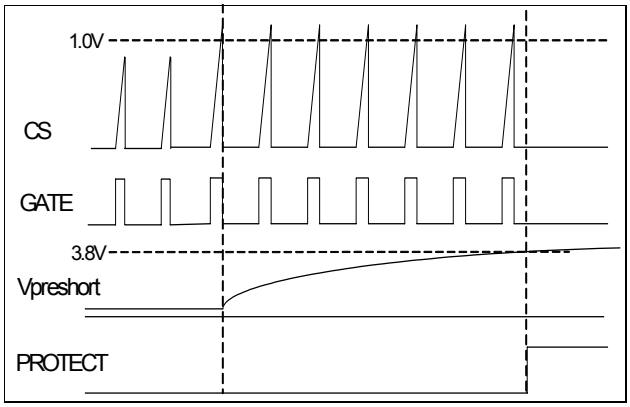


Figure 26 Pre-short Protection

The IC will enter into protection, turning off the gate when voltage at pin 9 (PWM CS) exceed 1.0V for a period set externally through pin 11 (PWM Pre-short). The IC will be resetted when IC exit out of PWM BOP.

3.5.10 External Synchronization

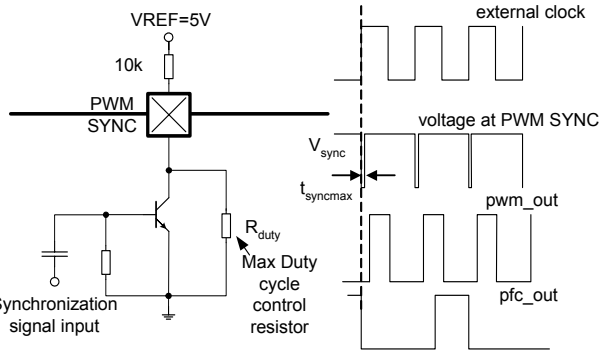


Figure 27 External Synchronization and Max Duty Selection

During External Synchronization, external clock is input by the synchronization signal input. PFC output is kept in synchronization with PWM output in 1:2 ratio. The maximum allowable external sync pulse width off time is 0.5µs.

3.5.11 Max Duty Cycle Selection

Vsync (V)	> 3.0	< 3.0	
Vsense (V)	-	> 2.6	< 2.6
Max Duty Cycle (%)	47	47	60

Figure 28 Max Duty Cycle Selection Table

The maximum duty cycle is selected based on the above setting at the PFC Vsense and PWM SYNC pins.

3.5.12 PWM Slope Compensation

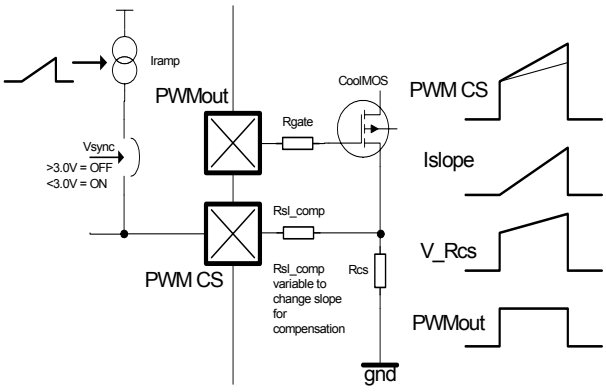


Figure 29 PWM slope compensation

The IC will enter into slope compensation at PWM CS pin when Vsync is less than 3.0V.

3.5.13 PWM External Shut down by Pre-Short

Whenever $V_{Preshort}$ fall below the value set by pin 11 (PWM Pre-short) of 0.4V, the PWM output will be shut down, as shown in Figure 30.

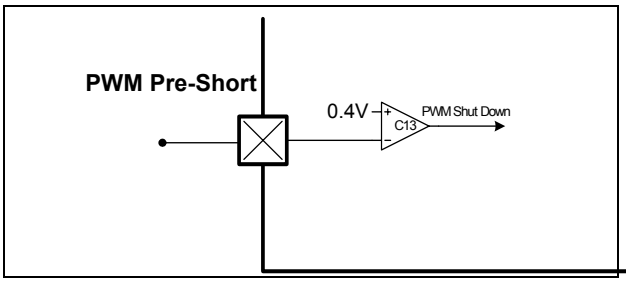


Figure 30 PWM Shut down by Pre-Short

3.5.14 PWM External Voltage Reference

The PWM external voltage reference is generated from an internal trimmed 5V voltage reference. The external voltage reference can source a minimum 12mA current at pin 13 (VREF). To protect this external voltage reference, it is equipped with a foldback characteristic, which will cut down the output current when VREF is shorted to GND. When using this external voltage reference, the total current consumption of this IC which includes this maximum source current must not exceed the maximum operating junction temperature of 125°C.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 5). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{VCC}	-0.3	26	V	
PWM FB Voltage	V_{FB}	-0.3	5.0	V	
PWM CS Voltage	V_{CS}	-0.3	5.0	V	
PWM SYNC Voltage	V_{SYNC}	-0.3	5.0	V	
PWM PRESHORT Voltage	$V_{PRESHORT}$	-0.3	5.0	V	
PFC VINS Voltage	V_{VINS}	-0.3	9.5	V	
PFC VINS Current	I_{VINS}	-1.0	35.0	µA	3)
PFC VINS_HYS Voltage	V_{VINS_HYS}	-0.3	5.0	V	
PFC ICOMP Voltage	V_{ICOMP}	-0.3	5.0	V	
PFC OVP Voltage	V_{OVP}	-0.3	5.0	V	
PFC ISENSE Voltage	V_{ISENSE}	-20	5.0	V	2)
PFC ISENSE Current	I_{ISENSE}	-1.0	1.0	mA	
PFC VSENSE Voltage	V_{VSENSE}	-0.3	5.0	V	
PFC VSENSE Current	I_{VSENSE}	-1.0	1.0	mA	R3>400kΩ
PFC VCOMP Voltage	V_{VCOMP}	-0.3	5.0	V	
External Voltage Reference	V_{VREF}	-0.3	V_{VREF0A}	V	
GATE Voltage	V_{GATE}	-0.3	17	V	Clamped at 15V if driven internally.
Junction Temperature	T_j	-40	150	°C	Controller
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}		90	K/W	PG-DIP-16-4
Thermal Resistance Junction-Ambient	R_{thJA}	-	125	K/W	PG-DSO-16-17
ESD Capability	V_{ESD}	-	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

2) Absolute ISENSE current should not be exceeded

3) Absolute VINS current should not be exceeded

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	25	V	V_{VCCmax} is limited by T_{jcon}
Junction Temperature of Controller	T_{jCon}	-25	125	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18V, internal clock frequency is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Current with Inactive Gate	$I_{VCCsup1}$	-	6	-	mA	
Supply Current with Active Gate	$I_{VCCsup2}$	-	10	22	mA	V_{FB} = 3.0V with VREF supply 0mA Gate Load = 1nF
Operating Current during Standby	$I_{CCStdby}$	-	2.0	-	mA	V_{VSENSE}= 0V
Start Up Current Before V_{CCon}	$I_{CCstart}$	-	1.3	-	mA	V_{VCC}=10V
VCC Turn-On Threshold VCC Turn-Off Threshold VCC Turn-On/Off Hysteresis	V_{VCCon} V_{VCCoff} V_{VCChys}	11.5 10.5 0.60	12.0 11.0 1.00	12.9 11.9 1.35	V V V	

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Reference Voltage	V_{VREF0A}	4.85	5.00	5.20	V	I_{VREF}=-0mA
Load Regulation	$\Delta V_{VREF12mA}$	-	-	252	mV	I_{VREF}=-12mA[1)]
Line Regulation	$\Delta V_{VREFDVCC}$	-	-	50	mV	ΔV_{CC}=3V
Maximum Source Current	I_{VREF}	12	-	-	mA	

1) max pulling current depends on max operating junction temperature

4.3.3 PWM Control Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PWM-OP Gain	A_V	3.0	3.2	3.6		
Max. Level of Voltage Ramp	$V_{Max-Ramp}$	-	0.6	-	V	
V_{FB} Operating Range Min Level	V_{FBmin}	0.3	0.4	-	V	
V_{FB} Operating Range Max level	V_{FBmax}	-	-	4.3	V	CS=1V limited by Comparator C10[1)]
Feedback Pull-Up Resistor	R_{FB}	11.3	17.4	22.7	kΩ	

1) This parameter is not subject to production test - verified by design/characterization

4.3.4 PWM Brown Out Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PWM BrownOut ON Threshold	V_{PWM_BOon}	1.87	1.95	2.03	V	
PWM BrownOut OFF Threshold	V_{PWM_BOoff}	2.75	2.85	2.95	V	
Blanking time for BrownOut Turn_On	t_{bkPWM_BOon}	-	50	-	µs	

4.3.5 PWM Current Limiting

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation	V_{csth}	0.95	1.00	1.05	V	
Leading Edge Blanking	t_{LEB}	-	220	-	ns	
CS Input Bias Current	I_{CSbias}	-1.0	-0.2	0	µA	V_{CS} = 0V

4.3.6 PWM Slope Compensation

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current for Slope Compenation	I_{slope}	85	150	215	µA	at f_{PWM}=70kHz, 60% Max Duty Cycle

4.3.7 PWM Timing Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft Start Timing	t_{SS}	-	12	-	ms	
Fixed Oscillator Frequency	f_{delta}	110		140	kHz	
Synchronizable range		70		150	kHz	
Max. Duty Cycle 2 Internal Free Run	$D_{max2INT}$	56.5	59.0	61.5	%	Vsync < 3.0V Vsense < 2.6V
Max. Duty Cycle 1 Internal Free Run	$D_{max1INT}$	44.5	47.0	49.5	%	Vsync < 3.0V Vsense > 2.6V
Max. Duty Cycle 2 (70kHz) External Synchronization	$D_{max2EXT70}$	51.0	57.0	63.0	%	at f_{PWM}=70kHz Vsync < 3.0V Vsense < 2.6V
Max. Duty Cycle 1 (70kHz) External Synchronization	$D_{max1EXT70}$	37.0	43.0	47.0	%	at f_{PWM}=70kHz Vsync < 3.0V Vsense > 2.6V
Max. Duty Cycle 2 (150kHz) External Synchronization	$D_{max2EXT150}$	54.0	60.0	66.0	%	at f_{PWM}=150kHz Vsync < 3.0V Vsense < 2.6V
Max. Duty Cycle 1 (150kHz) External Synchronization	$D_{max1EXT150}$	39.5	45.0	49.5	%	at f_{PWM}=150kHz Vsync < 3.0V Vsense > 2.6V
Min. Duty Cycle	D_{min}	0	-	-	%	V_{FB} < 0.3V
Max. Allowable External Sync Pulse Width off Time	$t_{syncmax}$	-	-	0.5	µs	
Min. Allowable External Sync Pulse Width off Time	$t_{syncmin}$	0.35	-	-	µs	

4.3.8 PFC Timing Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Oscillator Frequency	f_{delta}	55		70	kHz	
Max. Duty Cycle	D_{MAX}	93	95	99	%	
Min. Duty Cycle	D_{MIN}			0	%	V_{VCOMP}= 0V, V_{VSENSE}= 3V V_{ICOMP}= 4.3V
Min. Off Time	T_{OFFMIN}	120	320	500	ns	V_{VCOMP}= 3V, V_{VSENSE}= 3V V_{ISENSE}= 0.1V

4.3.9 PFC Current Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA2 Transconductance Gain	Gm_{OTA2}	0.7	1.0	1.2	mS	At Temp = 25°C
OTA2 Output Linear Range	I_{OTA2}		+/- 50		µA	
ICOMP Voltage during OLP	V_{ICOMPF}	4.0	4.5	5.1	V	V_{VSENSE}= 0.5V

4.3.10 PFC Voltage Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA1 Reference Voltage	V_{OTA1}	2.92	3.00	3.08	V	Trimmed Reference measured at PFC VSENSE
OTA1 Transconductance Gain	Gm_{OTA1}	26	40	52	µS	
OTA1 Max. Source Current Under Normal Operation	I_{OTA1SO}	19	30	39	µA	V_{VSENSE}= 2V V_{VCOMP}= 3V
OTA1 Max. Sink Current Under Normal Operation	I_{OTA1SK}	18	29	38	µA	V_{VSENSE}= 4V V_{VCOMP}= 3V
Enhanced Dynamic Response VSENSE High Threshold VSENSE Low Threshold	V_{Hi} V_{Lo}	3.10 2.76	3.18 2.85	3.27 2.94	V V	
VSENSE Input Bias Current at 3V	I_{VSEN3V}	0	-	1.5	µA	V_{VSENSE}= 3V
VSENSE Input Bias Current at 1V	I_{VSEN1V}	0	-	1	µA	V_{VSENSE}= 1V
VCOMP Voltage during OLP	V_{VCOMPF}	0.40	0.67	1.00	V	V_{VSENSE}= 0.5V I_{VCOMP}= 0.5mA

4.3.11 PFC Brown Out Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PFC Brown Out Threshold	V_{VINS}	1.18	1.25	1.32	V	
VINS Input Bias Current at 1.25V	I_{VINS}	-0.5	0	0.5	µA	V_{VINS}= 1.25V
C5 Transconductance Gain	Gm_{C5}	0.5	1.0	1.5	mS	
VINS_HYS Output Sink / Source Current	I_{VINS_HYS}	90	-	-	µA	V_{VINS_HYS} = 2.5V
Blanking time for Turn_On	t_{PFC_BOon}	-	30	-	µs	

4.3.12 System Protection Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PWM Preshort CS	V_{CS}	0.95	1.00	1.05	V	
PWM Pre-short Timing	$t_{Preshort}$	-	20	-	ms	with a 0.22µF capacitor
PWM Pre-short IC Shut Down Threshold	V_{Pre_th}	3.7	3.9	4.1	V	
PWM Pre-short Internal Charging Current	I_{Pre_Charge}	18	28	38	µA	$V_{Preshort}$= 1V
PWM Pre-short Internal Discharging Current	$I_{Pre\_Discharge}$	55	85	115	µA	$V_{Preshort}$= 3V
PFC Open Loop Protection (OLP) VSENSE Threshold	V_{OLP}	0.54	0.59	0.64	V	
PFC Peak Current Limitation (PCL) ISENSE Threshold	V_{PCL}	-0.72	-0.65	-0.58	V	
PWM External Shut Down Threshold	V_{Pre_Shd}	0.3	0.4	0.5	V	Threshold at PWM Preshort
PFC Output Over-Voltage Protection (OVP)	V_{OVP}	3.05	3.15	3.27	V	
PFC Output Over-Voltage Hystersis (OVPHYS)	V_{OVPHYS}	-	150	-	mV	

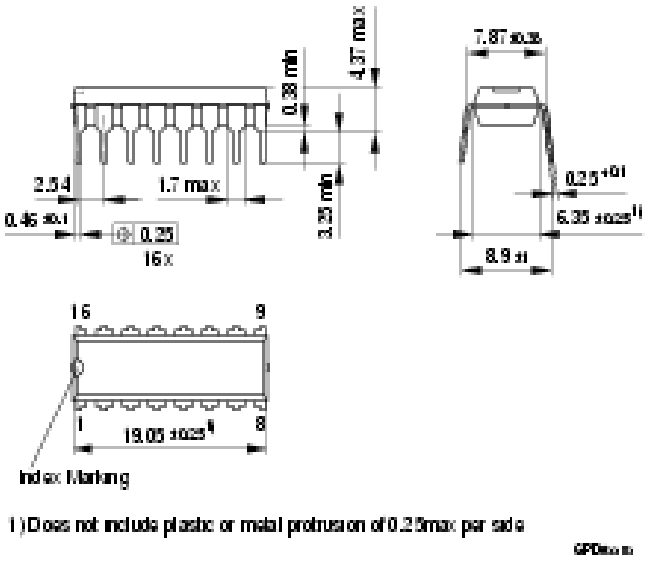
4.3.13 Driver Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	V_{GATEL}	-	-	1.2	V	V_{CC} = 10V I_{GATE} = 5 mA
		-	-	1.5	V	V_{CC} = 10V I_{GATE} = 20 mA
		-	0.4	-	V	I_{GATE} = 0 A
		-		1.4	V	I_{GATE} = 20 mA
		-0.2	0.2	-	V	I_{GATE} = -20 mA
GATE High Voltage	V_{GATEH}	-	14.8	-	V	V_{CC} = 25V C_L = 4.7nF
		-	12.2	-	V	V_{CC} = 15V C_L = 4.7nF
		-	7.5	-	V	V_{CC} = V_{VCCoff} + 0.2V C_L = 4.7nF
GATE Rise Time	t_r	-	60	-	ns	V_{Gate} = 20 ~ 80 %V_{GATEH} C_L = 4.7nF
GATE Fall Time	t_f	-	50	-	ns	V_{Gate} = 80 ~ 20 %V_{GATEH} C_L = 4.7nF
GATE Current, Peak, Rising Edge	I_{GATE}	-	-	-1.5	A	C_L = 4.7nF[1)]
GATE Current, Peak, Falling Edge	I_{GATE}	2.0	-	-	A	C_L = 4.7nF[1)]

1) Design characteristics (not meant for production testing)

5 Outline Dimension

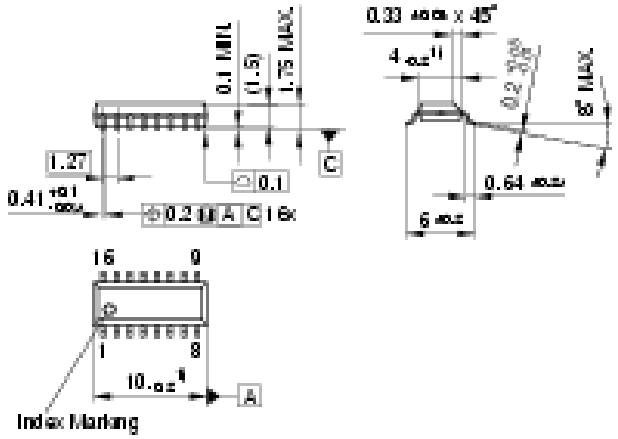
PG-DIP-16-4



Dimensions in mm

Figure 31 PG-DIP-16-4 Outline Dimension

PG-DSO-16-17
(Plastic Dual Small Outline Package)



Dimensions in mm

Figure 32 PG-DSO-16-17 Outline Dimension

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

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