Block Diagram

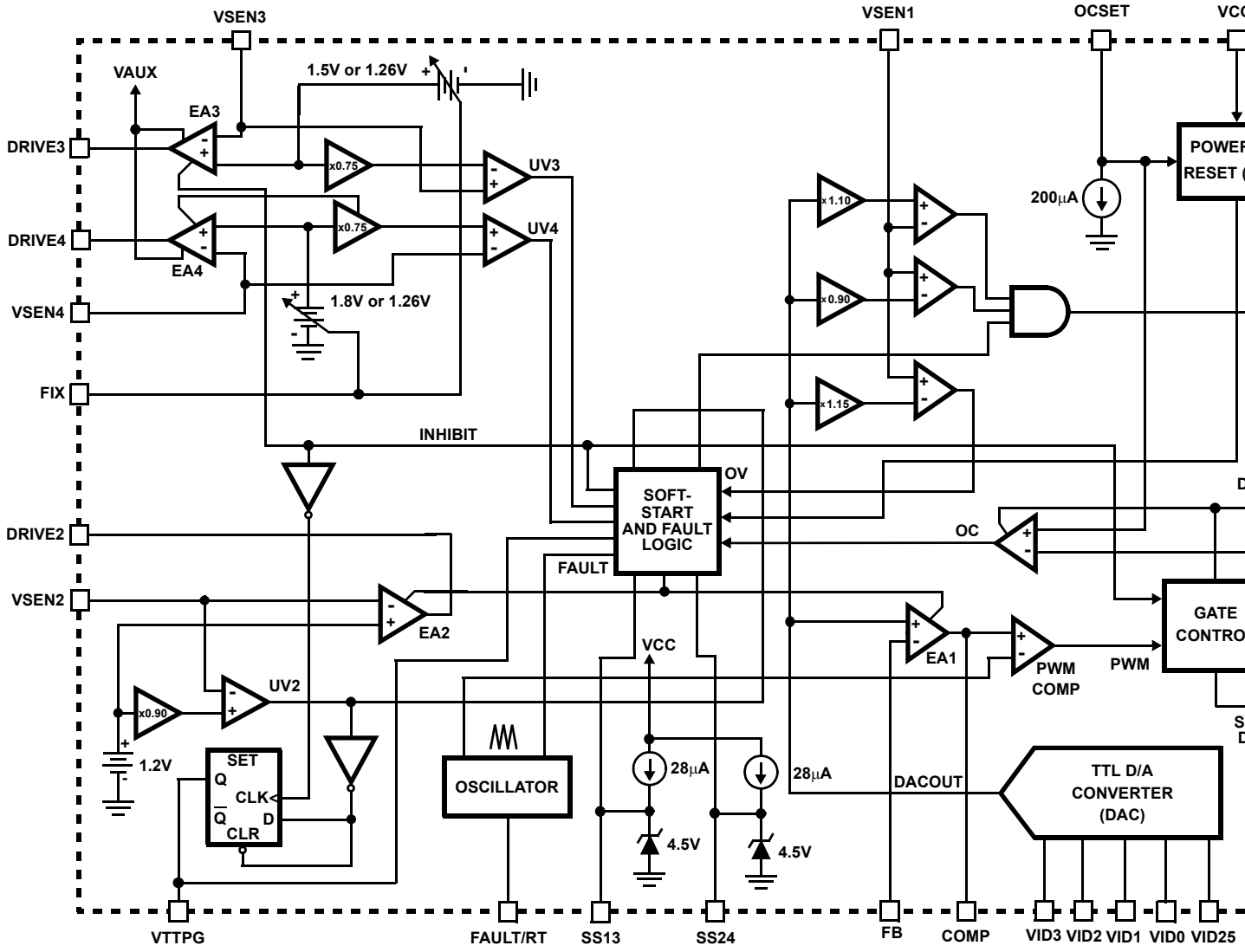


FIGURE 1.

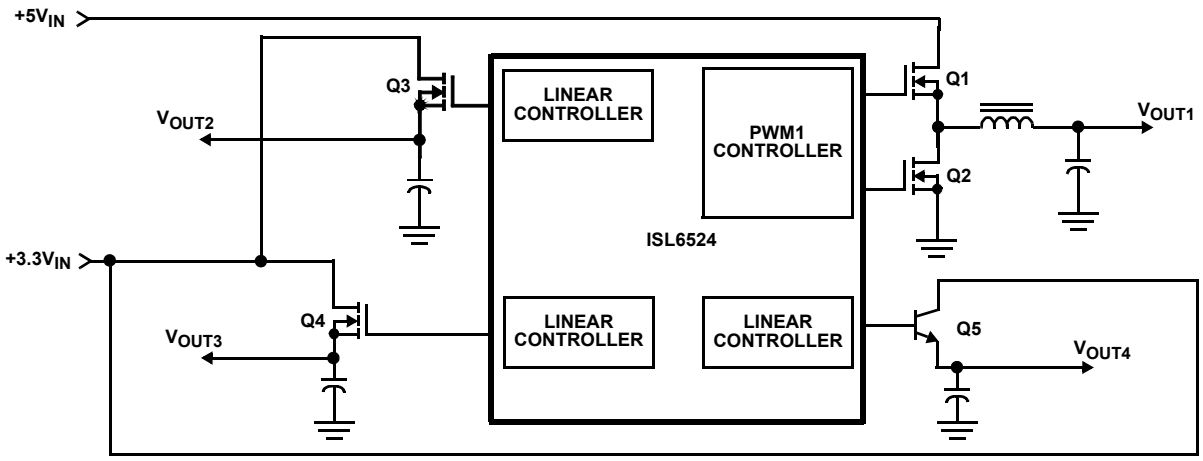


FIGURE 2. SIMPLIFIED POWER SYSTEM DIAGRAM

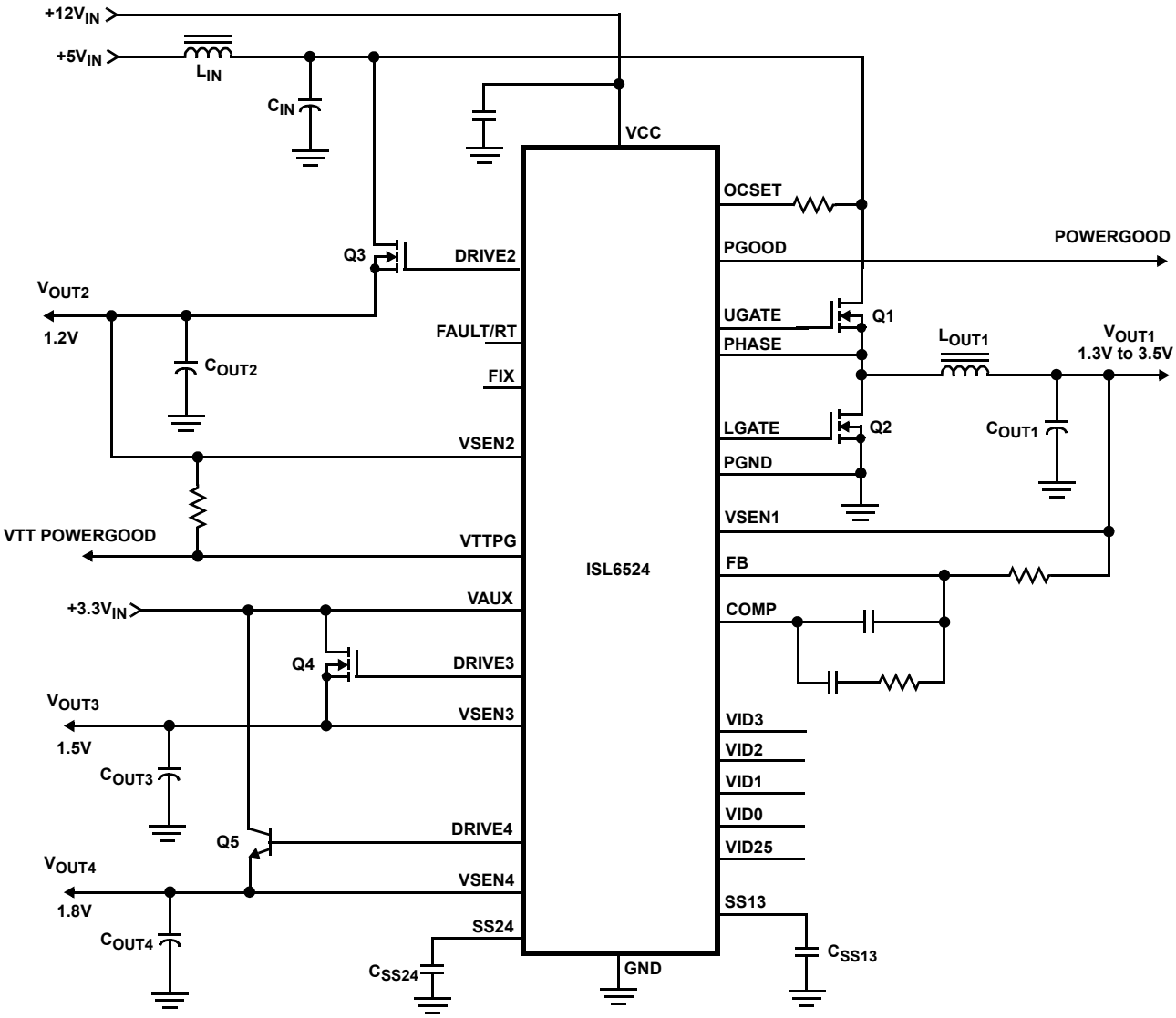


FIGURE 3. TYPICAL APPLICATION

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +15V
PGOOD, RT/FAULT, DRIVE, PHASE, and
GATE Voltage . . . . . GND - 0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . . GND -0.3V to 7V
ESD Classification . . . . . Class 1

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . +12V ±10%
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC}	UGATE, LGATE, DRIVE2, DRIVE3, and DRIVE4 Open	-	9	-	mA
POWER-ON RESET						
Rising VCC Threshold			-	-	10.4	V
Falling VCC Threshold			8.2	-	-	V
Rising VAUX Threshold			-	2.5	-	V
VAUX Threshold Hysteresis			-	0.5	-	V
Rising V_{OCSET} Threshold			-	1.26	-	V
OSCILLATOR						
Free Running Frequency	F_{OSC}		185	200	215	kHz
Total Variation		6kΩ < RT to GND < 200kΩ; Note 2	-15	-	+15	%
Ramp Amplitude	ΔV_{OSC}		-	1.9	-	V_{P-P}
DAC REFERENCE						
DAC (VID25-VID3) Input Low Voltage					0.8	V
DAC (VID25-VID3) Input High Voltage			2.0			V
DACOUT Voltage Accuracy			-1.0	-	+1.0	%
LINEAR REGULATORS (V_{OUT2}, V_{OUT3}, AND V_{OUT4})						
Regulation Tolerance			-	3	-	%
VSEN3 Regulation Voltage	$VREG_3$	FIX = 0V	-	1.26	-	V
VSEN2 Regulation Voltage	$VREG_2$		-	1.2	-	V
VSEN3 Regulation Voltage	$VREG_3$	FIX = Open	-	1.5	-	V
VSEN4 Regulation Voltage	$VREG_4$	FIX = Open	-	1.8	-	V
VSEN3, 4 Undervoltage Level	VSEN3, 4_{UV}	VSEN3, 4 Rising	-	75	-	%
VSEN3, 4 Undervoltage Hysteresis		VSEN3, 4 Falling		7		%
Output Drive Current		VAUX-$V_{DRIVE2,3,4}$ > 0.6V	20	40	-	mA
SYNCHRONOUS PWM CONTROLLER ERROR AMPLIFIER						
DC Gain		Note 2	-	88	-	dB

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP	Note 2	-	15	-	MHz
Slew Rate	SR	COMP = 10pF, Note 2	-	6	-	V/μs
PWM CONTROLLERS GATE DRIVERS						
UGATE Source	I_{UGATE}	VCC = 12V, V_{UGATE} = 6V	-	1	-	A
UGATE Sink	R_{UGATE}	$V_{GATE-PHASE}$ = 1V	-	1.7	3.5	Ω
LGATE Source	I_{LGATE}	VCC = 12V, V_{LGATE} = 1V	-	1	-	A
LGATE Sink	R_{LGATE}	V_{LGATE} = 1V	-	1.4	3.0	Ω
PROTECTION						
FAULT Sourcing Current	I_{OVP}	$V_{FAULT/RT}$ = 2.0V	-	8.5	-	mA
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V_{DC}	170	200	230	μA
Soft-Start Current	$I_{SS13,24}$	$V_{SS13,24}$ = 2.0V_{DC}	-	28	-	μA
POWER GOOD						
VSEN1 Upper Threshold (VSEN1/DACOUT)		VSEN1 Rising	108	-	110	%
VSEN1 Undervoltage (VSEN1/DACOUT)		VSEN1 Rising	92	-	94	%
VSEN1 Hysteresis (VSEN1/DACOUT)		VSEN1 Falling	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	-	0.8	V
VSEN2 Undervoltage		VSEN2 Rising		1.08		V
VSEN2 Hysteresis		VSEN2 Falling	-	48	-	mV
VTTPG Voltage Low	V_{VTTPG}	I_{VTTPG} = -4mA	-	-	0.8	V

NOTE:

2. Guaranteed by design

Typical Performance Curves

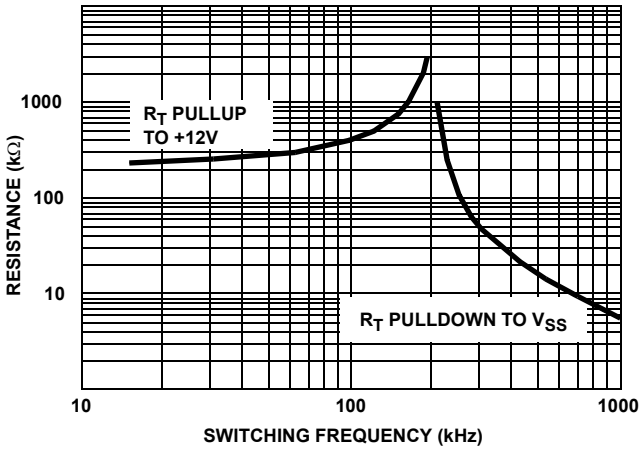


FIGURE 4. R_T RESISTANCE vs FREQUENCY

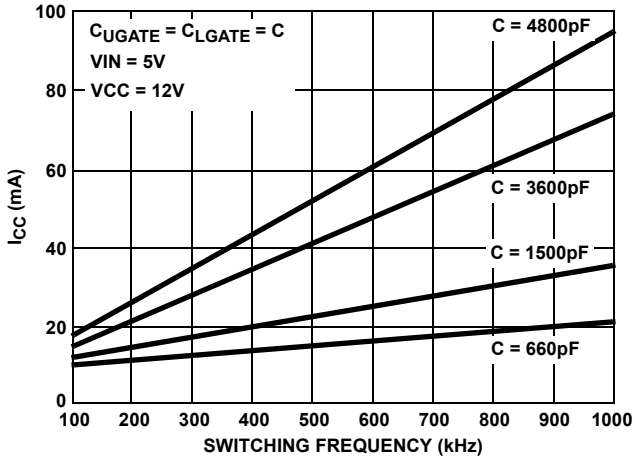


FIGURE 5. BIAS SUPPLY CURRENT vs FREQUENCY

Functional Pin Descriptions

VCC (Pin 28)

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGND (Pin 24)

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

VAUX (Pin 16)

Connect this pin to the ATX 3.3V output. The voltage present at this pin is monitored for sequencing purposes. This pin provides the necessary base bias for the NPN pass transistors, as well as the current sunk through the 5kW VID pull-up resistors.

SS13 (Pin 13)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28mA current source, sets the soft-start interval of the synchronous switching converter (V_{OUT1}) and the AGP regulator (V_{OUT3}). A VTTPG high signal is also delayed by the time interval required by the charging of this capacitor from 0V to 1.25V (see Soft-Start details).

SS24 (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28mA current source, sets the soft-start interval of the V_{OUT2} regulator. Pulling this pin below 0.8V induces a chip reset (POR) and shutdown.

VTTPG (Pin 9)

VTTPG is an open collector output used to indicate the status of the V_{OUT2} regulator output voltage. This pin is pulled low when the V_{OUT2} output is below the undervoltage threshold or when the SS13 pin is below 1.25V.

PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage or when any of the other outputs is below its undervoltage threshold.

VID3, VID2, VID1, VID0, VID25 (Pins 3-7)

VID3-25 are the TTL-compatible input pins to the 5-bit DAC. The logic states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the microprocessor core converter output voltage (V_{OUT1}), as well as the corresponding PGOOD and OVP thresholds. Each VID pin is connected to the VAUX pin through a 5kW pull-up resistor.

OCSET (Pin 23)

Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET. R_{OCSET}, an internal 200mA current source (I_{OCSET}), and the upper MOSFET's on-resistance ($r_{DS(ON)}$) set the converter overcurrent (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An overcurrent trip cycles the soft-start function.

The voltage at OCSET pin is monitored for power-on reset (POR) purposes.

PHASE (Pin 26)

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for overcurrent protection.

UGATE (Pin 27)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

LGATE (Pin 25)

Connect LGATE to the synchronous PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

COMP and FB (Pins 20, 21)

COMP and FB are the available external pins of the synchronous PWM regulator error amplifier. The FB pin is the inverting input of the error amplifier. Similarly, the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

VSEN1 (Pin 22)

This pin is connected to the synchronous PWM converters' output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status.

DRIVE2 (Pin 1)

Connect this pin to the gate/base of a N-type external pass transistor (MOSFET or bipolar). This pin provides the drive for the 1.2V regulator's pass transistor.

VSEN2 (Pin 11)

Connect this pin to the output of the standard buck PWM regulator. The voltage at this pin is regulated to a 1.2V level. This pin is also monitored for undervoltage events.

FIX (Pin 2)

Grounding this pin bypasses the internal resistor dividers that set the output voltage of the 1.5V and 1.8V linear regulators. This way, the output voltage of the two regulators can be adjusted from 1.26V up to the input voltage (+3.3V or +5V;

VOUT4 can only be set from 1.7V up) by way of an external resistor divider connected at the corresponding VSEN pin. The new output voltage set by the external resistor divider can be determined using the following formula:

$$V_{OUT} = 1.265V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

where R_{OUT} is the resistor connected from VSEN to the output of the regulator, and R_{GND} is the resistor connected from VSEN to ground. Left open, the FIX pin is pulled high, enabling fixed output voltage operation.

DRIVE3 (Pin 18)

Connect this pin to the gate/base of a N-type external pass transistor (MOSFET or bipolar). This pin provides the drive for the 1.5V regulator's pass transistor.

VSEN3 (Pin 19)

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for undervoltage events.

DRIVE4 (Pin 15)

Connect this pin to the base of an external bipolar transistor. This pin provides the drive for the 1.8V regulator's pass transistor.

VSEN4 (Pin 14)

Connect this pin to the output of the linear 1.8V regulator. This pin is monitored for undervoltage events.

FAULT/RT (Pin 10)

This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs \approx 200kHz + \frac{5 \times 10^6}{R_{T(k\Omega)}} \quad (R_T \text{ to GND})$$

Conversely, connecting a resistor from this pin to VCC reduces the switching frequency according to the following equation:

$$Fs \approx 200kHz - \frac{4 \times 10^7}{R_{T(k\Omega)}} \quad (R_T \text{ to 12V})$$

Nominally, the voltage at this pin is 1.26V. In the event of an overvoltage or overcurrent condition, this pin is internally pulled to VCC.

Description

Operation

The ISL6524 monitors and precisely controls 4 output voltage levels (Refer to Figures 1, 2, 3). It is designed for microprocessor computer applications with 3.3V, 5V, and 12V bias input from an ATX power supply. The IC has one PWM and three linear controllers. The PWM controller is designed to regulate the microprocessor core voltage (V_{OUT1}). The PWM controller drives 2 MOSFETs (Q1 and Q2) in a synchronous-rectified buck converter configuration and regulates the core voltage to a level programmed by the 5-bit digital-to-analog converter (DAC). The first linear controller (EA2) is designed to provide the AGTL+ bus voltage (V_{OUT2}) by driving a MOSFET (Q3) pass element to regulate the output voltage to a level of 1.2V. The remaining two linear controllers (EA3 and EA4) supply the 1.5V advanced graphics port (AGP) bus power (V_{OUT3}) and the 1.8V chip set core power (V_{OUT4}).

Initialization

The ISL6524 automatically initializes in ATX-based systems upon receipt of input power. The Power-On Reset (POR) function continually monitors the input supply voltages. The POR monitors the bias voltage ($+12V_{IN}$) at the VCC pin, the 5V input voltage ($+5V_{IN}$) at the OCSET pin, and the 3.3V input voltage ($+3.3V_{IN}$) at the VAUX pin. The normal level on OCSET is equal to $+5V_{IN}$ less a fixed voltage drop (see overcurrent protection). The POR function initiates soft-start operation after all supply voltages exceed their POR thresholds.

Soft-Start

The 1.8V supply designed to power the chip set (OUT4), cannot lag the ATX 3.3V by more than 2V, at any time. To meet this special requirement, the linear block controlling this output operates independently of the chip's power-on reset. Thus, DRIVE4 is driven to raise the OUT4 voltage before the input supplies reach their POR levels. As seen in Figure 6, at time T0 the power is turned on and the input supplies ramp up. Immediately following, OUT4 is also ramped up, lagging the ATX 3.3V by about 1.8V. At time T1, the POR function initiates the SS24 soft-start sequence. Initially, the voltage on the SS24 pin rapidly increases to approximately 1V (this minimizes the soft-start interval). Then, an internal 28mA current source charges an external capacitor (C_{SS24}) on the SS24 pin to about 4.5V. As the SS24 voltage increases, the EA2 error amplifier drives Q3 to provide a smooth transition to the final set voltage. The OUT4 reference (clamped to SS24) increasing past the intermediary level, established based on the ATX 3.3V presence at the VAUX pin, brings the output in regulation soon after T2.

As OUT2 increases past the 90% power-good level, the second soft-start (SS13) is released. Between T2 and T3, the SS13 pin voltage ramps from 0V to the valley of the oscillator's triangle wave (at 1.25V). Contingent upon OUT2 remaining above 1.08V, the first PWM pulse on PHASE1 triggers the VTTPG pin to go high. The oscillator's triangular wave form is compared to the clamped error amplifier output voltage. As the SS13 pin voltage increases, the pulse-width on the PHASE1 pin increases, bringing the OUT1 output within regulation limits. Similarly, the SS13 voltage clamps the reference voltage for OUT3, enabling a controlled output voltage ramp-up. At time T4, all output voltages are within power-good limits, situation reported by the PGOOD pin going high.

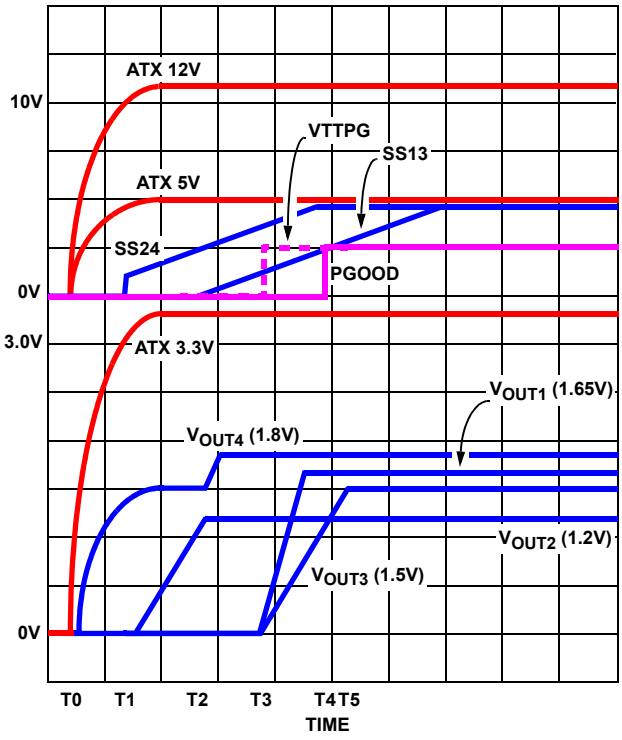


FIGURE 6. SOFT-START INTERVAL

The T2 to T3 time interval is dependent upon the value of C_{SS13}. The same capacitor is also responsible for the ramp-up time of the OUT1 and OUT3 voltages. If selecting a different capacitor then recommended in the circuit application literature, consider the effects the different value will have on the ramp-up time and inrush currents of the OUT1 and OUT3 outputs.

Fault Protection

All four outputs are monitored and protected against extreme overload. The chip's response to an output overload is selective, depending on the faulting output.

An overvoltage on V_{OUT1} output (VSEN1) disables outputs 1, 2, and 3, and latches the IC off. An undervoltage on V_{OUT4} output latches the IC off. A single overcurrent event on output 1, or an undervoltage event on output 2 or 3, increments the respective fault counters and triggers a shutdown of outputs 1, 2, and 3, followed by a soft-start re-start. After three consecutive fault events on either counter, the chip is latched off. Removal of bias power resets both the fault latch and the counters. Both counters are also reset by a successful start-up of all the outputs.

Figure 6 shows a simplified schematic of the fault logic. The overcurrent latches are set dependent upon the states of the overcurrent (OC1), output 2 and 3 undervoltage (UV2, UV3) and the soft-start signals (SS13, SS24). Window comparators monitor the SS pins and indicate when the respective C_{SS} pins are fully charged to above 4.0V (UP signals). An undervoltage on either linear output (VSEN2, VSEN3, or VSEN4) is ignored until the respective UP signal goes high. This allows V_{OUT3} and V_{OUT4} to increase without fault at start-up. Following an overcurrent event (OC1, UV2, or UV3 event), bringing the SS24 pin below 0.8V resets the overcurrent latch and generates a soft-started ramp-up of the outputs 1, 2, and 3.

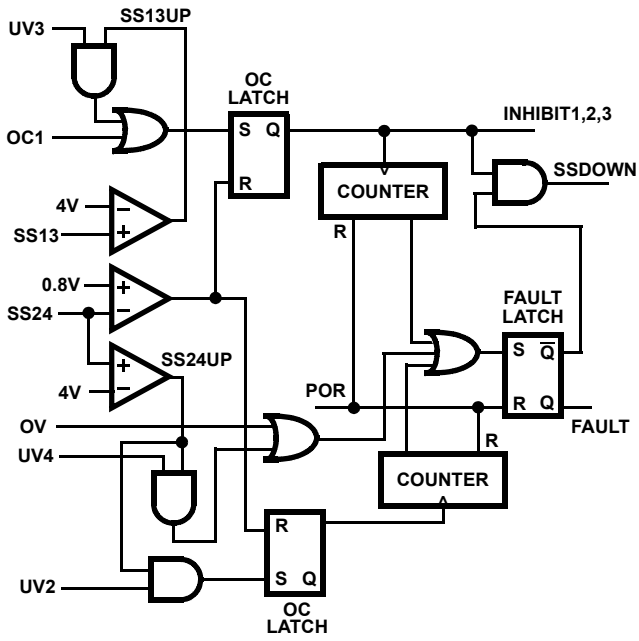


FIGURE 7. FAULT LOGIC - SIMPLIFIED SCHEMATIC

OUT1 Overvoltage Protection

The overvoltage circuit provides protection during the initial application of power. For voltages on the VCC pin below the power-on reset level (and above ~4V), the output level is monitored for voltages above 1.3V. Should VSEN1 exceed this level, the lower MOSFET, Q2, is driven on.

Overcurrent Protection

All outputs are protected against excessive overcurrents. The PWM controller uses the upper MOSFET's on-resistance, $r_{DS(ON)}$ to monitor the current for protection against a shorted output. All linear regulators monitor their respective VSEN pins for undervoltage to protect against excessive currents.

Figure 8 illustrates the overcurrent protection with an overload on OUT1. The overload is applied at T0 and the current increases through the inductor (L_{OUT1}). At time T1, the OC1 comparator trips when the voltage across Q1 ($i_D \cdot r_{DS(ON)}$) exceeds the level programmed by R_{OCSET}. This inhibits outputs 1, 2, and 3, discharges the soft-start capacitor C_{SS24} with 28mA current sink, and increments the counter. Soft-start capacitor C_{SS13} is quickly discharged. C_{SS13} starts ramping up at T2 and initiates a new soft-start cycle. With OUT2 still overloaded, the inductor current increases to trip the overcurrent comparator. Again, this inhibits the outputs, but the C_{SS24} soft-start voltage continues increasing to above

4.0V before discharging. Soft-start capacitor C_{SS13} is, again, quickly discharged. The counter increments to 2. The soft-start cycle repeats at T3 and trips the overcurrent comparator. The SS24 pin voltage increases to above 4.0V at T4 and the counter increments to 3. This sets the fault latch to disable the converter.

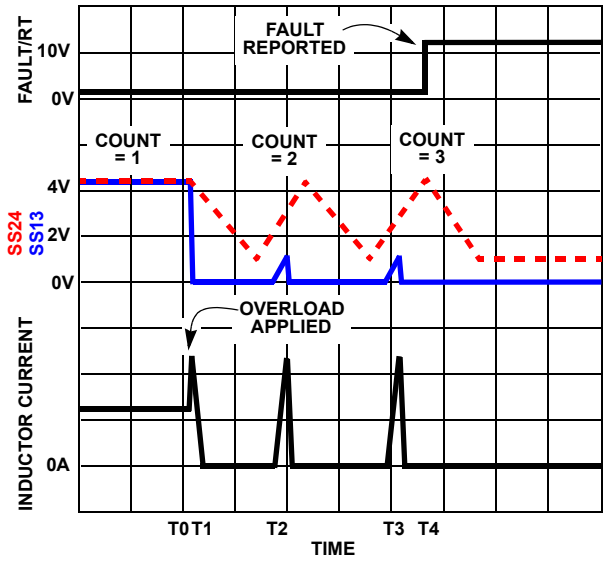


FIGURE 8. OVERCURRENT OPERATION

The three linear controllers monitor their respective VSEN pins for undervoltage. Should excessive currents cause VSEN3 or VSEN4 to fall below the linear undervoltage threshold, the respective UV signals set the OC latch or the FAULT latch, providing respective C_{SS} capacitors are fully charged. Blanking the UV signals during the C_{SS} charge interval allows the linear outputs to build above the undervoltage threshold during normal operation. Cycling the bias input power off then on resets the counter and the fault latch.

An external resistor (R_{OCSET}) programs the overcurrent trip level for the PWM converter. As shown in Figure 9, the internal 200mA current sink (I_{OCSET}) develops a voltage across R_{OCSET} (V_{SET}) that is referenced to V_{IN}. The DRIVE signal enables the overcurrent comparator (OC). When the voltage across the upper MOSFET ($V_{DS(ON)}$) exceeds V_{SET}, the overcurrent comparator trips to set the overcurrent latch. Both V_{SET} and V_{DS} are referenced to V_{IN} and a small capacitor across R_{OCSET} helps V_{OCSET} track the variations of V_{IN} due to MOSFET switching. The overcurrent function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

The OC trip point varies with MOSFET's $r_{DS(ON)}$ temperature variations. To avoid overcurrent tripping in the normal operating load range, determine the ROCSET resistor value from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{OCSET} from the specification table
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + (DI)/2$, where DI is the output inductor ripple current.

For an equation for the ripple current see the section under component guidelines titled 'Output Inductor Selection'.

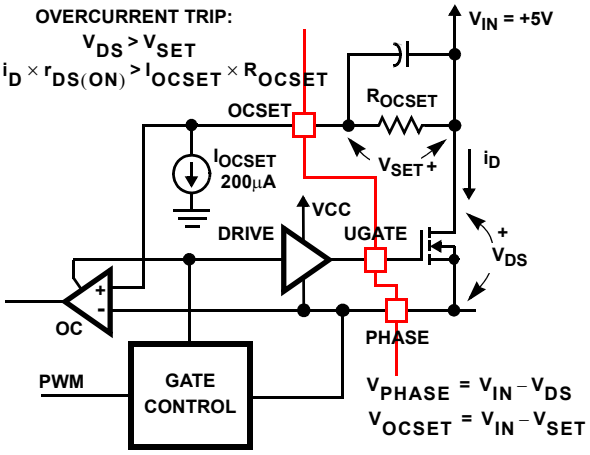


FIGURE 9. OVERCURRENT DETECTION

OUT1 Voltage Program

The output voltage of the PWM converter is programmed to discrete levels between 1.050V and 1.825V. This output (OUT1) is designed to supply the core voltage of Intel's advanced microprocessors. The voltage identification (VID) pins program an internal voltage reference (DACOUT) with a TTL-compatible 5-bit digital-to-analog converter (DAC). The level of DACOUT also sets the PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage for the different combinations of connections on the VID pins. The VID pins can be left open for a logic 1 input, since they are internally pulled to the VAUX pin through 5kW resistors. Changing the VID inputs during operation is not recommended and could toggle the PGOOD signal and exercise the overvoltage protection. The output voltage program is Intel VRM8.5 compatible.

TABLE 1. OUT1 OUTPUT VOLTAGE PROGRAM

PIN NAME					NOMINAL DACOUT VOLTAGE
VID3	VID2	VID1	VID0	VID25	
0	1	0	0	0	1.050
0	1	0	0	1	1.075
0	0	1	1	0	1.100
0	0	1	1	1	1.125
0	0	1	0	0	1.150
0	0	1	0	1	1.175
0	0	0	1	0	1.200
0	0	0	1	1	1.225
0	0	0	0	0	1.250
0	0	0	0	1	1.275
1	1	1	1	0	1.300
1	1	1	1	1	1.325
1	1	1	0	0	1.350
1	1	1	0	1	1.375
1	1	0	1	0	1.400
1	1	0	1	1	1.425
1	1	0	0	0	1.450
1	1	0	0	1	1.475
1	0	1	1	0	1.500
1	0	1	1	1	1.525
1	0	1	0	0	1.550
1	0	1	0	1	1.575
1	0	0	1	0	1.600
1	0	0	1	1	1.625
1	0	0	0	0	1.650
1	0	0	0	1	1.675
0	1	1	1	0	1.700
0	1	1	1	1	1.725
0	1	1	0	0	1.750
0	1	1	0	1	1.775
0	1	0	1	0	1.800
0	1	0	1	1	1.825

NOTE: 0 = connected to GND, 1 = open or connected to 3.3V through pull-up resistors

Application Guidelines

Soft-Start Interval

Initially, the soft-start function clamps the error amplifier's output of the PWM converter. This generates PHASE pulses of increasing width that charge the output capacitor(s). The resulting output voltages start-up as shown in Figure 6.

The soft-start function controls the output voltage rate of rise to limit the current surge at start-up. The soft-start interval and the surge current are programmed by the soft-start capacitor, C_{SS}. Programming a faster soft-start interval increases the peak surge current. Using the recommended 0.1mF soft start capacitors ensure all output voltages ramp up to their set values in a quick and controlled fashion, while meeting the system timing requirements.

Shutdown

The PWM output does not switch until the soft-start voltage (V_{SS13}) exceeds the oscillator's valley voltage. Additionally, the reference on each linear's amplifier is clamped to the soft-start voltage. Holding the SS24 pin low (with an open drain or open collector signal) turns off regulators 1, 2 and 3. Regulator 4 (MCH) will simply drop its output to the intermediate soft-start level. This output is not allowed to violate the 2V maximum potential gap to the ATX 3.3V output.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of the upper MOSFET. Prior to turn-off, the upper MOSFET was carrying the full load current. During the turn-off, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using an ISL6524 controller. The switching power components are the most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the controller IC should be placed first. Locate the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Locate the output inductor and output capacitors between the MOSFETs and the load. Locate the PWM controller close to the MOSFETs.

The critical small signal components include the bypass capacitor for VCC and the soft-start capacitor, C_{SS}. Locate these components close to their connecting pins on the control IC. Minimize any leakage current paths from any SS node, since the internal current source is only 28mA.

A multi-layer printed circuit board is recommended. Figure 10 shows the connections of the critical components in the converter. Note that the capacitors C_{IN} and C_{OUT} each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections with vias to this layer.

Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but do not unnecessarily oversize this particular island. Since the PHASE node is subject to very high dV/dt voltages, the stray capacitor formed between these island and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the control IC to the MOSFET gate and source should be sized to carry 2A peak currents.

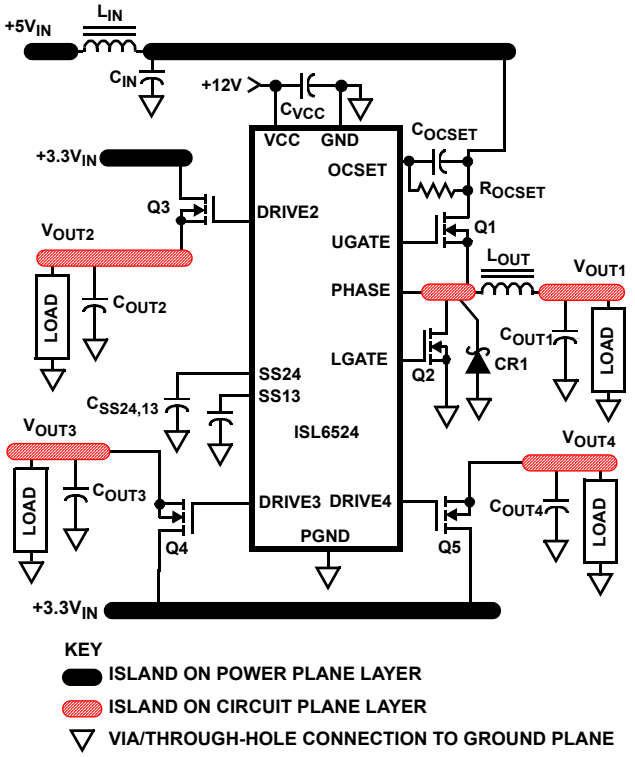


FIGURE 10. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

PWM1 Controller Feedback Compensation

The PWM controller uses voltage-mode control for output regulation. This section highlights the design consideration for a voltage-mode controller requiring external compensation.

Figure 11 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The reference voltage level is the DAC output voltage (DACOUT) for the PWM. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain, given by V_{IN}/V_{OSC}, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{ESR}.

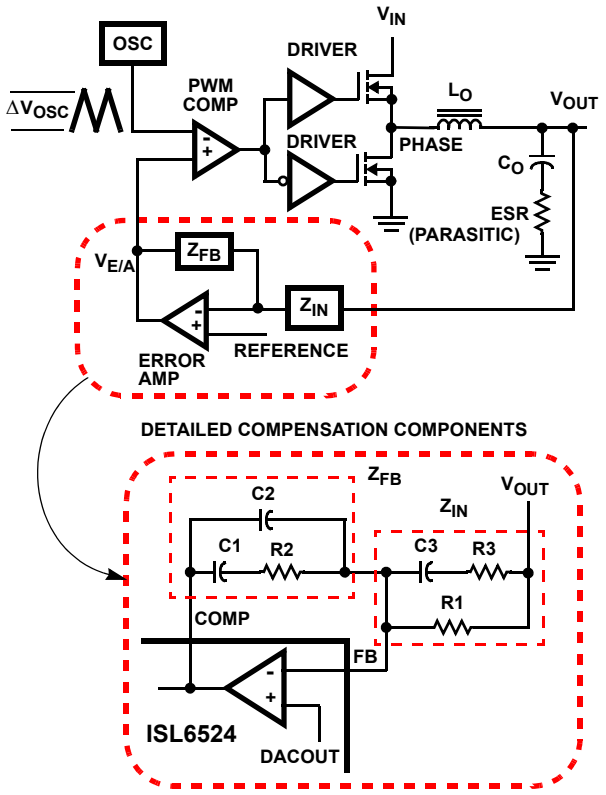


FIGURE 11. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

The compensation network consists of the error amplifier (internal to the ISL6524) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 11. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R2/R1) for desired converter bandwidth
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC})
3. Place 2ND Zero at Filter's Double Pole
4. Place 1ST Pole at the ESR Zero
5. Place 2ND Pole at Half the Switching Frequency
6. Check Gain against Error Amplifier's Open-Loop Gain
7. Estimate Phase Margin - Repeat if Necessary

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \qquad F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

Figure 12 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown in Figure 12. Using the above guidelines should yield a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the log-log graph of Figure 12 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

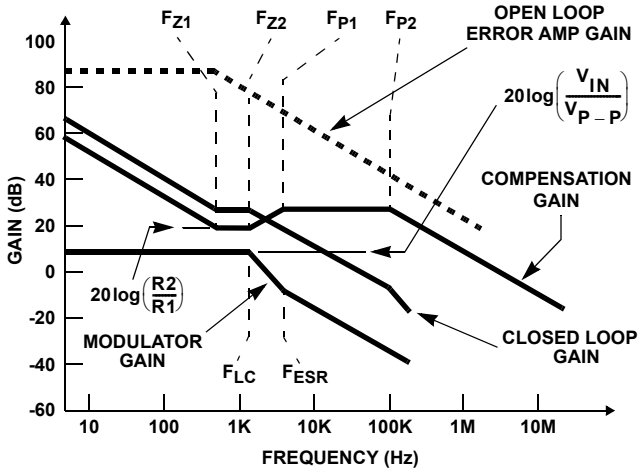


FIGURE 12. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

Component Selection Guidelines

Output Capacitor Selection

The output capacitors for each output have unique requirements. In general the output capacitors should be selected to meet the dynamic regulation requirements. Additionally, the PWM converter requires an output capacitor to filter the current ripple. The load transient for the microprocessor core requires high quality capacitors to supply the high slew rate (di/dt) current demands.

PWM Output Capacitors

Modern microprocessors produce transient load rates above 1A/ns. High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Linear Output Capacitors

The output capacitors for the linear regulators provide dynamic load current. Thus capacitors C_{OUT2}, C_{OUT3}, and C_{OUT4} should be selected for transient load regulation.

PWM Output Inductor Selection

The PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements and sets the converter's response time to a load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR$$

Increasing the value of inductance reduces the ripple current and voltage. However, large inductance values increase the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6524 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time interval required to slew the inductor current from an initial

current value to the post-transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L_O \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L_O \times I_{TRAN}}{V_{OUT}}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage. The maximum RMS current rating requirement for the input capacitors of a buck regulator is approximately 1/2 of the DC output load current. Worst-case RMS current draw in a circuit employing the ISL6524 amounts to the largest RMS current draw of the switching regulator.

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

For a through-hole design, several electrolytic capacitors (Panasonic HFQ series or Nichicon PL series or Sanyo MV-GX or equivalent) may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

MOSFET Selection/Considerations

The ISL6524 requires 5 external transistors. Two N-channel MOSFETs are employed by the PWM converter. The GTL, AGP, and memory linear controllers can each drive a MOSFET or a NPN bipolar as a pass transistor. All these transistors should be selected based upon $r_{DS(ON)}$, current gain, saturation voltages, gate supply requirements, and thermal management considerations.

PWM MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two main loss components: conduction losses and switching losses. These losses are distributed between the upper and lower MOSFET according to the duty factor. The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses, since the lower device turns on and off into near zero voltage.

The equations presented assume linear voltage-current transitions and do not model power losses due to the lower MOSFET's body diode or the output capacitances associated with either MOSFET. The gate charge losses are dissipated by the controller IC (ISL6524) and do not contribute to the MOSFETs' heat rise. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

The $r_{DS(ON)}$ is different for the two equations above even if the same device is used for both. This is because the gate drive applied to the upper MOSFET is different than the lower MOSFET. Figure 13 shows the gate drive where the upper MOSFET's gate-to-source voltage is approximately V_{CC} less the input supply. For +5V main power and +12VDC for the bias, the approximate gate-to-source voltage of Q1 is 7V. The lower gate drive voltage is 12V. A logic-level MOSFET is a good choice for Q1 and a logic-level MOSFET can be used for Q2 if its absolute gate-to-source voltage rating exceeds the maximum voltage applied to V_{CC}.

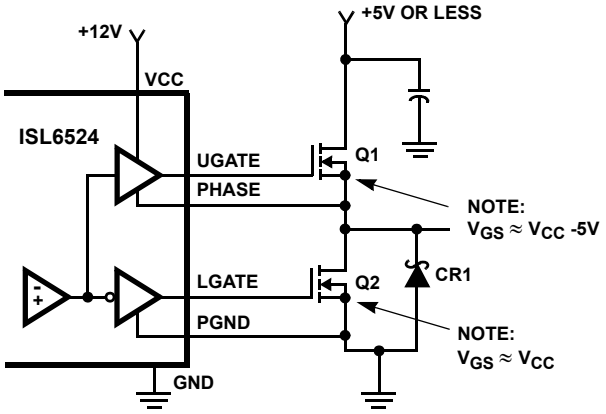


FIGURE 13. UPPER GATE DRIVE - DIRECT V_{CC} DRIVE

Rectifier CR1 is a clamp that catches the negative inductor swing during the dead time between the turn off of the lower MOSFET and the turn on of the upper MOSFET. For best results, the diode must be a surface-mount Schottky type to prevent the parasitic MOSFET body diode from conducting. It is acceptable to omit the diode and let the body diode of the lower MOSFET clamp the negative inductor swing, but one must ensure the PHASE node negative voltage swing does not exceed -3V to -5V peak. The diode's rated reverse breakdown voltage must be equal or greater to 1.5 times the maximum input voltage.

Linear Controllers Transistor Selection

The ISL6524 linear controllers are compatible with both NPN bipolar as well as N-channel MOSFET transistors. The main criteria for selection of pass transistors for the linear regulators is package selection for efficient removal of heat. The power dissipated in a linear regulator is

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the maximum desired temperature with the maximum expected ambient temperature.

When selecting bipolar NPN transistors for use with the linear controllers, insure the current gain at the given operating V_{CE} is sufficiently large to provide the desired output load current when the base is fed with the minimum driver output current.

In order to ensure the strict timing/level requirement of OUT4, an NPN transistor is recommended for use as a pass element on this output (Q5). A low gate threshold NMOS could be used, but meeting the requirements would then depend on the VCC bias being sufficiently high to allow control of the MOSFET.

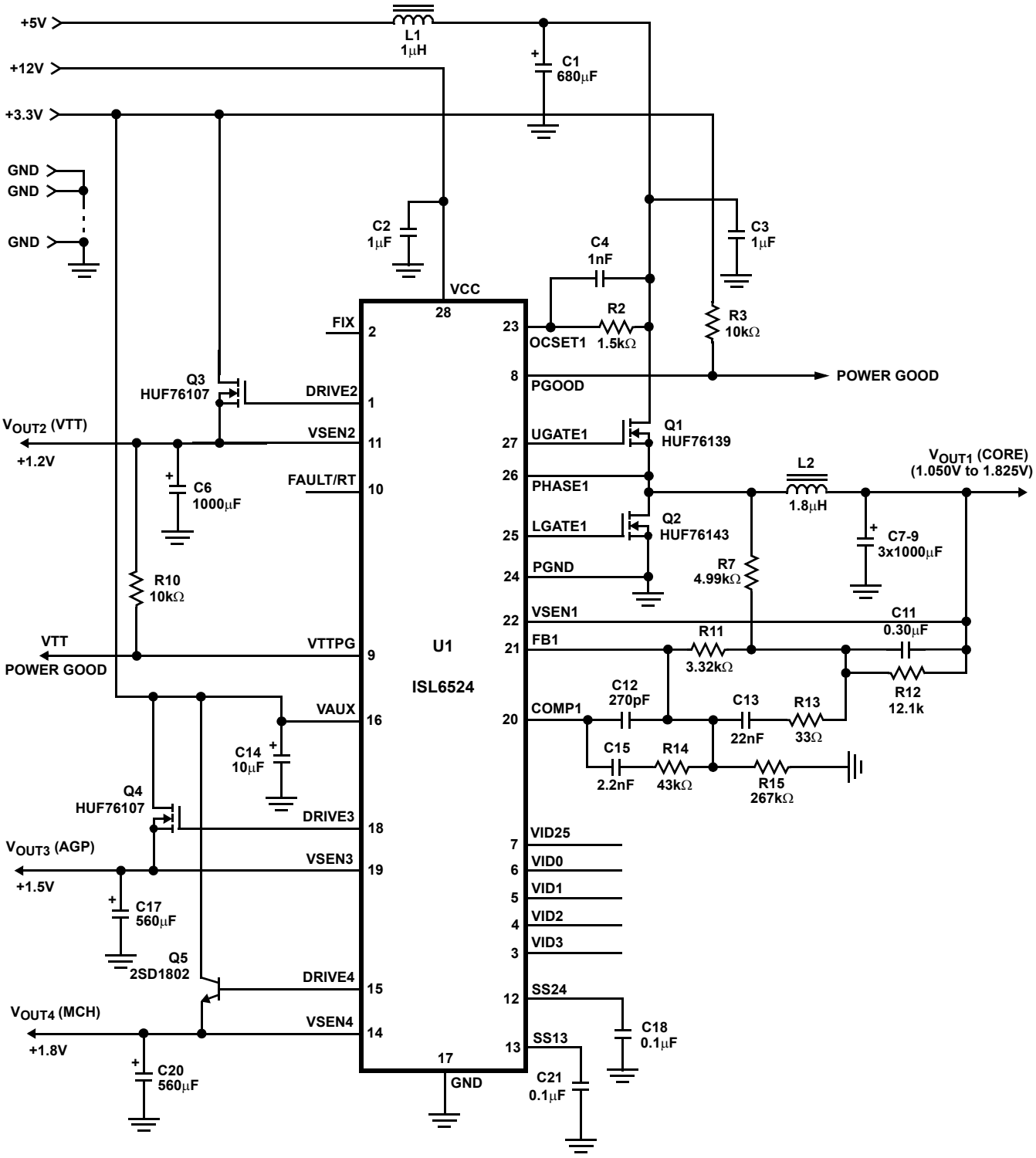
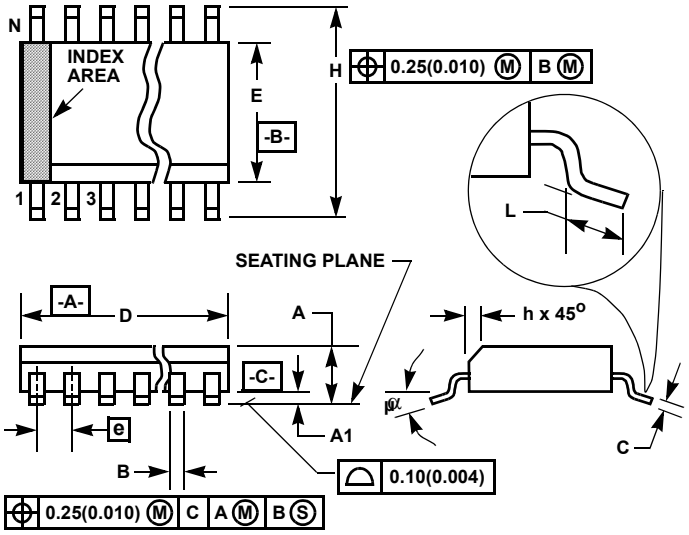


FIGURE 14. TYPICAL APPLICATION CIRCUIT

ISL6524 DC-DC Converter Application Circuit

Figure 14 shows an application circuit of a power supply for a microprocessor computer system. The power supply provides the microprocessor core voltage (V_{OUT1}), the GTL bus voltage (V_{OUT2}), the AGP bus voltage (V_{OUT3}), and the memory controller hub voltage (V_{OUT4}) from +3.3V, +5VDC, and +12VDC. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9925. Also see Intersil web page (www.intersil.com), for the latest information.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.