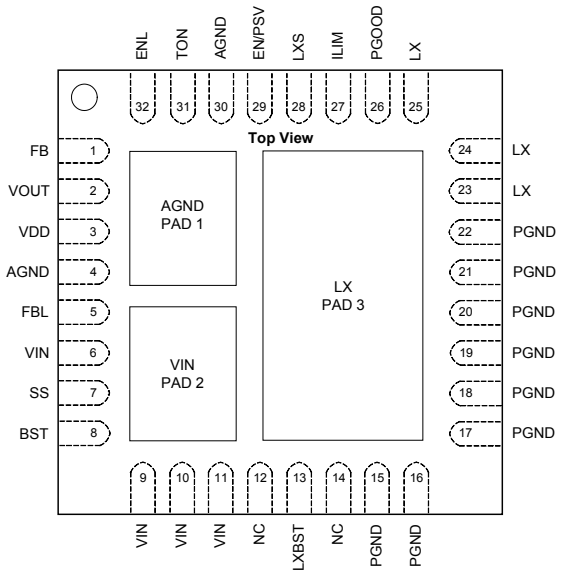
Pin Configuration



SC403B
MLPQ-32; 5x5, 32 LEAD

Ordering Information

Device	Package
SC403BMLTRT[(1)(2)]	MLPQ-32 5X5
SC403BEVB	Evaluation Board

Notes:
1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free package only. Device is RoHS/WEEE compliant and halogen-free.

Marking Information

yyww = Date Code
xxxxxx = Semtech Lot Number
xxxxxx = Semtech Lot Number

Absolute Maximum Ratings

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns max.) ..... -2 to +30
VIN to PGND (V) ..... -0.3 to +30
EN/PSV, PGOOD, ILIM, to GND (V) ..... -0.3 to +(V_{DD} + 0.3)
SS, VOUT, FB, FBL, to GND (V) ..... -0.3 to +(V_{DD} + 0.3)
VDD to PGND (V) ..... -0.3 to +6
TON to AGND (V) ..... -0.3 to +(VDD - 1.5)
ENL (V) ..... -0.3 to V_{IN}
BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +35
AGND to PGND (V) ..... -0.3 to +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
VDD to PGND (V) ..... 3.0 to 5.5
VOUT to PGND (V) ..... 0.6 to 5.5

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient [2] (°C/W)
- High-side MOSFET 48
- Low-side MOSFET 38
- PWM controller and LDO thermal resistance 36

Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, V_{DD} = +5V, per applicable Detailed Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
VIN UVLO Threshold)	Sensed at ENL pin, rising edge	2.40	2.60	2.95	V
	Sensed at ENL pin, falling edge	2.235	2.40	2.565	
VIN UVLO Hysteresis	EN/PSV = High		0.2		V
VDD UVLO Threshold	Measured at VDD pin, rising edge	2.5		3.0	V
	Measured at VDD pin, falling edge	2.4		2.9	
VDD UVLO Hysteresis			0.2		V
VIN Supply Current	ENL , EN/PSV = 0V, V_{IN} = 28V		8.5	20	µA
	Standby mode; ENL=V_{DD}, EN/PSV = 0V		130		

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
	ENL , EN/PSV = 0V, V_{DD} from external source		190	300	
	EN/PSV = V_{DD}, no load, V_{FB} > 600mV[2]		0.7		mA
	V_{DD} = 5V, f_{SW} = 250kHz, EN/PSV = floating , no load		4		
	V_{DD} = 3V, f_{SW} = 250kHz, EN/PSV = floating , no load		2.5		
FB On-Time Threshold	Static V_{IN} and load, 0 to +85 °C	0.595	0.600	0.605	V
	Static V_{IN} and load, -40 to +85 °C	0.594		0.606	V
Frequency Range	Continuous mode operation			1000	kHz
	Minimum f_{SW}, EN/PSV = V_{DD}, no load		25		
Bootstrap Switch Resistance			10		Ω
Switching MOSFET Resistance					
R_{DSON}	High Side FET		30		mΩ
	Low Side FET		10		
Timing					
On-Time	Continuous mode operation, V_{IN} = 15V, V_{OUT} = 5V, f_{SW}= kHz, R_{TON} = 300kΩ	2386	2650	2915	ns
	3V < V_{DD} < 4.5V[3]				
Minimum On-Time			80		ns
Minimum Off-Time	V_{DD} = 5V		250		ns
	V_{DD} = 3V		370		
Soft-Start					
Soft-Start Current			3		µA
Soft-Start Voltage	When V_{OUT} reaches regulation		1.5		V
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND	-3	0	+3	mV
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal reference		+20		%
	Lower limit, V_{FB} < internal reference		-10		%
Start-Up Delay Time (between PWM enable and PGOOD going high)	V_{DD} = 3V, C_{SS} = 10nF		7		ms
	V_{DD} = 5V, C_{SS} = 10nF		12		
Soft Start Threshold	When PGOOD logic switches high		64		%
Fault (noise immunity) Delay Time			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω
Fault Protection					
Valley Current Limit	V_{DD} = 5V,R_{ILIM} = 7.06k Ω	4.8	6	7.2	A
	V_{DD} = 3V,R_{ILIM} = 7.06k Ω		5.1		
Output Under-Voltage Fault	V_{FB} with respect to internal reference, 8 consecutive switching cycles		-25		%
Smart Power-save Protection Threshold	V_{FB} with respect to internal reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal reference		+20		%
Over-Voltage Fault Delay			5		µs
Over-Temperature Shutdown	10°C hysteresis		155		°C
Logic Inputs/Outputs					
Logic Input High Voltage	ENL, minimum level		1		V
Logic Input Low Voltage	ENL, maximum level		0.4		V
EN/PSV Input for PSAVE Operation	Maximum level expressed in % of V_{DD}		100		%
	Minimum level expressed in % of V_{DD}		45		

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Logic Inputs/Outputs (continued)					
EN/PSV Input for Forced Continuous Operation	Maximum level expressed in % of V_{DD}		42		%
	Minimum level		1		V
EN/PSV Input for Disabling Switcher	Maximum level		0.4		V
	Minimum level		0		
EN/PSV Input Bias Current	EN/PSV= VDD or AGND	-10		+10	µA
ENL Input Bias Current	V_{IN} = 16V		11	18	µA
FBL, FB Input Bias Current	FBL, FB = VDD or AGND	-1		+1	µA
Linear Regulator (The LDO is shorted to the VDD pin internally.)					
FBL Accuracy	LDO load = 10mA	0.735	0.75	0.765	V
LDO Current Limit	Short-circuit protection, V_{IN} = 12V, V_{DD} < 0.75V		65		mA
	Start-up and foldback, V_{IN} = 12V, 0.75 < V_{DD} < 90% of final V_{DD} value		115		
	Operating current limit, V_{IN} = 12V, V_{DD} > 90% of final V_{DD} value	135	200		
LDO to VOUT Switch-over Threshold (4)		-140		+140	mV
LDO to VOUT Non-switch-over Threshold (4)		-450		+450	mV
LDO to VOUT Switch-over Resistance	V_{OUT} = +5V		2		Ω
LDO Drop Out Voltage (5)	From V_{IN} to V_{DD}, V_{DD} = +5V, I_{LDO} = 100mA		1.2		V

Notes:

(1) V_{IN} UVLO is programmable using a resistor divider from VIN to ENL to AGND pins. The ENL voltage is compared to an internal reference.

(2) For V_{FB} > 0.750V for the SC403 and V_{FB} > 0.600V

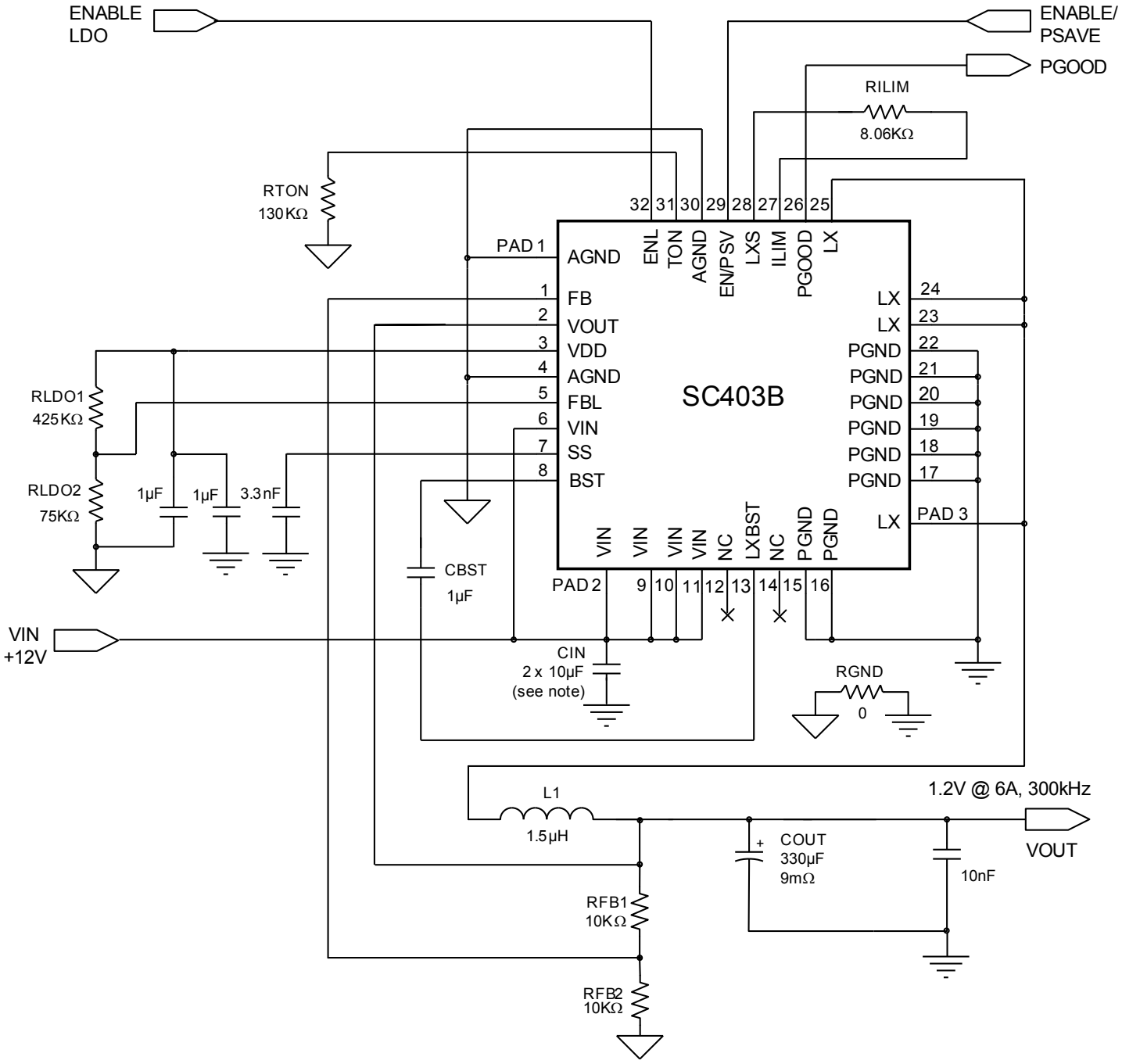
(3) For VDD less than 4.5V, the on-time may be limited by the VDD supply voltage and by the V_{IN}. See the TON limitation and VDD supply voltage section in the applications Information.

(4) The switch-over threshold is the maximum voltage differential between the VDD and VOUT pins which ensures that LDO will internally switch-over to VOUT. The non-switch-over threshold is the minimum voltage differential between the LDO and VOUT pins which ensures that LDO will not switch-over to VOUT.

(5) The LDO drop out voltage is the voltage at which the LDO output drops 2% below the no load regulation value.

Detailed Application Circuit — 1

Internal LDO Used as Bias

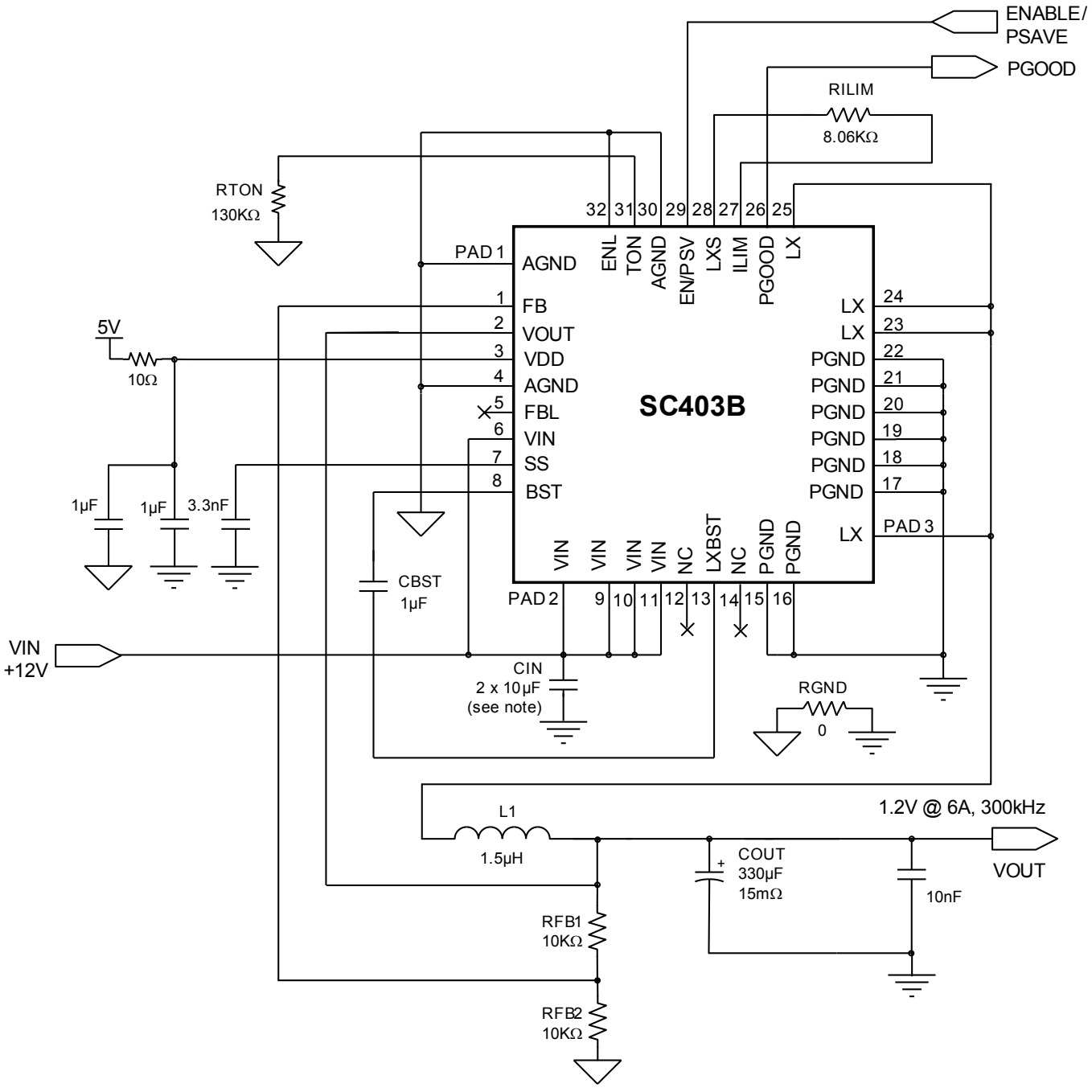


Key Components

Component	Value	Manufacturer	Part Number	Web
CIN	2 x 10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	330µF/9mΩ	Panasonic	EEF-SX0E331ER	www.panasonic.com
L1	1.5µH/6.7mΩ	Cyntec	PCMB065T-1R5MS	www.cyntec.com

Detailed Application Circuit — 2

External 5V Used as Bias



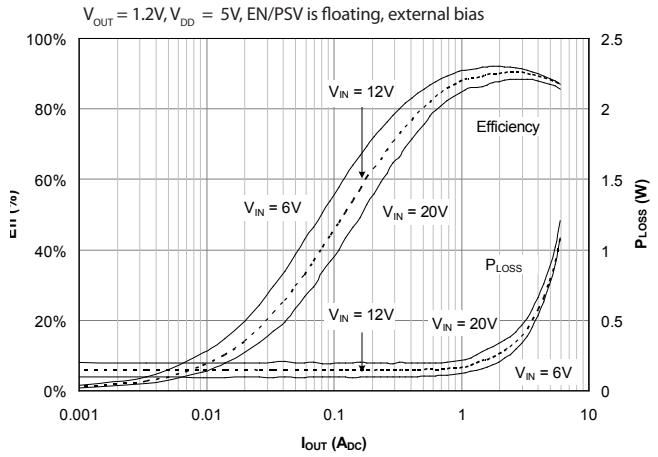
Key Components

Component	Value	Manufacturer	Part Number	Web
CIN	2 x 10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	330µF/9mΩ	Panasonic	EEF-SX0E331ER	www.panasonic.com
L1	1.5µH/6.7mΩ	Cyntec	PCMB065T-1R5MS	www.cyntec.com

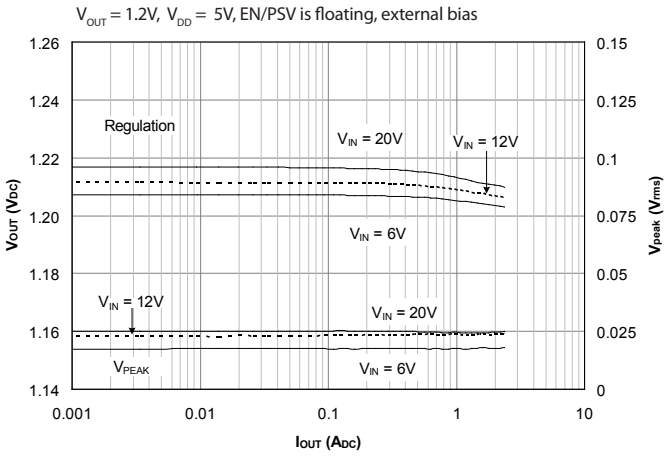
Typical Characteristics

Characteristics in this section are based on using the applicable Detailed Application Circuit — 2.

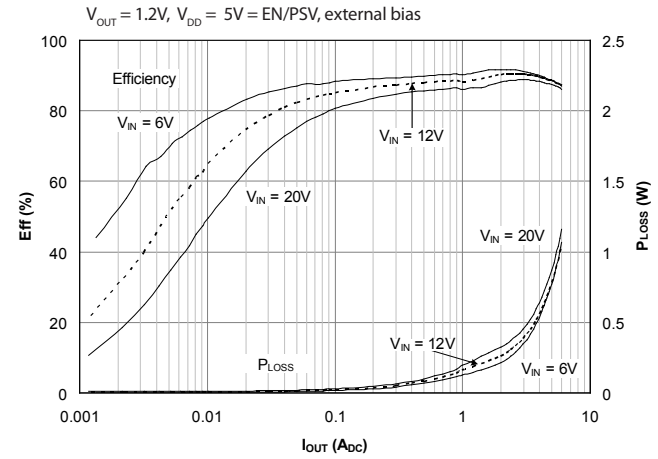
Efficiency vs. Load — Forced Continuous Mode



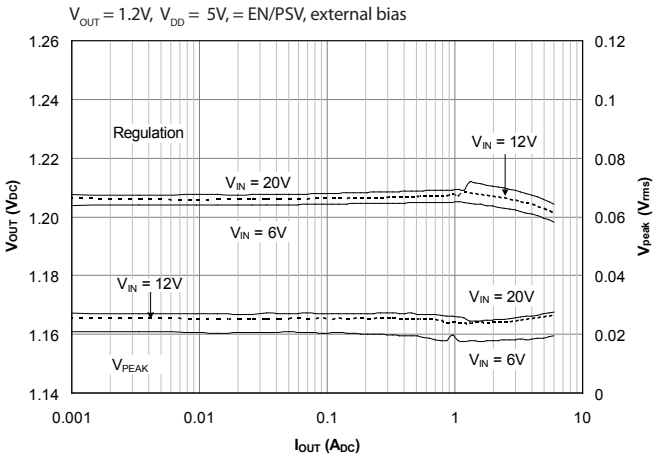
V_{OUT} vs. Load — Forced Continuous Mode



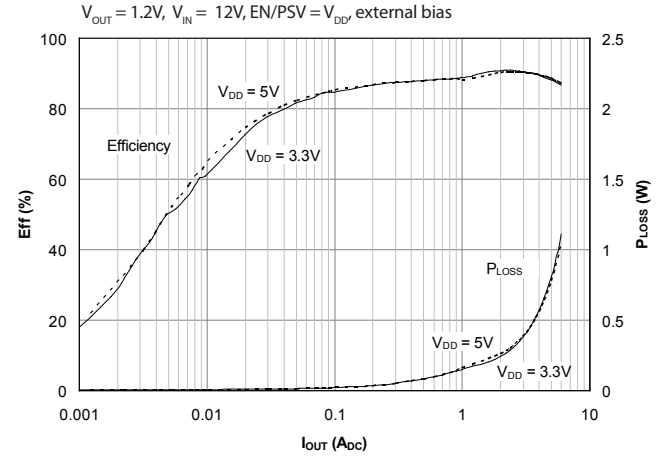
Efficiency vs. Load — PSAVE Mode



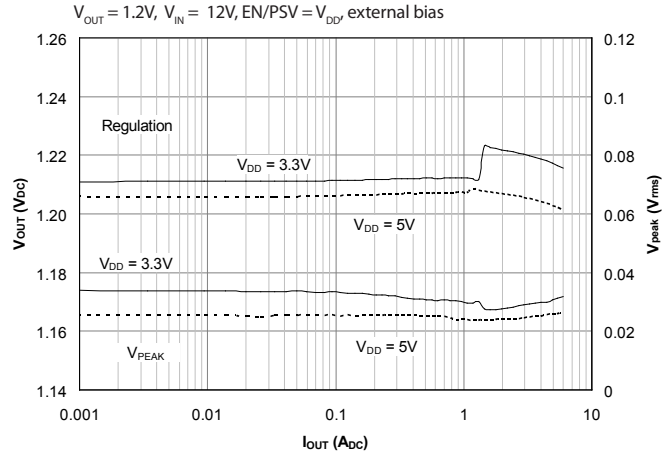
V_{OUT} vs. Load — PSAVE Mode



Efficiency vs. Load — PSAVE Mode



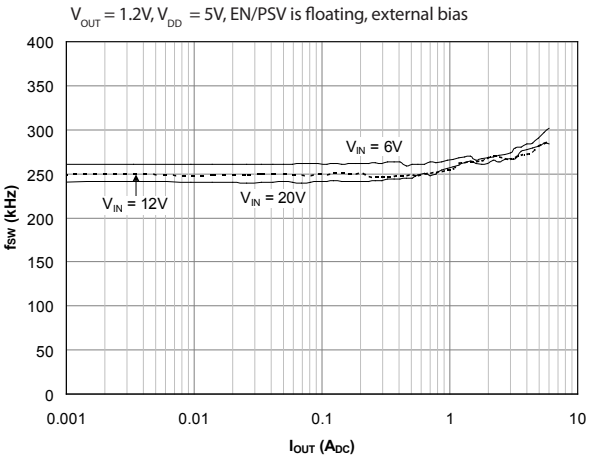
V_{OUT} vs. Load — PSAVE Mode



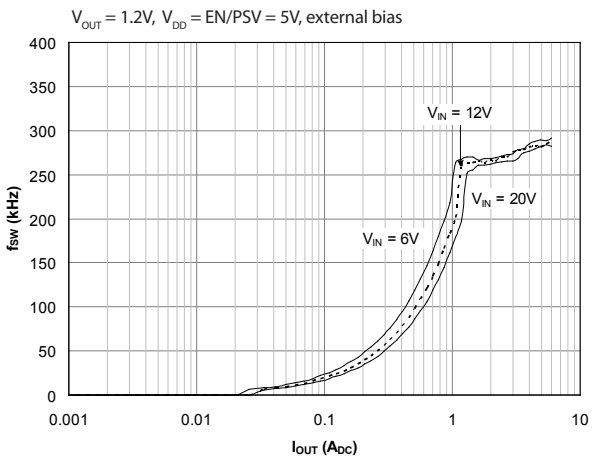
Typical Characteristics (continued)

Characteristics in this section are based on using the applicable Detailed Application Circuit — 2.

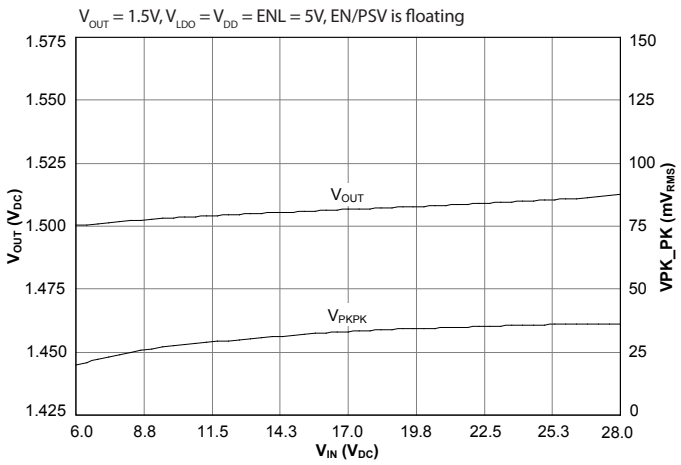
Frequency vs. Load — Forced Continuous Mode



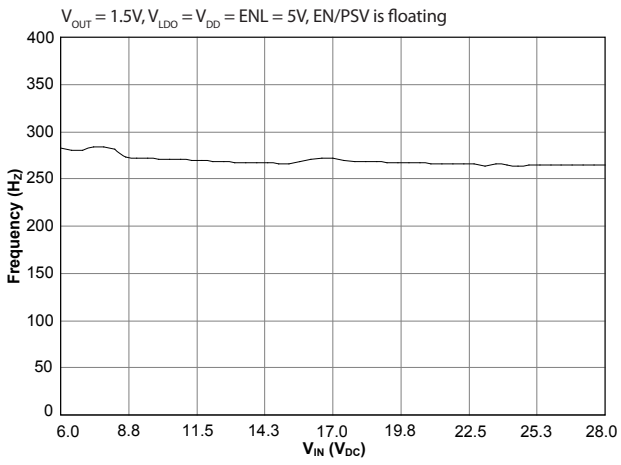
Frequency vs. Load — PSAVE Mode



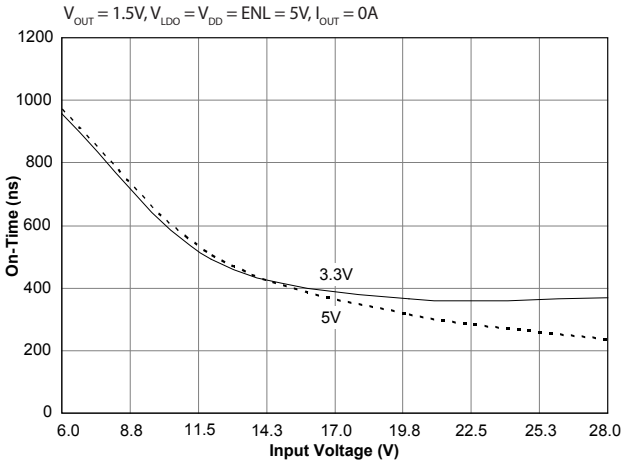
V_{OUT} vs. Line — Forced Continuous Mode



Frequency vs. Line — FCM Mode



On Time vs. Line

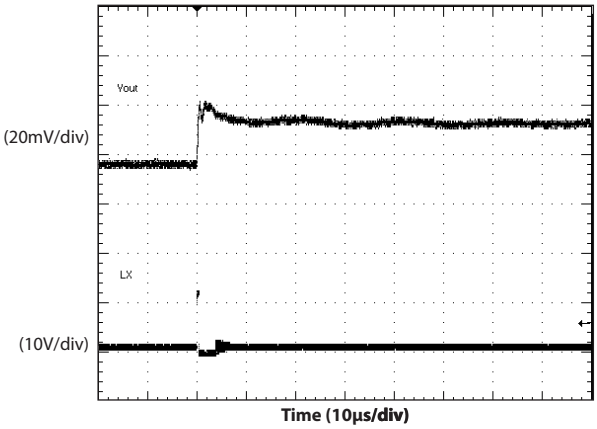


Typical Characteristics (continued)

Characteristics in this section are based on using the applicable Detailed Application Circuit — 2.

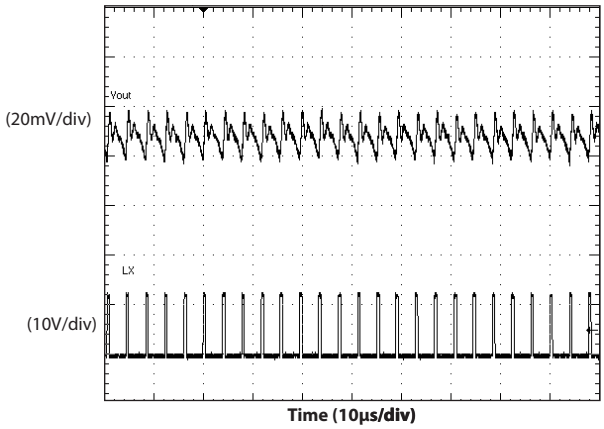
Powersave Mode — No Load

V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A, V_{LDO} = V_{DD} = EN/PSV= ENL = 5V



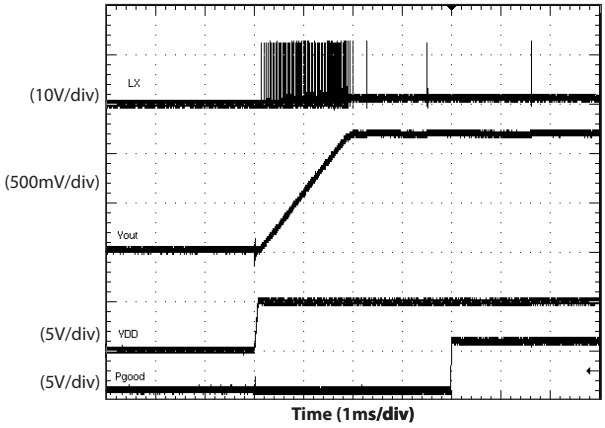
Forced Continuous Mode — No Load

V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{LDO} = V_{DD} = ENL = 3.3V, EN/PSV= floating



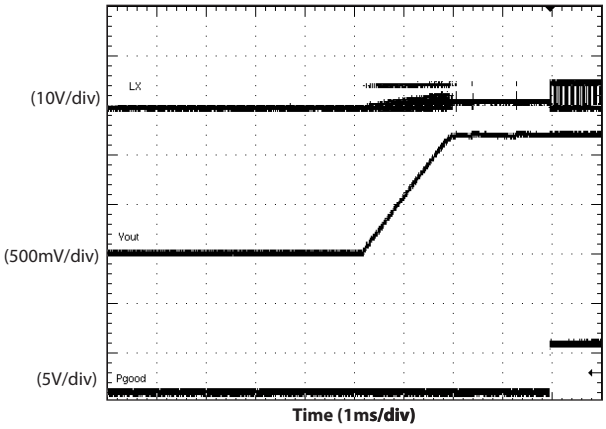
Self-Biased Start-Up — Power Good True

V_{IN} = 0V to 12V step, V_{OUT} = 1.2V, I_{OUT} = 0A, V_{LDO} = V_{DD} = EN/PSV= ENL = 5V



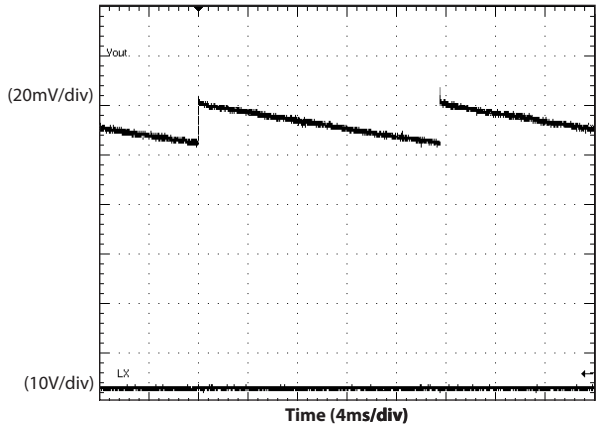
Enabled Loaded Output

V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 1A, V_{LDO} = V_{DD} = ENL = EN/PSV= 5V



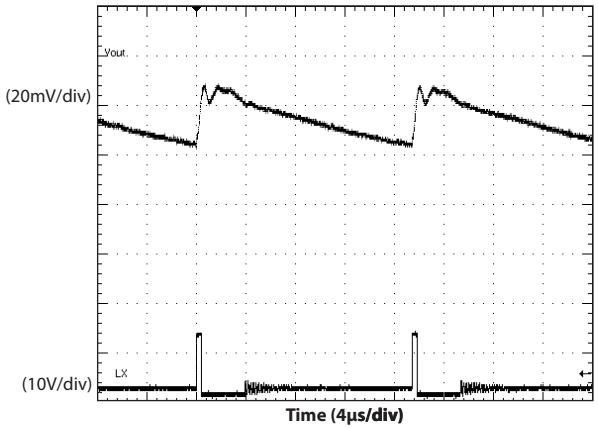
Self-Biased Start-Up — Power Good True

V_{IN} = 12V step, V_{OUT} = 1.2V, I_{OUT} = 0A, external V_{DD} = EN/PSV= 5V



Self-Biased Start-Up — Power Good True

V_{IN} = 12V step, V_{OUT} = 1.2V, I_{OUT} = 300mA, external V_{DD} = EN/PSV= 5V

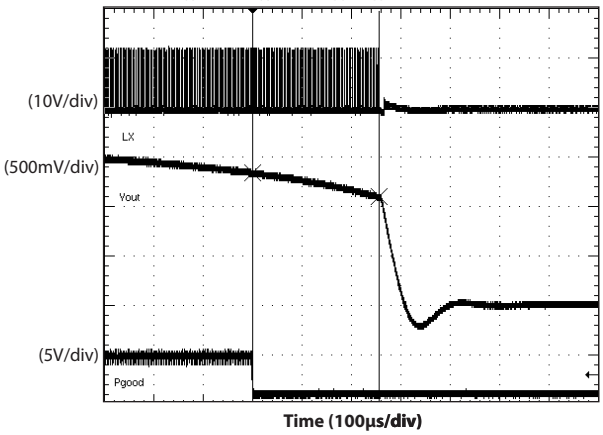


Typical Characteristics (continued)

Characteristics in this section are based on using the applicable Detailed Application Circuit — 2.

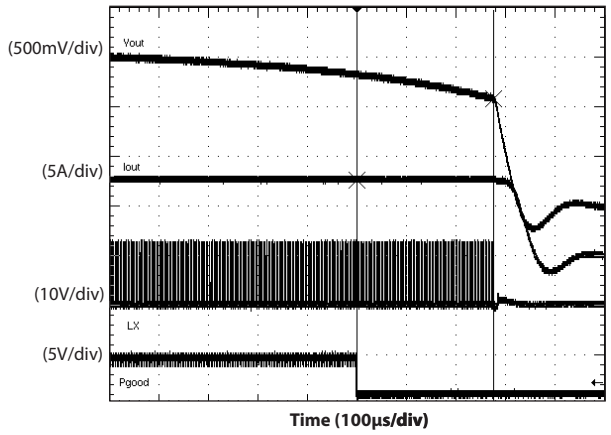
Output Under-voltage Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{LDO} = V_{DD} = ENL = 3.3V, floating EN/PSV



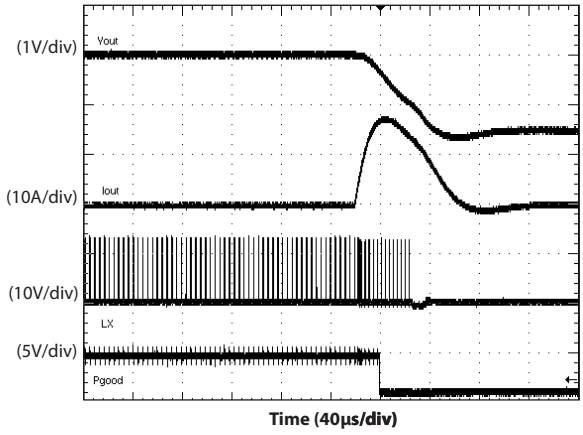
Output Over-current Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.5V, V_{LDO} = V_{DD} = ENL = 3.3V, EN/PSV= floating; I_{OUT} ramped to trip point



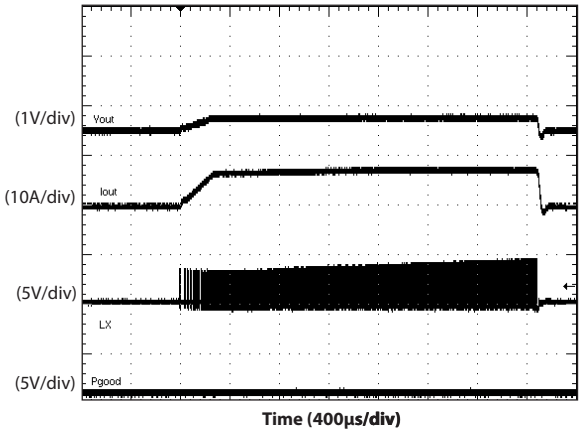
Shorted Output Response — Normal Operation

V_{IN} = 12V, V_{OUT} = 1.5V, V_{LDO} = V_{DD} = ENL = 3.3V, EN/P5V is floating



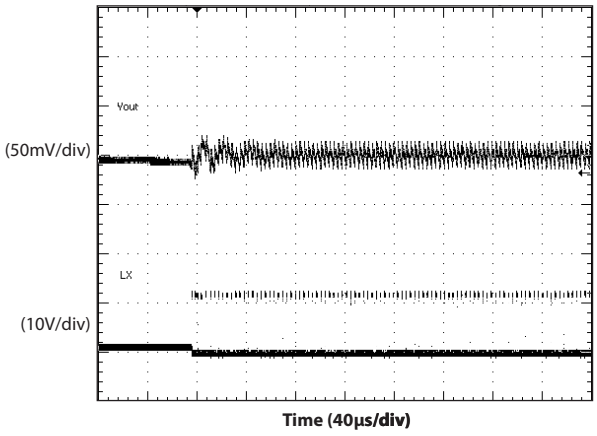
Shorted Output Response — Soft-start Operation

V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{LDO} = V_{DD} = EN/PSV= ENL = 3.3V



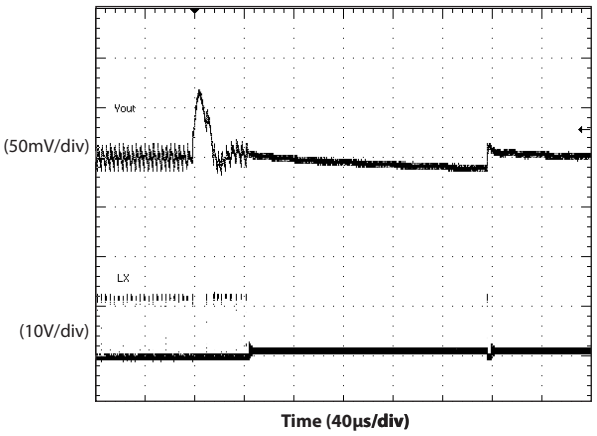
Transient Response

V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A to 6A, V_{LDO} = V_{DD} = EN/PSV= ENL = 5V



Transient Response

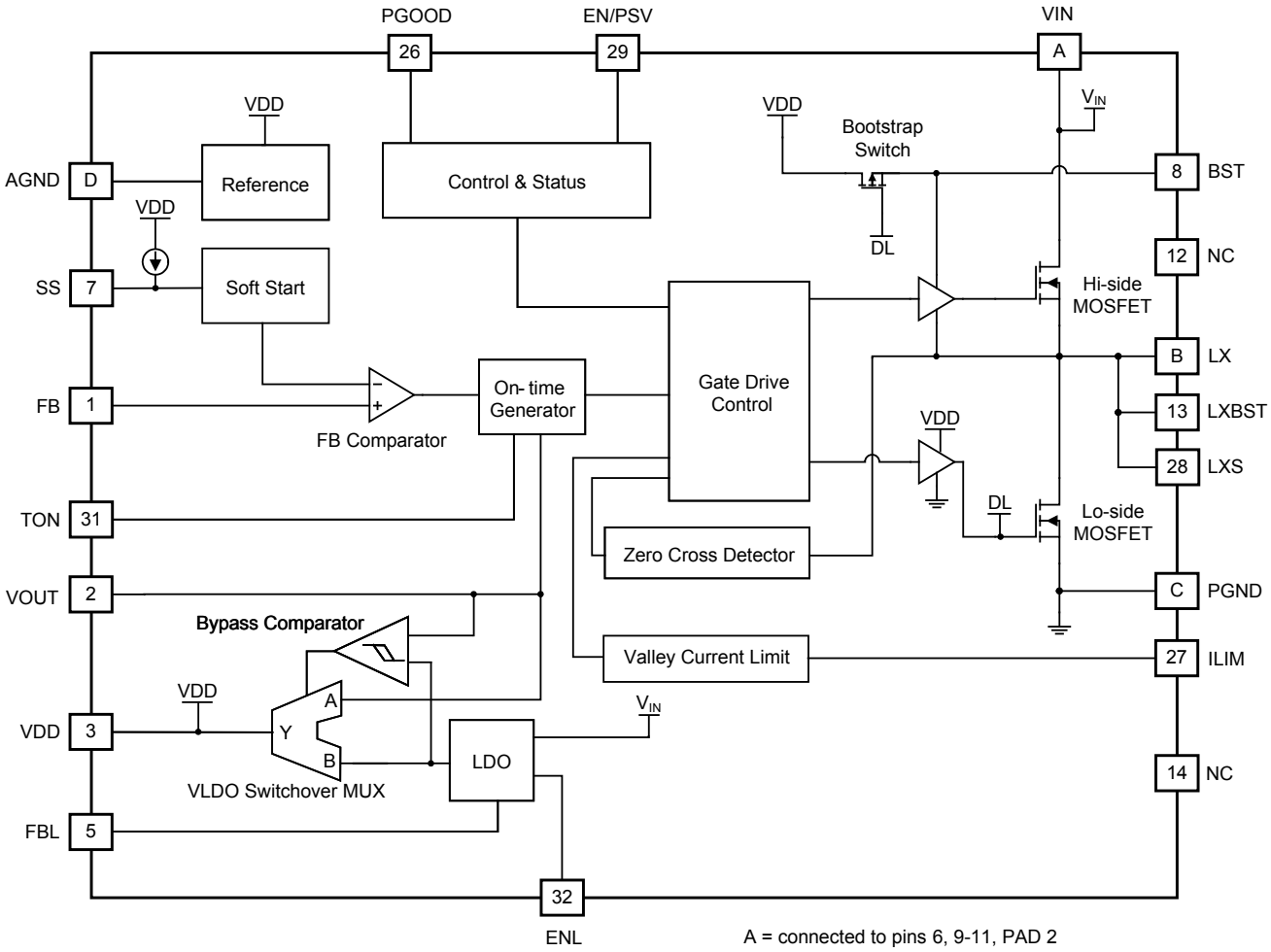
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 6A to 0A, V_{LDO} = V_{DD} = EN/PSV= ENL = 5V



Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator used to program the output voltage — connect to an external resistor divider from VOUT to AGND.
2	VOUT	Switcher output voltage sense pin — also the input to the internal switch-over between VOUT and VLDO. The voltage at this pin must be less than or equal to the voltage at the VDD pin.
3	VDD	Bias supply for the IC — when using the internal LDO as a bias power supply, the VDD is the LDO output. When using an external power supply to bias the IC, the LDO output should be disabled.
4, 30, PAD 1	AGND	Analog ground
5	FBL	Feedback input for the internal LDO — connect to an external resistor divider from VDD to AGND to program the LDO output.
6, 9-11, PAD 2	VIN	Input supply voltage
7	SS	The soft start time is programmed by an internal current source charging a capacitor on this pin.
8	BST	Bootstrap pin — connect a capacitor of at least 100nF from BST to LX to develop the floating supply for the high-side gate drive.
12	NC	No connection
13	LXBST	LX Boost — connect to the BST capacitor.
23-25, PAD 3	LX	Switching (phase) node
14	NC	No connection
15-22	PGND	Power ground
26	PGOOD	Open-drain power good indicator — high impedance indicates power is good. An external pull-up resistor is required.
27	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LXS.
28	LXS	LX sense — connects to R_{ILIM}.
29	EN/PSV	Enable/power-save input for the switching regulator — connect to AGND to disable the switching regulator. Float to operate in forced continuous mode (PSAVE disabled). Connect to VDD to operate with PSAVE mode enabled.
31	TON	On-time programming input — set the on-time by connecting through a resistor to AGND.
32	ENL	Enable input for the LDO — connect ENL to AGND to disable the LDO. Drive with logic signal for logic control, or program the VIN UVLO with a resistor divider between VIN, ENL, and AGND pins.

Block Diagram



A = connected to pins 6, 9-11, PAD 2
B = connected to pins 23-25, PAD 3
C = connected to pins 15-22
D = connect to pins 4, 30, PAD 1

Applications Information

Synchronous Buck Converter

The SC403B is a step down synchronous DC-DC buck converter with integrated power MOSFETs and a 200mA programmable LDO. The device operates at a current up to 6A at very high efficiency. A space saving 5x5 (mm) 32-pin package is used. The programmable operating frequency of up to 1MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response which permits the use of smaller output capacitors.

In addition to the following information, the user can click on the applicable link to go to the SC403B online C-SIM design and simulation tool, which will lead the user through the design process.

Input Voltage Requirements

The SC403B requires two input supplies for normal operation: V_{IN} and V_{DD}. V_{IN} operates over a wide range from 3V to 28V. VDD requires a supply voltage between 3V to 5V that can be an external source or the internal LDO from V_{IN}.

Power Up Sequence

The SC403B initiates a start up when VIN, VDD, and EN/PSV pins are above the applicable thresholds. When using an external bias supply for the V_{DD} voltage, it is recommended that the V_{DD} is applied to the device only after the V_{IN} voltage is present because V_{DD} cannot exceed V_{IN} at any time. A 10Ω resistor must be placed between the external V_{DD} supply and the VDD pin to avoid damage to the device during power-up and or shutdown situations where V_{DD} could exceed V_{IN} unexpectedly.

Shutdown

The SC403B can be shutdown by pulling either VDD or EN/PSV pin below its threshold. When using an external supply voltage for V_{DD}, the VDD pin must be deactivated while the V_{IN} voltage is still present. A 10Ω resistor must be placed between the external V_{DD} supply and the VDD pin to avoid damage to the device.

When the VDD pin is active and EN/PSV is at low logic level, the output voltage discharges through an internal FET.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC403B is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the controller on-time.

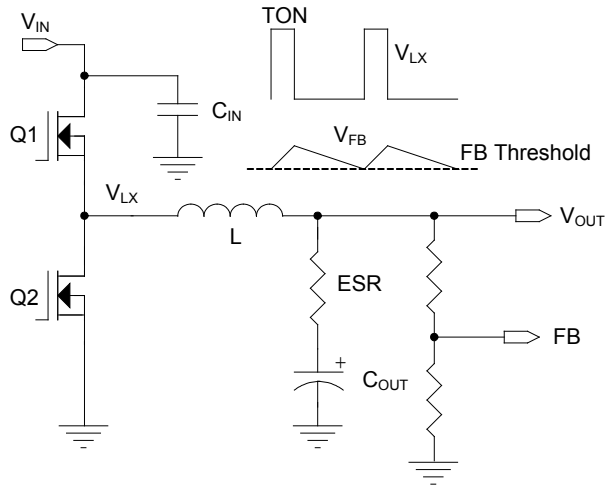


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}. The period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response

Applications Information (continued)

One-Shot Timer and Operating Frequency

One-shot timer operation is shown in Figure 2. The FB Comparator output goes high when V_{FB} is less than the internal reference. This feeds into the gate drive and turns on the high-side MOSFET, and starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

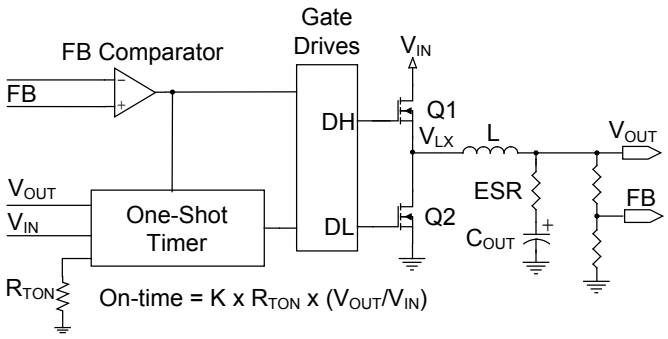


Figure 2 — On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC403B uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{(t_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{10 \times 1.5\mu A}$$

Immediately after the on-time, the DL (drive signal for the low side FET) output drives high to turn on the low-side MOSFET. DL has a minimum high time of ~320ns, after which DL continues to stay high until one of the following occurs:

- VFB falls below the reference
- The zero cross detector senses that the voltage on the LX node is below ground. Power save is activated eight switching cycles after a zero crossing is detected.

TON Limitations and V_{DD} Supply Voltage

For V_{DD} below 4.5V, the TON accuracy may be limited by the input voltage.

The original R_{TON} equation is accurate if V_{IN} satisfies the relationship over the entire V_{IN} range, as follows.

$$V_{IN} < (V_{DD} - 1.6V) \times 10$$

If V_{IN} exceeds (V_{DD} - 1.6V) x 10, for all or part of the V_{IN} range, the R_{TON} equation is not accurate. In all cases where $V_{IN} > (V_{DD} - 1.6V) \times 10$, the R_{TON} equation must be modified, as follows.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times (V_{DD} - 1.6V) \times 10}{25pF \times V_{OUT}}$$

Note that when $V_{IN} > (V_{DD} - 1.6V) \times 10$, the actual on-time is fixed and does not vary with V_{IN}. When operating in this condition, the switching frequency will vary inversely with V_{IN} rather than approximating a fixed frequency.

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal reference voltage, see Figure 3.

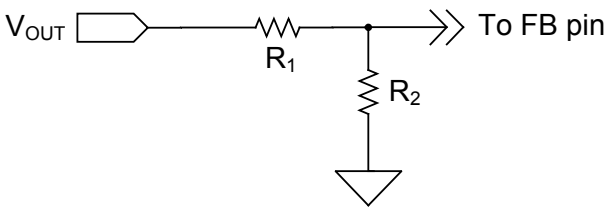


Figure 3 — Output Voltage Selection

Applications Information (continued)

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

When a large capacitor is placed in parallel with R1 (C_{TOP}) V_{OUT} is shown by the following equation.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

Enable and Power Save Input

The EN/PSV input is used to enable or disable the switching regulator. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 15Ω internal resistor via the V_{OUT} pin. When EN/PSV is allowed to float, the pin voltage will float to 33% of the voltage at VDD. The switching regulator turns on with PSAVE (power save) disabled and all switching is in forced continuous mode.

When EN/PSV is high (above 45% of the voltage at VDD), the switching regulator turns on with power-save enabled.

Forced Continuous Mode Operation

The SC403B operates the switcher in FCM (Forced Continuous Mode) by floating the EN/PSV pin (see Figure 4). In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs. DH is the gate signal driving the upper MOSFET. DL is the lower gate signal driving the lower MOSFET.

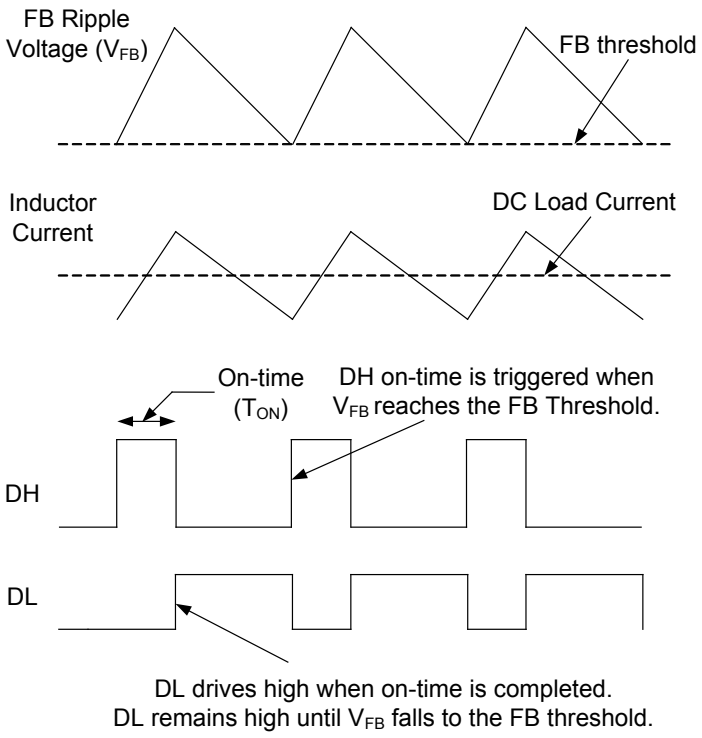


Figure 4 — Forced Continuous Mode Operation

Power-save Operation

The SC403B provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 600mV threshold. Because the MOSFETs are off, the load is supplied by the output capacitor.

Applications Information (continued)

If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode.

Figure 5 shows power-save operation at light loads.

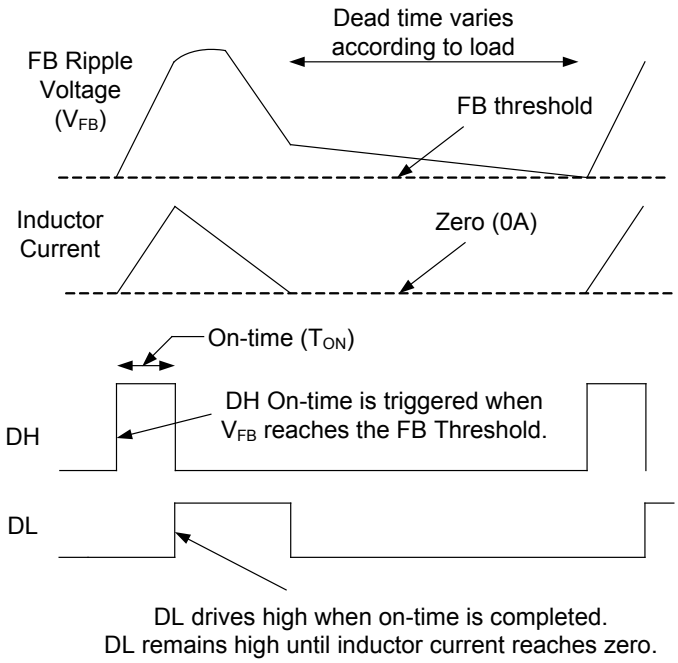


Figure 5 — PSAVE Operation

Smart PSAVE Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with PSAVE enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutdown. Smart PSAVE prevents this condition. When the FB voltage exceeds 10% above nominal, the device immediately disables PSAVE, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the internal reference trip point, a normal t_{ON} switching cycle begins. This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 6 shows typical waveforms for the Smart PSAVE feature.

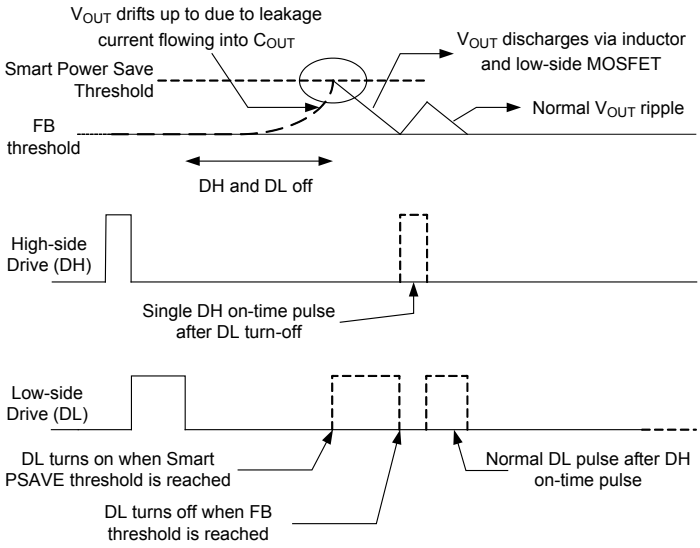


Figure 6 — Smart PSAVE

SmartDrive™

For each DH pulse the DH driver initially turns on the high-side MOSFET at a lower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 1V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching power loss while maintaining high efficiency and also avoids the need for snubbers or series resistors in the gate drive.

Current Limit Protection

Programmable current limiting is accomplished by using the RDS_{ON} of the lower MOSFET for current sensing. The current limit is set by the R_{ILIM} resistor. The R_{ILIM} resistor connects from the ILIM pin to the LXS pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~10µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the RDS_{ON}. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by ILIM in Figure 7.

Applications Information (continued)

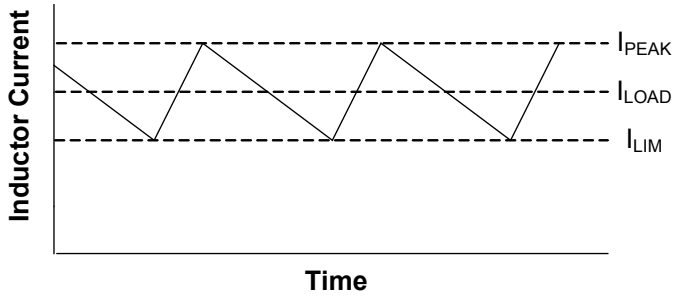


Figure 7 — Valley Current Limit

Setting the valley current limit to 6A results in a peak inductor current of 6A plus the peak-to-peak ripple current. In this situation, the average (load) current through the inductor is 6A plus one-half the peak-to-peak ripple current.

The internal 10µA current source is temperature compensated at 4100ppm in order to provide tracking with the RDS_{ON}.

The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 1176 \times I_{LIM} \times [0.088 \times (5V - V_{DD}) + 1] \ (\Omega)$$

where I_{LIM} is in Amps.

When selecting a value for R_{ILIM} do not exceed the absolute maximum voltage value for the ILIM pin. Note that because the low-side MOSFET with low RDS_{ON} is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to optimize operation. R_{ILIM} should be connected directly to LXS (pin 28).

Soft-Start of PWM Regulator

SC403B has a programmable soft-start time that is controlled by an external capacitor at the SS pin. After the controller meets both UVLO and EN/PSV thresholds, the controller has an internal current source of 3µA flowing through the SS pin to charge the capacitor. During the start up process (Figure 8), a percentage of the voltage at the SS pin is used as the reference for the FB comparator. The percentage is 50% for the SC403 and 40% for the SC403B. The PWM comparator issues an on-time pulse when the voltage at the FB pin is less than 50% (or 40%) of the SS pin. As result, the output voltage follows the SS start voltage. The output voltage reaches and maintains regulation when the soft start voltage is $\geq$ 1.5V. The time between the first LX pulse and when V_{OUT} meets regulation is the soft start time (t_{SS}). The calculation for the soft-start time is shown by the following equation.

$$t_{SS} = C_{SS} \times \frac{1.5V}{3\mu A}$$

The voltage at the SS pin continues to ramp up and eventually is equal to 64% of V_{DD}. After soft start completes, the FB pin voltage is compared to the internal reference. The delay time between the V_{OUT} regulation point and PGOOD going high is shown by the following equation.

$$t_{PGOOD\text{-}DELAY} = \frac{Css \times (0.64 \times V_{DD} - 1.5V)}{3\mu A}$$

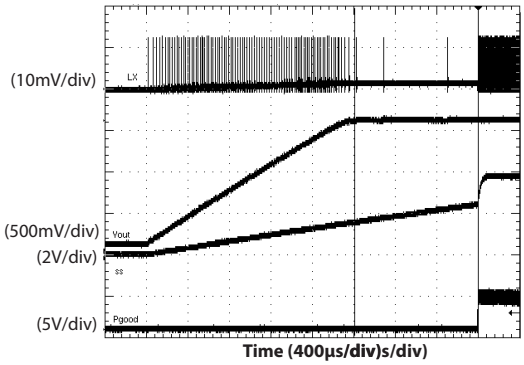


Figure 8 — Soft-start Timing Diagram

Pre-Bias Startup

SC403B can start up as if in a soft-start condition with an existing output voltage level. The soft start time is still the same as normal start up (when the output voltage starts from zero). The output voltage starts to ramp up when 40% of the voltage at SS pin meets the pre-charge FB voltage level. Pre-bias startup is achieved by turning off the lower gate when the inductor current falls below zero. This method prevents the output voltage from decreasing.

Power Good Output

The PGOOD (power good) output is an open-drain output which requires a pull-up resistor. When the voltage at the FB pin is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the output voltage returns above 92% of nominal.

Applications Information (continued)

PGOOD will transition low if the V_{FB} pin exceeds +20% of nominal, which is also the over-voltage shutdown threshold. PGOOD also pulls low if the EN/PSV pin is low when V_{DD} voltage is present.

Output Over-Voltage Protection

Over-voltage protection becomes active as soon as the device is enabled. The threshold is set at 20% above the feedback reference voltage. When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or VDD is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage for eight consecutive switching cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs. The controller stays off until EN/PSV is toggled or VDD is cycled.

VDD UVLO, and POR

UVLO (Under-Voltage Lock-Out) circuitry inhibits switching and tri-states the DH/DL drivers until V_{DD} rises above 3.0V. An internal POR (Power-On Reset) occurs when V_{DD} exceeds 3.0V, which resets the fault latch and soft-start counter to prepare for soft-start. The SC403B then begins a soft-start cycle. The PWM will shut off if VDD falls below 2.4V.

LDO Regulator

SC403B has an option to bias the switcher by using an internal LDO from V_{IN}. The LDO output is connected to VDD internally. The output of the LDO is programmable by using external resistors from the VDD pin to AGND. The feedback pin (FBL) for the LDO is regulated to 750mV (see Figure 9).

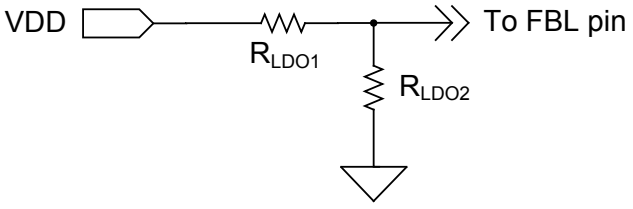


Figure 9 — LDO Voltage Divider

The LDO output voltage is set by the following equation.

$$VLDO = 750mV \times \left(1 + \frac{R_{LDO1}}{R_{LDO2}}\right)$$

A minimum 1µF capacitor referenced to AGND is required along with a minimum 1.0µF capacitor referenced to PGND to filter the gate drive pulses. The capacitance to PGND will need to increase to 10uF if VLDO is set to a voltage lower than 4.5V. Refer to the layout guidelines section for component placement suggestions.

LDO ENL Functions

The ENL input is used to control the internal LDO. When ENL is low (grounded), the LDO is off. When ENL is above the V_{IN} UVLO threshold, the LDO is enabled and the switcher is also enabled if EN/PSV and VDD meet the thresholds.

The ENL pin also acts as the switcher UVLO (under-voltage lockout) for the V_{IN} supply. The V_{IN} UVLO voltage is programmable via a resistor divider at the VIN, ENL and AGND pins.

If the ENL pin transitions from high to low within 2 switching cycles and is less than 1V, then the LDO will turn off but the switcher remains on. If the ENL goes below the V_{IN} UVLO threshold and stays above 1V, then the switcher will turn off but the LDO remains on. The V_{IN} UVLO function has a typical threshold of 2.6V on the V_{IN} rising edge. The falling edge threshold is 2.4V.

Note that it is possible to operate the switcher with the LDO disabled, but the ENL pin must be below the logic low threshold (0.4V maximum). In this case, the UVLO function for the input voltage cannot be used. The table below summarizes the function of the ENL and EN pins, with respect to the rising edge of ENL.

EN	ENL	LDO status	Switcher status
low	low, < 0.4V	off	off
high	low, < 0.4V	off	on
low	high, < 2.6V	on	off
high	high, < 2.6V	on	off
low	high, > 2.6V	on	off
high	high, > 2.6V	on	on

Applications Information (continued)

Figure 10 shows the ENL voltage thresholds and their effect on LDO and switcher operation.

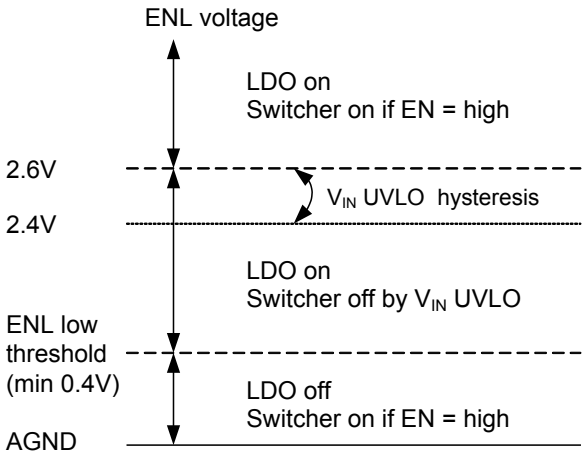


Figure 10 — ENL Threshold

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. V_{IN} input voltage

When the ENL pin is high and V_{IN} is above the UVLO point, the LDO will begin start-up. During the initial phase, when the V_{DD} voltage (which is the LDO output voltage) is less than 0.75V, the LDO initiates a current-limited start-up (typically 65mA) to charge the output capacitors while protecting from a short circuit event. When V_{DD} is greater than 0.75V but still less than 90% of its final value (as sensed at the FBL pin), the LDO current limit is increased to ~115mA. When V_{DD} has reached 90% of the final value (as sensed at the FBL pin), the LDO current limit is increased to ~200mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator. It is recommended that during LDO start-up to hold the PWM switching off until the LDO has reached 90% of the final value. This prevents overloading the current-limited LDO output during the LDO start-up.

Due to the initial current limitations on the LDO during power up (Figure 11), any external load attached to the VDD pin must be limited to 20mA before the LDO has reached 90% of it final regulation value.

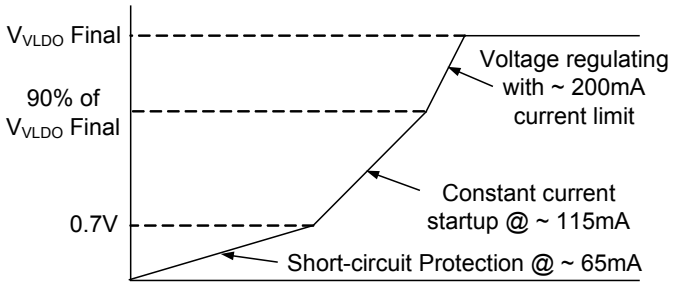


Figure 11 — LDO Start-Up

LDO Switch-Over Operation

The switch-over function is provided to increase efficiency by using the more efficient DC-DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the VDD pin directly to the VOUT pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in power savings and maximizes efficiency. If the LDO output is used to bias the SC403B, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over logic waits for 32 switching cycles before it starts the switch-over. When the LDO is already in regulation and the DC-DC converter is later enabled, as soon as the PGOOD output goes high, the 32 cycles are started. The voltages at the VDD and VOUT pins are then compared; if the two voltages are within ±300mV of each other, the VDD pin connects to the VOUT pin using an internal switch, and the LDO is turned off.

Switch-over Limitations on VOUT, ENL, and VDD

Because the internal switch-over circuit always compares the VOUT and VDD pins at start-up, there are limitations on permissible combinations of these pins. Consider the case where V_{OUT} is programmed to 3.0V and V_{LDO} is programmed to 3.3V. After start-up, the device would connect VOUT to VDD and disable the LDO, since the two voltages are within the ±300mV switch-over window. To avoid unwanted switch-over, the minimum difference between the voltages for V_{OUT} and V_{LDO} should be ±500mV.

Applications Information (continued)

In many applications, the EN/PSV pin will be pulled high to the VDD node to allow control of the PWM and LDO ENL pin. If the switch over feature is used, this circuit must be implemented with caution or the circuit may be damaged. In the case where the ENL pin is being controlled by a GPIO signal or is tied directly to the input voltage, the ENL pin can be pulled low while the PWM is still generating an output voltage that is seen across one of the switch-over diodes. This may result in the VDD node being held above its UVLO threshold while the LDO is deactivated. This type of operation can potentially damage the part.

In the case where the ENL pin is used to control the input UVLO, it is acceptable to connect EN/PSV directly to the VDD node.

It is not recommended to use the switch-over feature for an output voltage less than 3V since this does not provide sufficient voltage for the gate-source drive to the internal p-channel switch-over MOSFET.

Switch-over MOSFET Parasitic Diode

The switch-over MOSFET contains a parasitic diode that is inherent to its construction, as shown in Figure 12.

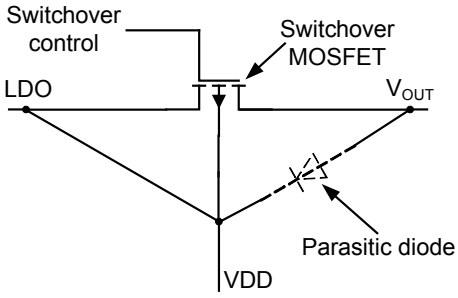


Figure 12— Switch-over MOSFET Parasitic Diodes

If V_{OUT} is higher than VDD, then the diode will turn on and the SC403B operating current will flow through this diode. This has the potential of damaging the device.

There are some important design rules that must be followed to prevent forward bias of this diode. The following condition, $V_{DD} \geq V_{OUT}$ needs to be satisfied in order for the parasitic diode to stay off and prevent damaging the device. Many applications connect the EN pin to V5V and control the on/off of the LDO and PWM simultaneously with the ENL pin. This allows one signal to control both the bias and power output of the SC403B. When V_{OUT} > 3.0V this configuration can cause problems due to the parasitic diodes in the LDO switchover circuitry. After the V_{OUT} > 3.0V PWM output is up and running the switchover diodes can hold up V5V > UVLO even if the ENL pin is grounded, turning off the LDO. Operating in this way can potentially damage the part.

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 12V ± 10%
- V_{OUT} = 1.5V ± 4%
- f_{SW} = 300kHz
- Load = 6A maximum
- V_{FB} = 600mV

Applications Information (continued)

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 300kHz which results from using components selected for optimum size and cost.

A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{(t_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for t_{ON} use the value associated with maximum V_{IN}.

$$t_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

t_{ON} = 379 ns at 13.2V_{IN}, 1.5V_{OUT}, 300kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 129.9kΩ, use R_{TON} = 130kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current and ripple voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for PSAVE operation. The switching will typically enter PSAVE mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then PSAVE operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then PSAVE will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50% of the maximum load current. Therefore ripple current will be 50% x 6A or 3A. To find the minimum inductance needed, use the V_{IN} and t_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2 - 1.5) \times 379ns}{3A} = 1.48\mu H$$

A slightly larger value of 1.5µH is selected. This will decrease the typical I_{RIPPLE} to 2.7A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$t_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 461ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L}$$

$$I_{RIPPLE\_MIN} = \frac{(10.8 - 1.5) \times 461ns}{1.5\mu H \times (1 + 0.2)} = 2.38A$$

$$I_{RIPPLE\_MAX} = \frac{(10.8 - 1.5) \times 379ns}{1.5\mu H \times (1 - 0.2)} = 3.7A$$

The value of L has been adjusted by ±20% for the equations above assuming an inductor tolerance of ±20%.

Applications Information (continued)

Output Capacitor Selection

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is that the output voltage regulation be ±4% under static conditions. The internal reference tolerance is ±1%. Allowing ±1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 60mV for a 1.5V output.

The maximum ripple current of 3.7A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{60mV}{3.7A}$$

$$ESR_{MAX} = 16.2\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when the inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor requiring a capacitance provided by the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.6V (100mV rise upon load release), and a 6A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{1.5\mu H\left(6A + \frac{1}{2} \times 3.7A\right)^2}{(1.6V)^2 - (1.5V)^2}$$

$$COUT_{MIN} = 298\mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt.

Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 6 + 1/2 \times 3.7 = 7.9A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 6A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2A}{1\mu s}$$

This would cause the output current to move from 6A to 0A in 3.0µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 7.9A \times \frac{1.5\mu H \times \frac{7.9}{1.5} - \frac{6}{2} \times 1\mu s}{2(1.6V - 1.5V)}$$

$$C_{OUT} = 194\ \mu F$$

Note that C_{OUT} is much smaller in this example, 194µF compared to 298µF based on a worst-case load release. To meet the maximum design criteria of minimum 298µF

Applications Information (continued)

and maximum 16mΩ ESR, select one capacitor rated at 330µF and 9mΩ ESR.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Soft Start Capacitor Selection

For a soft-start time (t_{SS}) of approximately 3ms, solve the following equation for C_{SS}.

$$C_{SS} = t_{SS} \frac{3\mu A}{1.5V}$$

$$C_{SS} = 6nF$$

If C_{SS} is selected as 4.7 nF, then t_{SS} will be 2.4 ms.

Then the PGOOD delay, the time from V_{OUT} regulation to PGOOD signal high is shown by the following equation.

$$t_{PGOOD\text{-}DELAY} = \frac{4.7nF \times (0.64V_{DD} - 1.5V)}{3\mu A}$$

At V_{DD} = 5V, the PGOOD delay will be 2.7ms.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~ 10pF) capacitor across the upper feedback resistor, as shown in Figure 13. This capacitor should be left unpopulated until it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

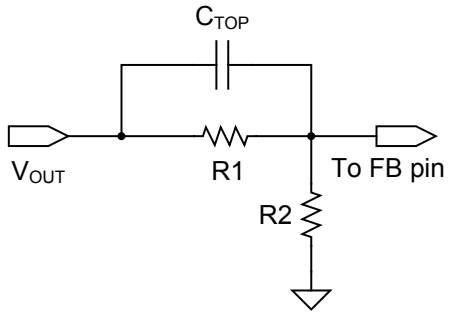


Figure 13 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one switching cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is a decrease in load regulation performance.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the

Applications Information (continued)

output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Using Ceramic Output Capacitors

For applications using ceramic output capacitors, the ESR is normally too small to meet the above ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in Figure 14. This network creates a ramp voltage across C_L, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitively coupled into the FB pin via capacitor C_C.

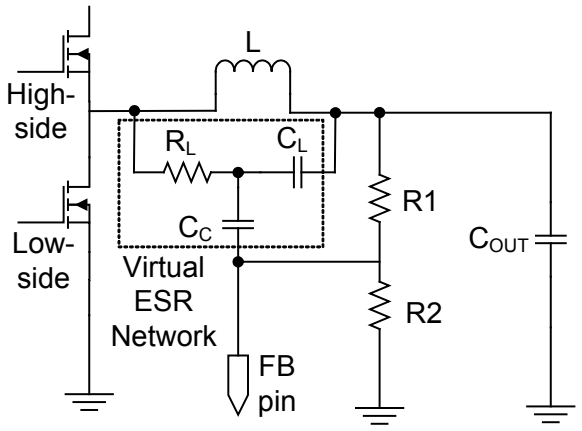


Figure 14 — Virtual ESR Ramp Circuit

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 80ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is within $\pm$1% of the reference voltage.

The on-time pulse from the SC403B in the design example is calculated to give a pseudo-fixed frequency of 300kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors may result in up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

Applications Information (continued)

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variation

The switching frequency will vary depending upon line and load conditions. The line variation is a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A constant on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

Applications Information (continued)

PCB Layout Guidelines

The optimum layout for the SC403B is shown in Figure 15. This layout shows an integrated FET buck regulator with a maximum current of 6A. The total PCB area is approximately 25 x 29 mm.

Critical Layout Guidelines

The following critical layout guidelines must be followed to ensure proper performance of the device.

- IC decoupling capacitors
- PGND plane
- AGND island
- FB, VOUT, and other analog control signals
- BST, ILIM, and LX
- CIN and COUT placement and current loops

IC Decoupling Capacitors

- A 0.1 µF capacitor must be located as close as possible to the IC and directly connected to pins 3 (VDD) and 4 (AGND).
- All other decoupling capacitors must be located as close as possible to the IC.

PGND Plane

- PGND requires its own copper plane with no other signal traces routed on it.
- Copper planes, multiple vias and wide traces are needed to connect PGND to input capacitors, output capacitors, and the PGND pins on the device.
- The PGND copper area between the input capacitors, output capacitors, and PGND pins must be as tight and compact as possible to reduce the area of the PCB that is exposed to noise due to current flow on this node.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the device as possible.

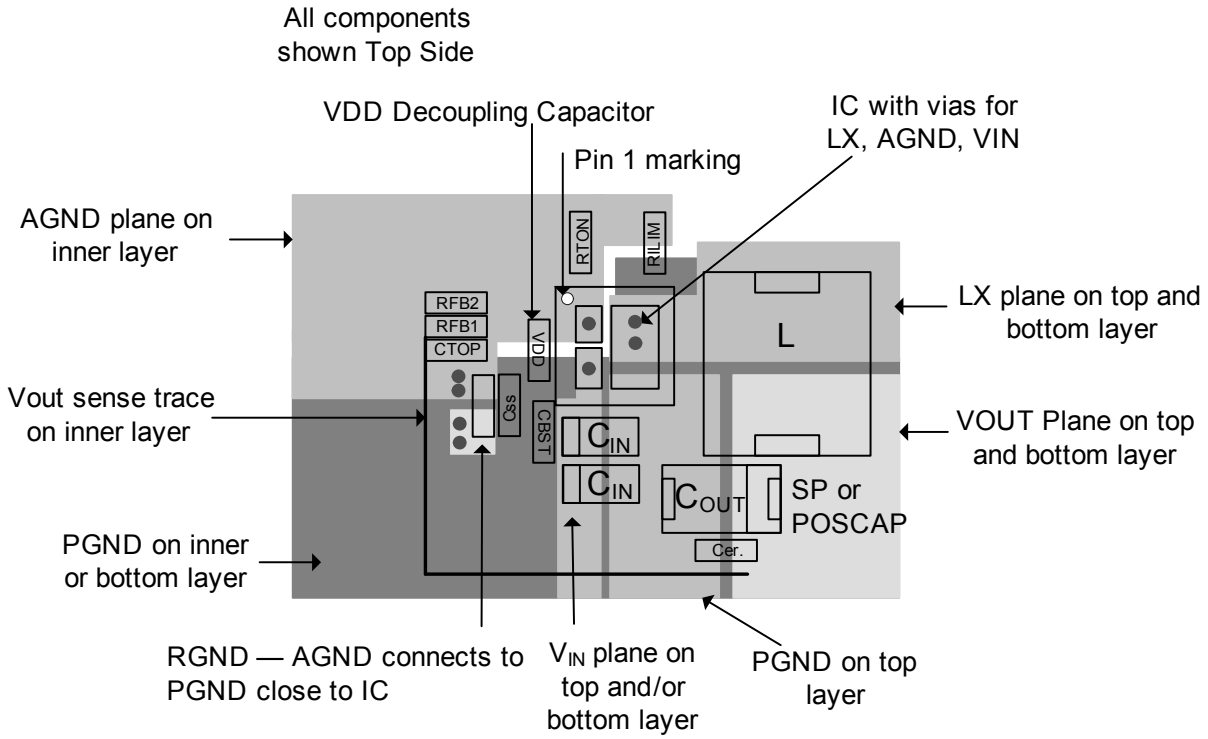


Figure 15 — PCB Layout

Applications Information (continued)

AGND Island

- AGND should have its own island of copper with no other signal traces routed on this layer that connects the AGND pins and pad of the device to the analog control components.
- All of the components for the analog control circuitry should be located so that the connections to AGND are done by wide copper traces or vias down to AGND.
- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the device as possible.

FB, VOUT, and Other Analog Control Signals

- The connection from the V_{OUT} power to the analog control circuitry must be routed from the output capacitors and located on a quiet layer.
- The traces between VOUT and the analog control circuitry (VOUT, and FB pins) must be short and routed away from noise sources, such as BST, LX, VIN, and PGND between the input capacitors, output capacitors, and the device.
- ILIM and TON nodes must be as short as possible to ensure the best accuracy in current limit and on time.
- The R_{ILIM} resistor should be close to the device and connected to LX with a Kelvin trace to pin 28 on the device. All of the LX pins are connected to the LX PAD on the device, which should be a sufficient connection and will prevent the need to connect the resistor further into the LX plane.
- The feedback components for the switcher and the LDO need to be as close to the FB and FBL pins of the device as possible to reduce the possibility of noise corrupting these analog signals.

BST, ILIM, and LX

- LX and BST are very noisy nodes and must be routed to minimized the PCB area that is exposed to these signals.
- The connections for the boost capacitor between the device and LX must be short and directly connected to the LXBST (pin 13).
- The connections for the current limit resistor between the ILIM pin and LX must be as short as possible and directly connected to pin 28 (LXS).
- The LX node between the IC and the inductor should be wide enough to handle the inductor current and short enough to eliminate the possibility of LX noise corrupting other signals.
- Multiple vias should be used to provide a good connection to LX between the device and the inductor.

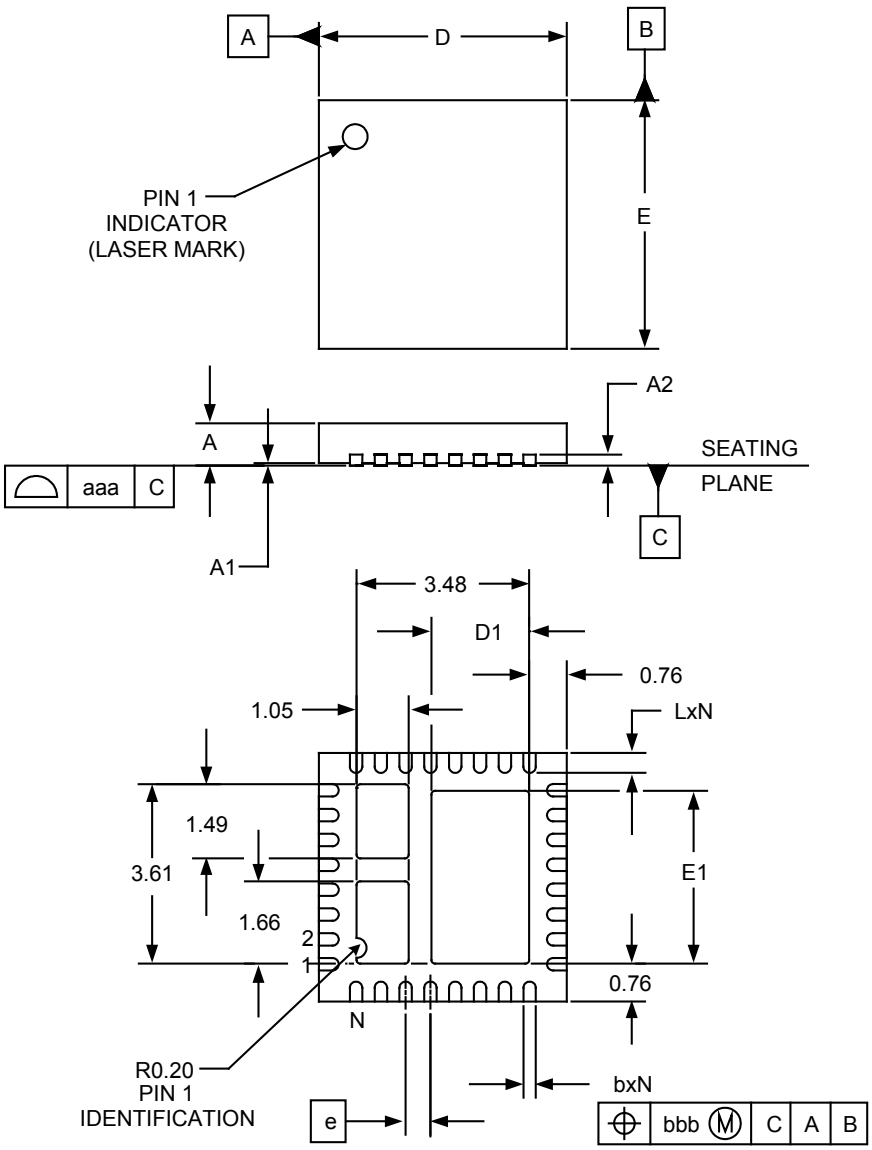
Capacitors and Current Loops

- The current loops between the input capacitors, the device, the inductor, and the output capacitors must be as close as possible to each other to reduce IR drop across the copper.
- All bypass and output capacitors must be connected as close as possible to the pin on the device.

Soft-Start Capacitor

- The capacitor used for soft-start should be located away from the BST pin and its capacitor.
- If possible locate the boost capacitor on the opposite side of the board form the IC and soft-start capacitor.

Outline Drawing — MLPQ-5x5-32

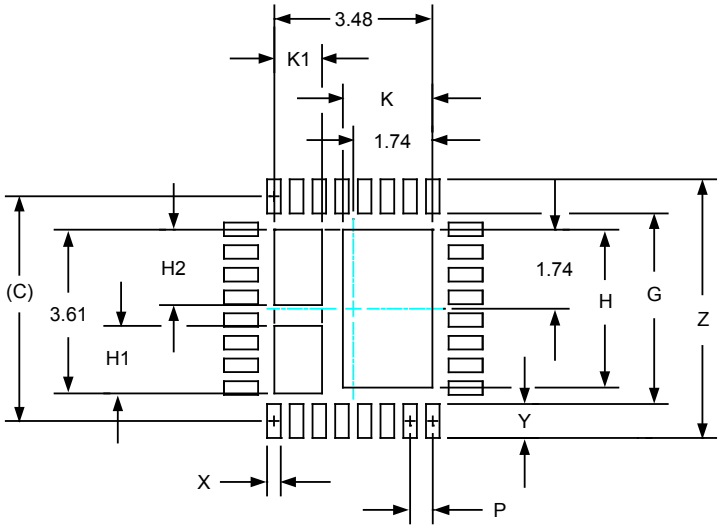


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.076	.078	.080	1.92	1.97	2.02
E	.193	.197	.201	4.90	5.00	5.10
E1	.135	.137	.139	3.43	3.48	3.53
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-5x5-32



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.195)	(4.95)
G	.165	4.20
H	.137	3.48
H1	.059	1.49
H2	.065	1.66
K	.078	1.97
K1	.041	1.05
P	.020	0.50
X	.012	0.30
Y	.030	0.75
Z	.224	5.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Semtech:

SC403BMLTRT SC403MLTRT