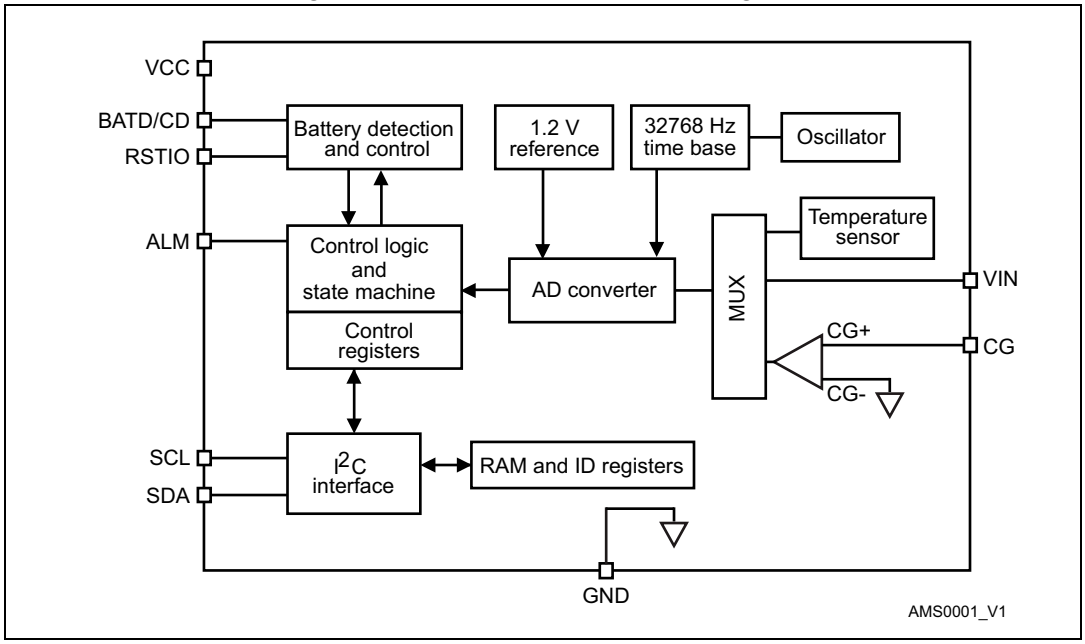
Contents

1 Block diagram

Figure 1. STC3115 internal block diagram



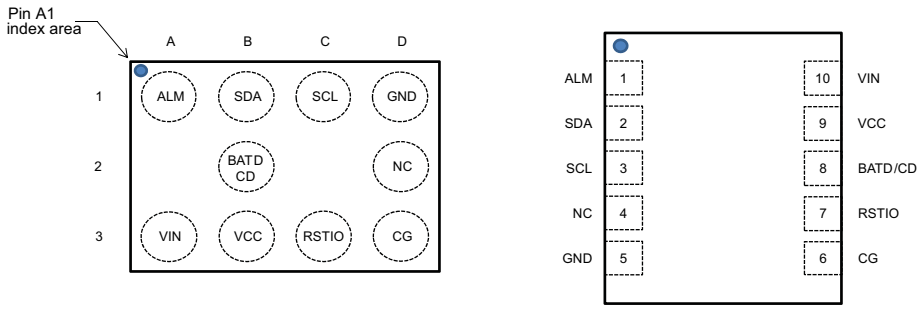
2 Pin assignment

Table 1. STC3115 pin description

DFN Pin	CSP bump	Pin name	Type(1)	Function
1	A1	ALM	I/OD	Alarm signal output, open drain, external pull-up with resistor
2	B1	SDA	I/OD	I^2C serial data
3	C1	SCL	I_D	I^2C serial clock
4	D2	NC	-	Not connected
5	D1	GND	Ground	Analog and digital ground
6	D3	CG	I_A	Current sensing input
7	C3	RSTIO	I/OD	Reset sense input & reset control output (open drain)
8	B2	BATD/CD	I/OA	Battery charge inhibit (active high output) Battery detection (input)
9	B3	VCC	Supply	Power supply
10	A3	VIN	I_A	Battery voltage sensing input

1. I = input, 0 = output, OD = open drain, A = analog, D = digital, NC = not connected

Figure 2. Pin connections for each package (top view)



CSP (1.4 mm x 2.0 mm) DFN10 (2.0 mm x 3.0 mm)

3 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCMAX}	Maximum voltage on VCC pin	6	V
V_{IO}	Voltage on I/O pins	-0.3 to 6	
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature	150	
ESD	Electrostatic discharge (HBM: human body model)	2	kV

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Operating supply voltage on V_{CC}	2.7 to 4.5	V
V_{MIN}	Minimum voltage on V_{CC} for RAM content retention	2.0	
T_{OPER}	Operating free air temperature range	-40 to 85	°C
T_{PERF}		-20 to 70	

4 Electrical characteristics

Table 4. Electrical characteristics (2.7 V < V_{CC} < 4.5 V, -20 °C to 70 °C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Supply						
I_{CC}	Operating current consumption	Average value over 4 s in power-saving voltage mode		45	60	µA
		Average value over 4 s in mixed mode			100	
I_{STBY}	Current consumption in standby	Standby mode, inputs = 0 V			2	
I_{PDN}	Current consumption in power-down	V_{CC} < $UVLO_{TH}$, inputs = 0 V			1	
$UVLO_{TH}$	Undervoltage threshold	(V_{CC} decreasing)	2.5	2.6	2.7	V
$UVLO_{HYST}$	Undervoltage threshold hysteresis			100		mV
POR	Power-on reset threshold	(V_{CC} decreasing)		2.0		V
Current sensing						
Vin_gg	Input voltage range		-40		+40	mV
I_{IN}	Input current for CG pin				500	nA
ADC_res	AD converter granularity			5.88		µV
ADC_offset	AD converter offset	CG = 0 V	-3		3	LSB
ADC_time	AD conversion time			500		ms
ADC_acc	AD converter gain accuracy at full scale (using external sense resistor)	25 °C		0.5		%
		Overtemperature range			1	
F_{OSC}	Internal time base frequency			32768		Hz
Osc_acc	Internal time base accuracy	25 °C, V_{CC} = 3.6 V		2		%
		Overtemperature and voltage ranges			2.5	
Cur_res	Current register LSB value			5.88		µV

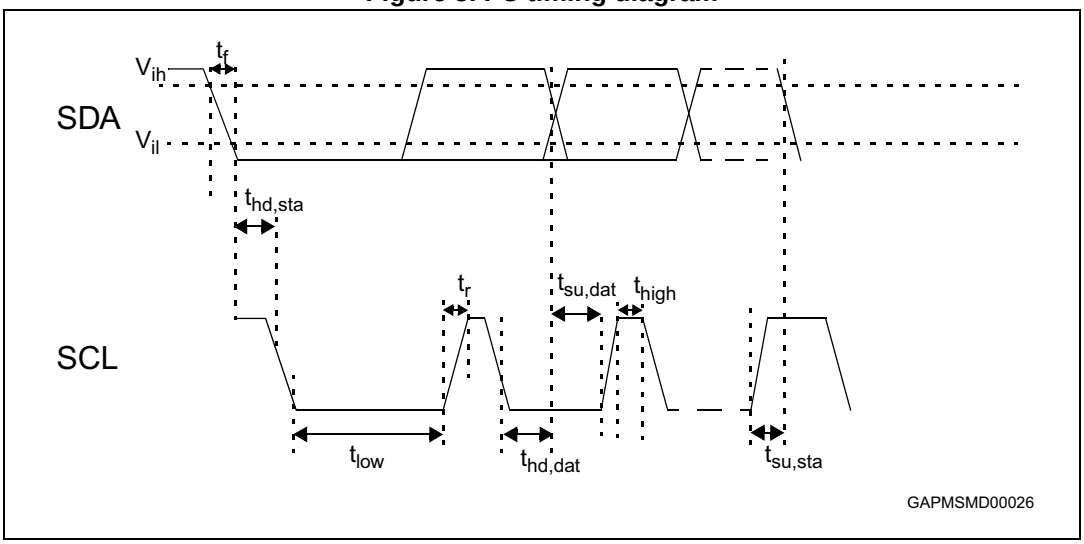
Table 4. Electrical characteristics (2.7 V < V_{CC} < 4.5 V, -20 °C to 70 °C) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Battery voltage and temperature measurement						
Vin_adc	Input voltage range	V_{CC} = 4.5 V	0		4.5	V
LSB	LSB value	Voltage measurement		2.20		mV
		Temperature measurement		1		°C
ADC_time	AD conversion time			250		ms
Volt_acc	Battery voltage measurement accuracy	2.7 V < Vin < 4.5 V, V_{CC} = Vin 25 °C	-0.25		+0.25	%
		Overtemperature range	-0.5		+0.5	
Temp_acc	Internal temperature sensor accuracy		-3		3	°C
Digital I/O pins (SCL, SDA, ALM, RSTIO)						
Vih	Input logic high		1.2			V
Vil	Input logic low				0.35	
Vol	Output logic low (SDA, ALM, RSTIO)	Iol = 4 mA			0.4	
BATD/CD pin						
Vith	Input threshold voltage		1.46	1.61	1.76	V
Vihyst	Input voltage hysteresis			0.1		
Voh	Output logic high (charge inhibit mode enable)	Ioh = 3 mA			Vbat-0.4	

Table 5. I^2C timing - V_{IO}= 2.8 V, T_{amb} = -20 °C to 70 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6			µs
t_{low}	LOW period of the SCL clock	1.3			
t_{high}	HIGH period of the SCL clock	0.6			
$t_{su,sta}$	Setup time for repeated START condition	0.6			
$t_{hd,dat}$	Data hold time	0		0.9	
$t_{su,dat}$	Data setup time	100			ns
t_r	Rise time of both SDA and SCL signals	20+ 0.1C_b		300	ns
t_f	Fall time of both SDA and SCL signals	20+ 0.1C_b		300	ns
$t_{su,sto}$	Setup time for STOP condition	0.6			µs
t_{buf}	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF

Figure 3. I²C timing diagram



5 Application information

Figure 4. Example of an application schematic using the STC3115 in mixed mode

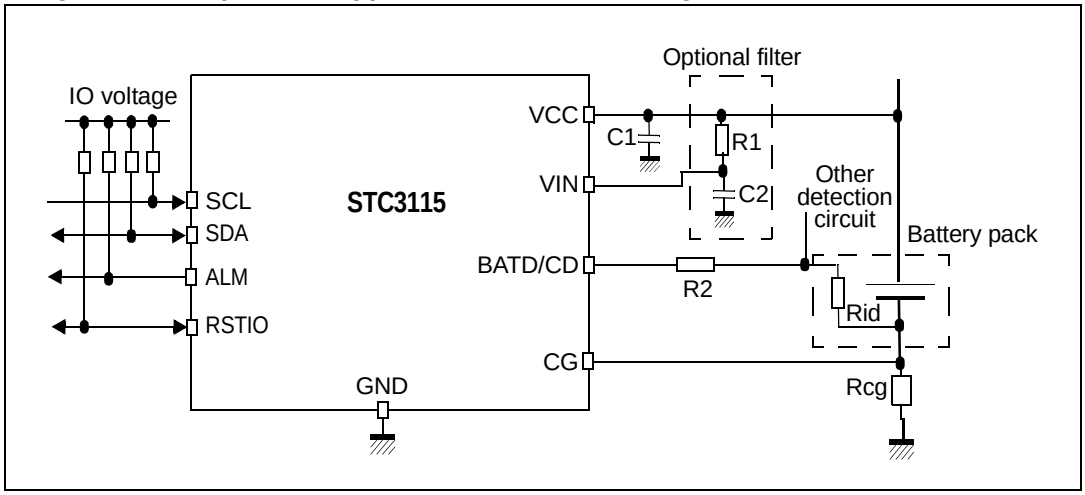


Table 6. External component list

Name	Value	Tolerance	Comments
Rcg	5 to 50 mΩ	1% to 5%	Current sense resistor (2% or better recommended)
C1	1 µF		Supply decoupling capacitor
C2	220 nF		Battery voltage input filter (optional)
R1	1 kΩ		Battery voltage input filter (optional)
R2	1 kΩ		Battery detection function

Figure 5. Example of an application schematic using the STC3115 without current sensing

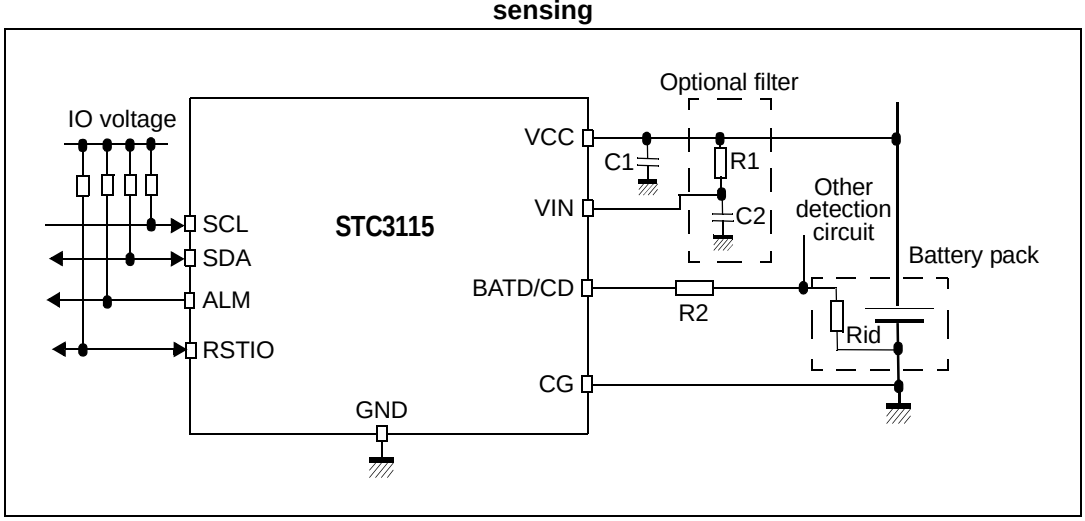
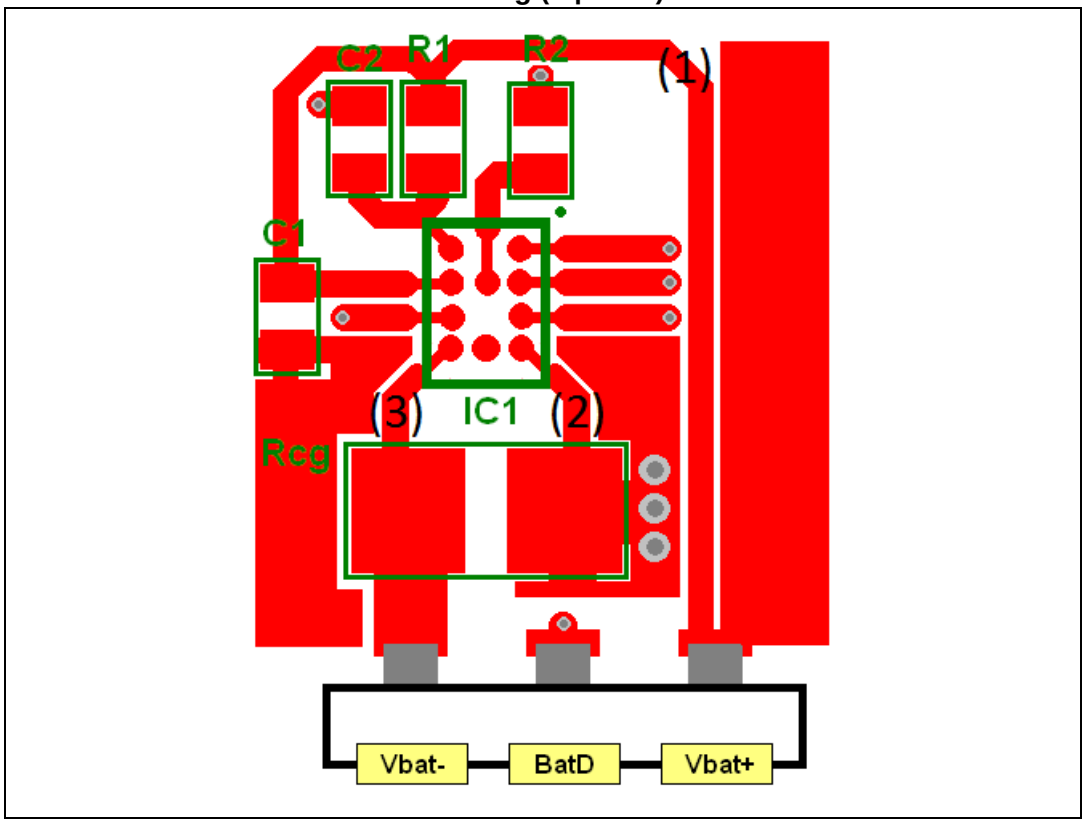


Table 7. External component list

Name	Value	Comments
C1	1 µF	Supply decoupling capacitor
C2	220 nF	Battery voltage input filter (optional)
R1	1 kΩ	
R2	1 kΩ	Battery detection function

Figure 6. Example of an application layout using the STC3115 with current sensing (top view)



1. This track is a dedicated power supply track for the STC3115 system which, for voltage measurement accuracy, is isolated from the application Vbat plane.
2. The STC3115 GND pin should be connected to the RCG only and for current measurement accuracy, it should be isolated from the ground plane.
3. The STC3115 CG pin should be connected to the RCG first and for current measurement accuracy, it should be isolated from the battery minus power path.

Note: For a detailed explanation of the RCG layout, please refer to the AN4324 (place and route guidelines).

6 Functional description

6.1 Battery monitoring functions

6.1.1 Operating modes

The monitoring functions include the measurement of battery voltage, current, and temperature. A Coulomb counter is available to track the SOC when the battery is charging or discharging at a high rate. A sigma-delta A/D converter is used to measure the voltage, current, and temperature.

The STC3115 can operate in two different modes with different power consumption (see *Table 8*. Mode selection is made by the VMODE bit in register 0 (refer to *Table 13* for register 0 definition).

Table 8. STC3115 operating modes

VMODE	Description
0	Mixed mode, Coulomb counter is active, voltage gas gauge runs in parallel
1	Voltage gas gauge with power saving Coulomb counter is not used. No current sensing.

In mixed mode, current is measured continuously (except for a conversion cycle every 4 s and every 16 s seconds for measuring voltage and temperature respectively). This provides the highest accuracy from the gas gauge.

In voltage mode with no current sensing, a voltage conversion is made every 4 s and a temperature conversion every 16 s. This mode provides the lowest power consumption.

It is possible to switch between the two operating modes to get the best accuracy during active periods, and to save power during standby periods while still keeping track of the SOC information.

6.1.2 Battery voltage monitoring

Battery voltage is measured by using one conversion cycle of the A/D converter every 4 s.

The conversion cycle takes 2^{13} = 8192 clock cycles. Using the 32768 Hz internal clock, the conversion cycle time is 250 ms.

The voltage range is 0 to 4.5 V and resolution is 2.20 mV. Accuracy of the voltage measurement is ±0.5% over the temperature range. This allows accurate SOC information from the battery open-circuit voltage.

The result is stored in the REG_VOLTAGE register (see *Table 12*).

6.1.3 Internal temperature monitoring

The chip temperature (close to the battery temperature) is measured using one conversion cycle of the A/D converter every 16 s.

The conversion cycle takes 2^{13} = 8192 clock cycles. Using the 32768 Hz internal clock, the conversion cycle time is 250 ms. Resolution is 1° C and range is -40 to +125 °C.

The result is stored in the REG_TEMPERATURE register (see *Table 12*).

6.1.4 Current sensing

Voltage drop across the sense resistor is integrated during a conversion period and input to the 14-bit sigma-delta A/D converter.

Using the 32768 Hz internal clock, the conversion cycle time is 500 ms for a 14-bit resolution. The LSB value is 5.88 µV. The A/D converter output is in two's complement format.

When a conversion cycle is completed, the result is added to the Coulomb counter accumulator and the number of conversions is incremented in a 16-bit counter.

The current register is updated only after the conversion closest to the voltage conversion (that is: once per 4-s measurement cycle). The result is stored in the REG_CURRENT register (see *Table 12*).

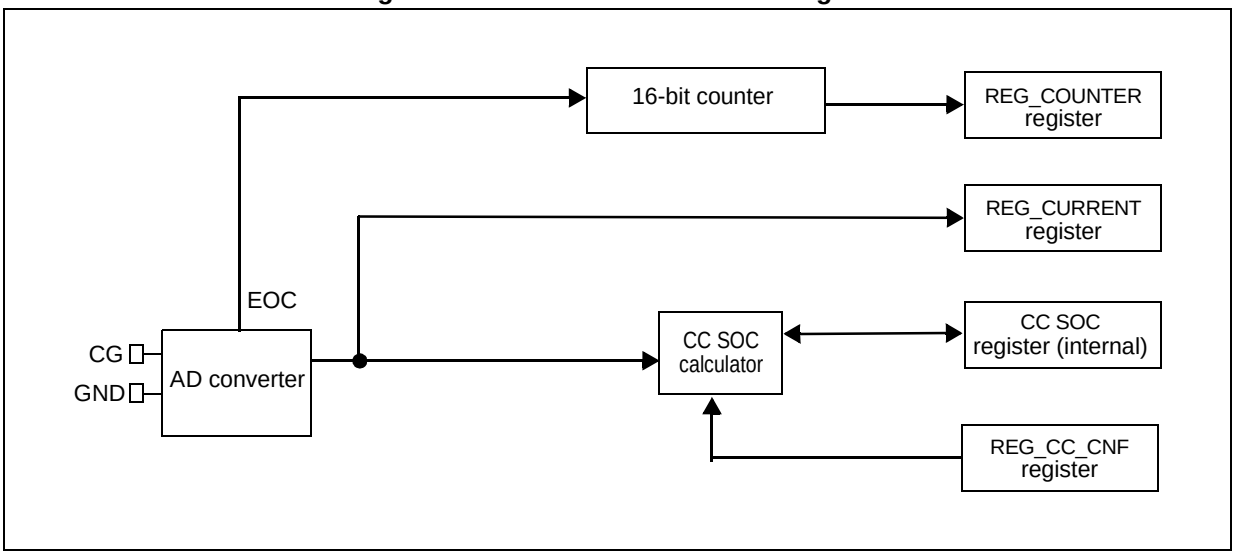
6.2 STC3115 gas gauge architecture

6.2.1 Coulomb counter

The Coulomb counter is used to track the SOC of the battery when the battery is charging or discharging at a high rate. Each current conversion result is accumulated (Coulomb counting) for the calculation of the relative SOC value based on the configuration register.

The system controller can control the Coulomb counter and set and read the SOC register through the I^2C control registers.

Figure 7. Coulomb counter block diagram



The REG_CC_CNF value depends on battery capacity and the current sense resistor. It scales the charge integrated by the sigma delta converter into a percentage value of the battery capacity. The default value is 395 (corresponding to a 10 mΩ sense resistor and 1957 mA.h battery capacity).

The Coulomb counter is inactive if the VMODE bit is set, this is the default state at power-on-reset (POR) or reset (VMODE bit = 1).

Writing a value to the register REG_SOC (mixed mode SOC) forces the Coulomb counter gas gauge algorithm to restart from this new SOC value.

REG_CC_CNF register is a 16-bit integer value and is calculated as shown in *Equation 1*:

Equation 1

$$REG\_CC\_CNF = Rsense \times Cnom / 49.556$$

Rsense is in mΩ and Cnom is in mA.h

Example: Rsense =10 mΩ, Cnom = 1650 mA.h, REG_CC_CNF = 333

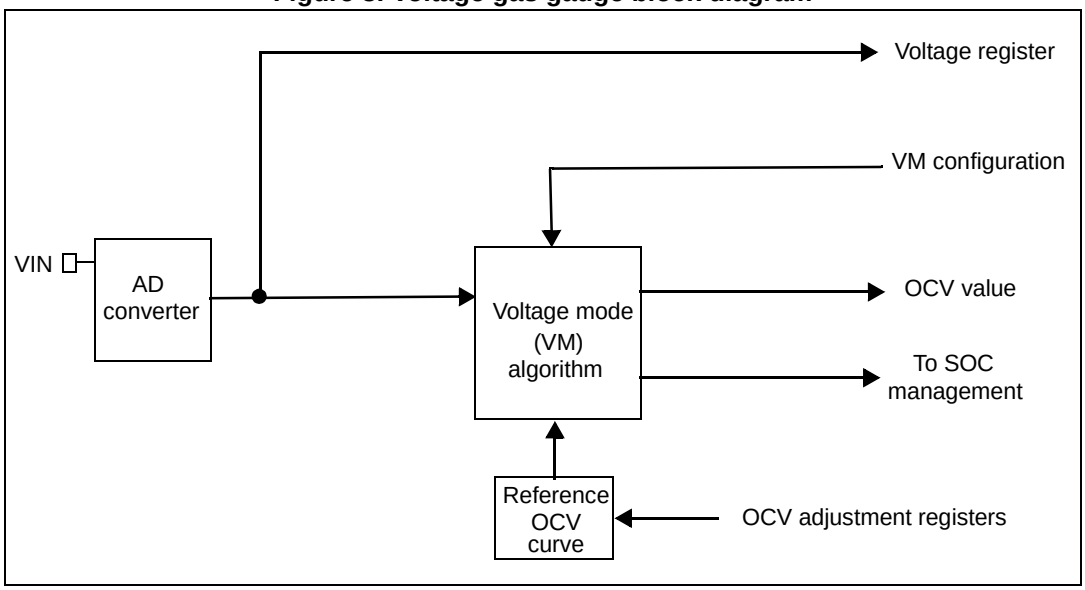
6.2.2 Voltage gas gauge algorithm

No current sensing is needed for the voltage gas gauge. An internal algorithm precisely simulates the dynamic behavior of the battery and provides an estimation of the OCV. The battery SOC is related to the OCV by means of a high-precision reference OCV curve built into the STC3115.

Any change in battery voltage causes the algorithm to track both the OCV and SOC values, taking into account the non-linear characteristics and time constants related to the chemical nature of the Li-Ion and Li-Po batteries.

A single parameter fits the algorithm to a specific battery. The default value provides good results for most battery chemistries used in hand-held applications.

Figure 8. Voltage gas gauge block diagram



Voltage gas gauge algorithm registers

The REG_VM_CNF configuration register is used to configure the parameter used by the algorithm based on battery characteristic. The default value is 321.

The REG_OCV register holds the estimated OCV value corresponding to the present battery state.

The REG_OCVTAB registers are used to adjust the internal OCV table to a given battery type.

The REG_VM_CNF register is a 12-bit integer value and is calculated from the averaged internal resistance and nominal capacity of the battery as shown in *Equation 2*:

Equation 2

$$REG\_VM\_CNF = Ri \times Cnom / 977.78$$

Ri is in mΩ and Cnom is in mA.h

Example: Ri = 190 mΩ, Cnom =1650 mA.h, REG_VM_CNF = 321

6.2.3 Mixed mode gas gauge system

The STC3115 provides a mixed mode gas gauge using both a Coulomb counter (CC) and a voltage-mode (VM) algorithm to track the SOC of the battery in all conditions with optimum accuracy. The STC3115 directly provides the SOC information.

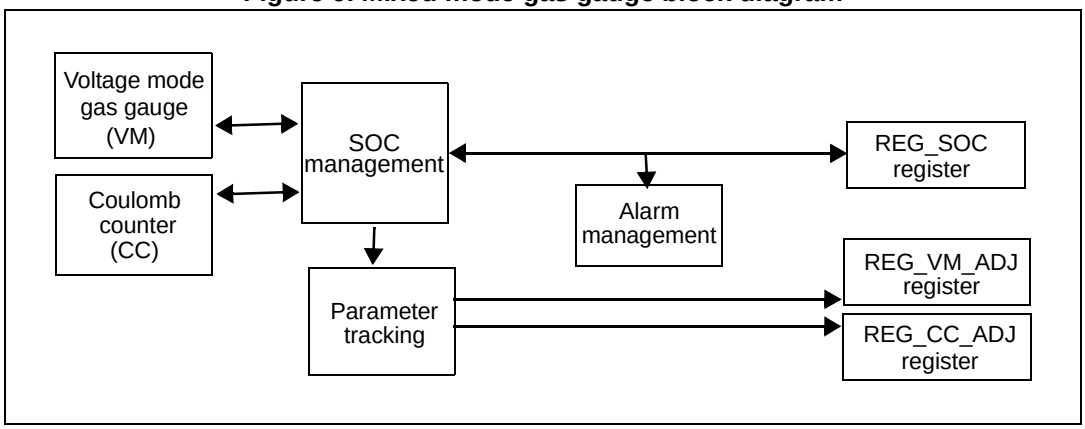
The Coulomb counter is mainly used when the battery is charging or discharging at a high rate. Each current conversion result is accumulated (Coulomb counting) for the calculation of the relative SOC value based on a configuration register.

The voltage-mode algorithm is used when the application is in low power consumption state.

The STC3115 automatically uses the best method in any given application condition.

However, when the application enters standby mode, the STC3115 can be put in power-saving mode: only the voltage-mode gas gauge stays active, the Coulomb counter is stopped and power consumption is reduced.

Figure 9. Mixed mode gas gauge block diagram



The combination of the CC and VM algorithms provides optimum accuracy under all application conditions. The voltage gas gauge cancels any long-term errors and prevents the SOC drift problem that is commonly found in Coulomb counter only solutions.

Furthermore, the results of the two algorithms are continuously compared and adjustment factors are calculated. This enables the application to track the CC and VM algorithm parameters for long-term accuracy, automatically compensating for battery aging, application condition changes, and temperature effects. Five registers are dedicated to this monitoring:

- REG_CC_ADJ and REG_VM_ADJ are continuously updated. They are signed, 16-bit, user-adjusted registers with LSB = 1/512%.
- ACC_CC_ADJ and ACC_VM_ADJ are updated only when a method switch occurs. They are signed, 16-bit user adjusted accumulators with LSB = 1/512%.
- RST_ACC_CC_ADJ and RST_ACC_VM_ADJ bits in the REG_MODE register are used to clear the associated counter.

6.3 Low battery alarm

The ALM pin provides an alarm signal in case of a low battery condition. The output is an open drain and an external pull-up resistor is needed in the application. Writing the IO0DATA bit to 0 forces the ALM output low; writing the IO0DATA bit to 1 lets the ALM output reflect the battery condition. Reading the IO0DATA bit gives the state of the ALM pin.

When the IO0DATA bit is 1, the ALM pin is driven low if either of the following two conditions is met:

- The battery SOC estimation from the mixed algorithm is less than the programmed threshold (if the alarm function is enabled by the ALM_ENA bit).
- The battery voltage is less than the programmed low voltage level (if the ALM_ENA bit is set).

When a low-voltage or low-SOC condition is triggered, the STC3115 drives the ALM pin low and sets the ALM_VOLT or ALM_SOC bit in REG_CTRL.

The ALM pin remains low (even if the conditions disappear) until the software writes the ALM_VOLT and ALM_SOC bits to 0 to clear the interrupt.

Clearing the ALM_VOLT or ALM_SOC while the corresponding low-voltage or low-SOC condition is still in progress does not generate another interrupt; this condition must disappear first and must be detected again before another interrupt (ALM pin driven low) is generated for this alarm. Another alarm condition, if not yet triggered, can still generate an interrupt.

Usually, the low-SOC alarm occurs first to warn the application of a low battery condition, then if no action is taken and the battery discharges further, the low-voltage alarm signals a nearly-empty battery condition.

At power-up, or when the STC3115 is reset, the SOC and voltage alarms are enabled (ALM_ENA bit = 1). The ALM pin is high-impedance directly after POR and is driven low if the SOC and/or the voltage is below the default thresholds (1% SOC, 3.00 V voltage), after the first OCV measurement and SOC estimation.

The REG_SOC_ALM register holds the relative SOC alarm level in 0.5% units (0 to 100%). Default value is 2 (i.e. 1% SOC).

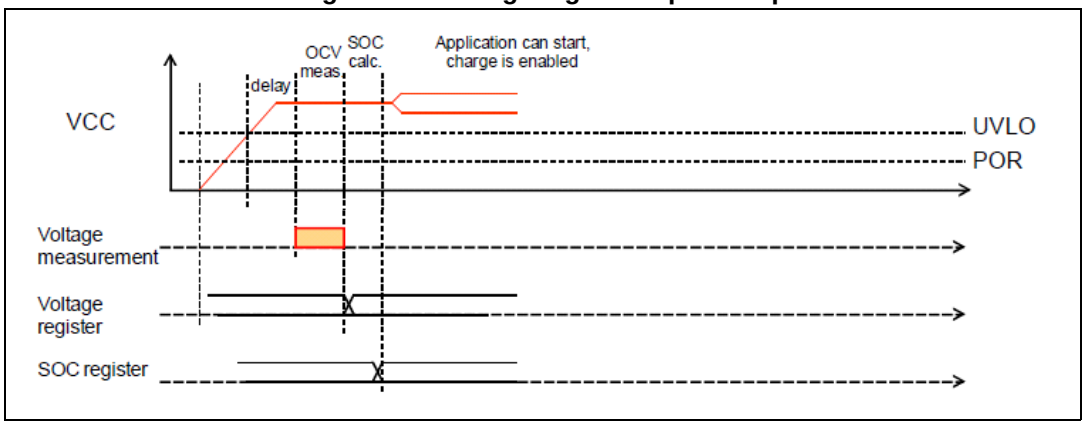
The REG_ALARM_VOLTAGE holds the low voltage threshold and can be programmed over the full scale voltage range with 17.60 (2.20 * 8) mV steps. The default value is 170 (3.00 V).

6.4 Power-up and battery swap detection

When the STC3115 is powered up at first battery insertion, an automatic battery voltage measurement cycle is made immediately after startup and debounce delay.

This feature enables the system controller to get the SOC of a newly inserted battery based on the OCV measured just before the system actually starts.

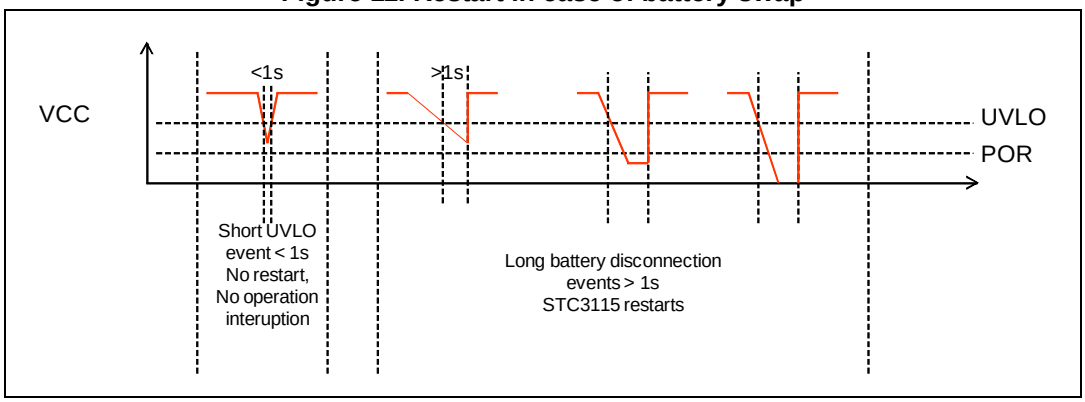
Figure 10. Timing diagram at power-up



A battery swap is detected when the battery voltage drops below the undervoltage lockout (UVLO) for more than 1 s. The STC3115 restarts when the voltage goes back above UVLO, in the same way as for a power-up sequence.

Such filtering provides robust battery swap detection and prevents restarting in case of short voltage drops. This feature protects the application against high surge currents at low temperatures.

Figure 11. Restart in case of battery swap



Example: When BATD/CD is high (voltage above the 1.61 V threshold) for more than 1 s, a battery swap is detected. The STC3115 restarts when the BATD/CD level returns below the threshold, in the same way as for a power-up sequence.

Using the 1-s filter prevents false battery swap detection if short contact bouncing occurs at the battery terminals due to mechanical vibrations or shocks.

6.5 Improving accuracy of the initial OCV measurement with the advanced functions of BATD/CD and RSTIO pins

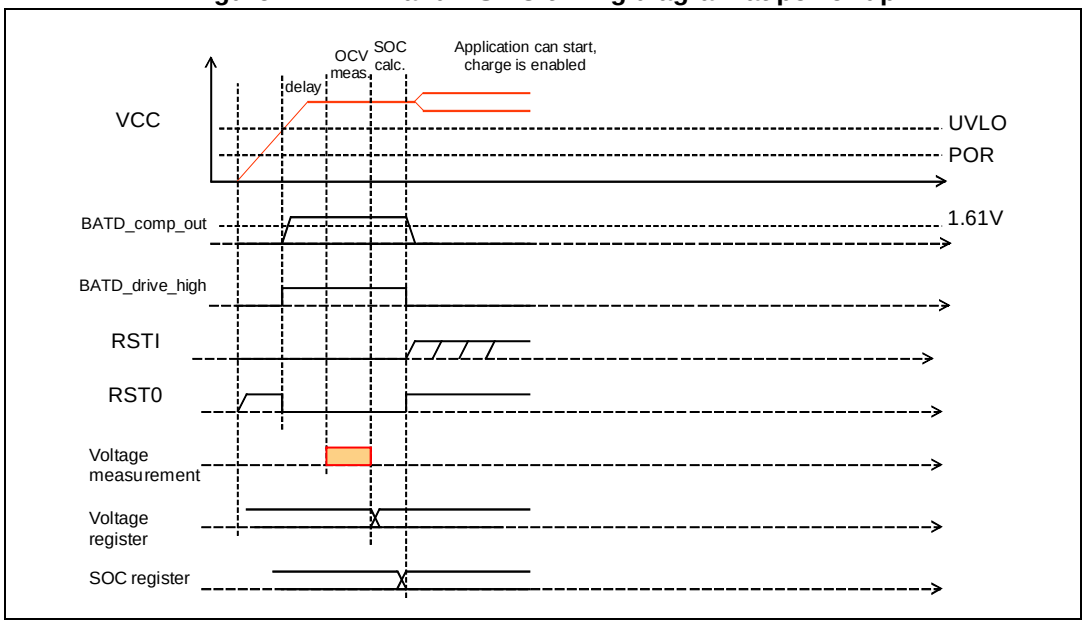
The advanced functions of the BATD/CD and RSTIO pins provide a way to ensure that the OCV measurement at power-up is not affected by the application startup or by the charger operation. This occurs as follows:

- The BATD/CD pin is driven high to V_{CC} voltage which inhibits the charge function (assuming that the BATD/CD signal is connected to disable input of the charger circuit).
- The RSTIO pin senses the system reset state and if the system reset is active (that is RSTIO is low), the RSTIO is kept low until the end of the OCV measurement.

Figure 12 describes the BATD/CD and RSTIO operation at power-up. Please refer to the block diagram of *Figure 13* for the RSTI, RSTO, BATD_comp_out, and BATD_drive_high signals.

At the end of the OCV measurement, the BATD/CD and RSTIO pin are released (high impedance), the application can start and the charger is enabled.

Figure 12. BATD and RSTIO timing diagram at power-up



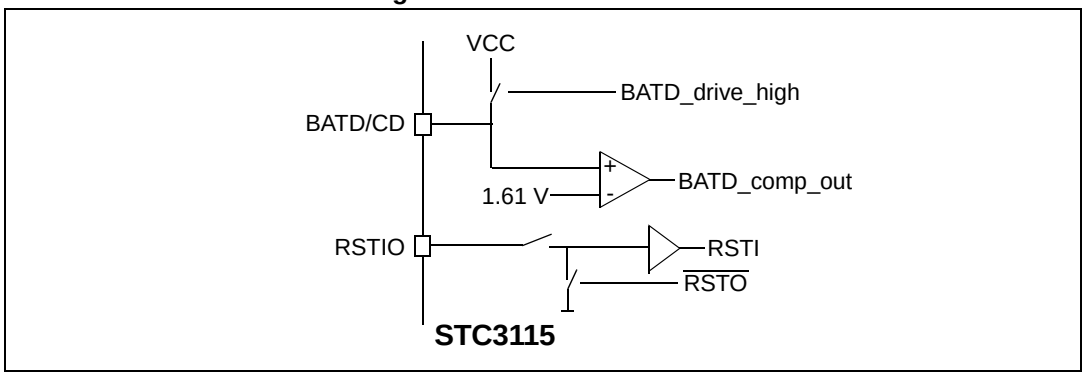
6.5.1 BATD and RSTIO pins

The STC3115 provides platform synchronization signals to provide reliable SOC information in different cases.

The BATD/CD pin senses the presence of the battery independently of the battery voltage and it controls the battery charger to inhibit the charge during the initial OCV measurement.

The RSTIO pin can be used to delay the platform startup during the first OCV measurement at battery insertion.

Figure 13. BATD and RSTIO



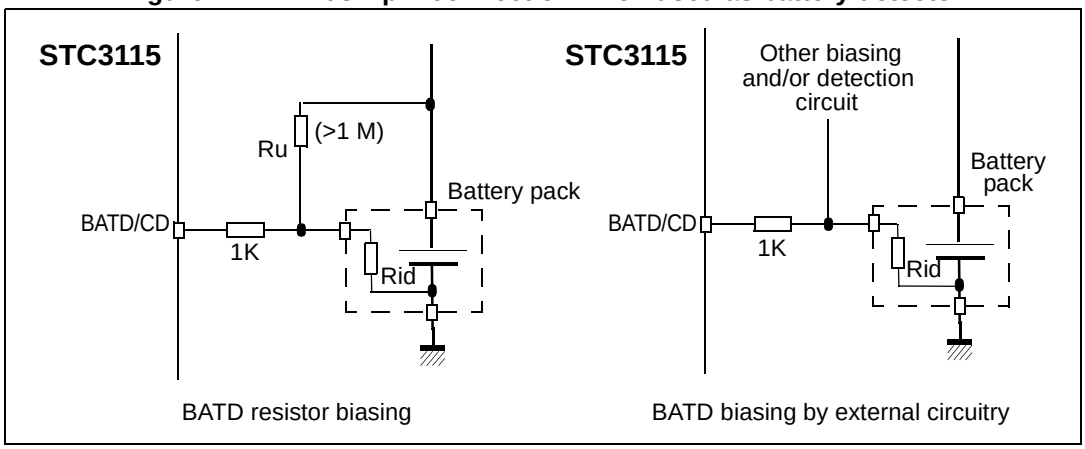
The BATD/CD pin used as a battery detector is an analog I/O.The input detection threshold is typically 1.61V.

BATD/CD is also an output connected to V_{CC} level when active. Otherwise, it is high impedance.

The RSTIO signal is used to control the application system reset during the initial OCV measurement. The RSTIO pin is a standard I/O pin with open drain output.

BATD/CD can be connected to the NTC sensor or to the identification resistor of the battery pack. The STC3115 does not provide any biasing voltage or current for the battery detection. An external pull-up resistor or another device has to pull the BATD/CD pin high when the battery is removed.

Figure 14. BATD/CD pin connection when used as battery detector



6.6

7 I²C interface

7.1 Read and write operations

The I²C interface is used to control and read the current accumulator and registers. It is compatible with the Philips I²C Bus® (version 2.1). It is a slave serial interface with a serial data line (SDA) and a serial clock line (SCL).

- SCL: input clock used to shift data
- SDA: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit. The default device address value is 1110 000. The STC3115 then sends an acknowledge at the end of an 8-bit long sequence. The next eight bits correspond to the register address followed by another acknowledge.

The data field is the last 8-bit long sequence sent, followed by a last acknowledge.

Table 9. Device address format

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	1	1	0	0	0	0	R/W

Table 10. Register address format

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

Table 11. Register data format

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 15. Read operation

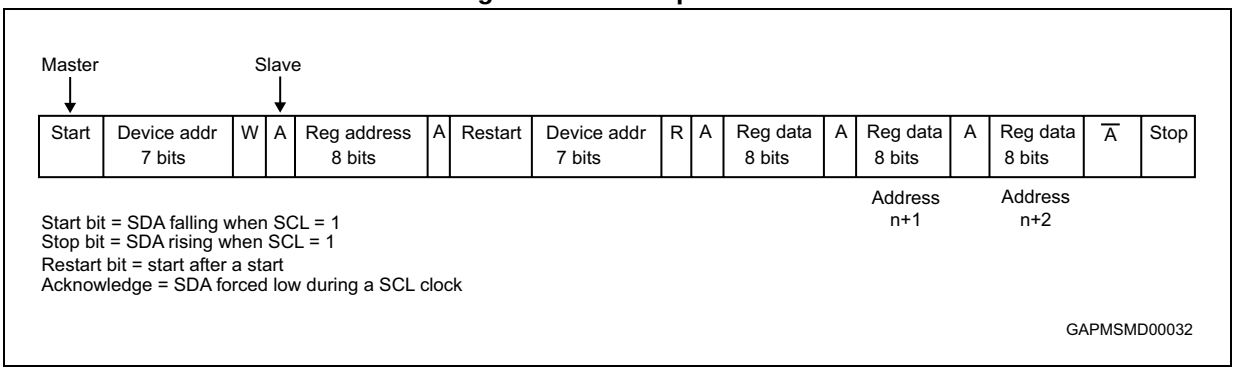
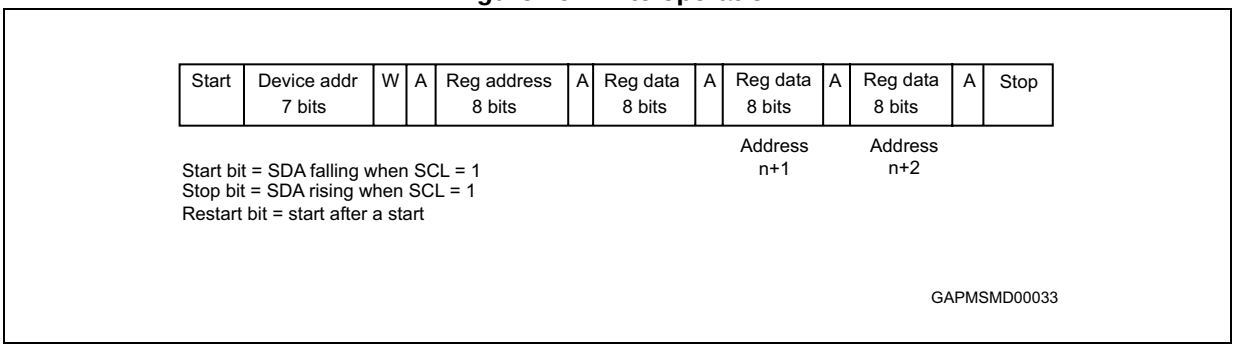


Figure 16. Write operation



7.2 Register map

7.2.1 Register map

The register space provides 30 control registers, 1 read-only register for device ID, 16 read/write RAM working registers reserved for the gas gauge algorithm, and 16 OCV adjustment registers. Mapping of all registers is shown in *Table 12*. Detailed descriptions of registers 0 (REG_MODE) and 1 (REG_CTRL) are shown in *Table 13* and *Table 14*. All registers are reset to default values at power-on or reset, and the PORDET bit in register REG_CTRL is used to indicate the occurrence of a power-on reset.

Table 12. Register map

Name	Address (decimal)	Type	POR	Soft POR	Description	LSB
Control registers	0 to 23					
REG_MODE	0	R/W			Mode register	
REG_CTRL	1	R/W			Control and status register	
REG_SOC (L-H)	2-3	R/W			Gas gauge relative SOC	1/512%
REG_COUNTER (L-H)	4-5	R	0x00	0x00	Number of conversions (2 bytes)	500 ms
REG_CURRENT (L-H)	6-7	R	0x00	0x00	Battery current value (2 bytes)	5.88 µV
REG_VOLTAGE (L-H)	8-9	R	0x00	0x00	Battery voltage value (2 bytes)	2.2 mV
REG_TEMPERATURE	10	R	0x00	0x00	Temperature data	1 °C
REG_CC_ADJ_HIGH	11	R	0x00	0x00	Coulomb counter adjustment factor	1/2%
REG_VM_ADJ_HIGH	12	R	0x00	0x00	Voltage mode adjustment factor	
REG_OCV (L-H)	13-14	R/W	0x00	0x00	OCV register (2 bytes)	0.55 mV
REG_CC_CNF (L-H)	15-16	R/W	395	395	Coulomb counter gas gauge configuration	
REG_VM_CNF (L-H)	17-18	R/W	321	321	Voltage gas gauge algorithm parameter	
REG_ALARM_SOC	19	R/W	0x02	0x02	SOC alarm level (default = 1%)	1/2%
REG_ALARM_VOLTAGE	20	R/W	0xAA	0xAA	Battery low voltage alarm level (default is 3 V)	17.6 mV
REG_CURRENT_THRES	21	R/W	0x0A	0x0A	Current threshold for the relaxation counter	47.04 µV
REG_RELAX_COUNT	22	R	0x78	0x78	Relaxation counter	
REG_RELAX_MAX	23	R/W	0x78	0x78	Relaxation counter max value	
REG_ID	24	R	0x14	0x14	Part type ID = 14h	

Table 12. Register map (continued)

Name	Address (decimal)	Type	POR	Soft POR	Description	LSB
REG_CC_ADJ_LOW	25	R	0x00	0x00	Coulomb counter adjustment factor	1/512%
REG_VM_ADJ_LOW	26	R	0x00	0x00	Voltage mode adjustment factor	
ACC_CC_ADJ (L-H)	27-28	R	0x00	0x00	Coulomb Counter correction accumulator	
ACC_VM_ADJ (L-H)	29-30	R	0x00	0x00	Voltage mode correction accumulator	
RAM registers	32 to 47					
REG_RAM0	32	R/W	Random	Unchanged	Working register 0 for gas gauge	
...	...				...	
REG_RAM15	47	R/W	Random	Unchanged	Working register 15 for gas gauge	
OCV adjustment registers						
REG_OCVTAB	48 to 63	R/W	0x00	0x00	OCV adjustment table (16 registers)	0.55 mV

7.2.2 Register description

Values held in consecutive registers (such as the charge value in the REG_SOC register pair) are stored with low bits in the first register and high bits in the second register. The registers must be read with a single I^2C access to ensure data integrity. It is possible to read multiple values in one I^2C access. All values must be consistent.

The SOC data are coded in binary format and the LSB of the low byte is 1/512 %. The battery current is coded in 2's complement format and the LSB value is 5.88 µV. The battery voltage is coded in 2's complement format and the LSB value is 2.20 mV. The temperature is coded in 2's complement format and the LSB value is 1°C.

Table 13. REG_MODE - address 0

Name	Position	Type	Def.	Description
VMODE	0	R/W	1	0: Mixed mode (Coulomb counter active) 1: Power saving voltage mode
CLR_VM_ADJ	1	R/W	0	Write 1 to clear ACC_VM_ADJ and REG_VM_ADJ. Auto clear bit if GG_RUN = 1
CLR_CC_ADJ	2	R/W	0	Write 1 to clear ACC_CC_ADJ and REG_CC_ADJ Auto clear bit if GG_RUN = 1
ALM_ENA	3	R/W	1	Alarm function 0: Disabled 1: Enabled
GG_RUN	4	R/W	0	0: Standby mode. Accumulator and counter registers are frozen, gas gauge and battery monitor functions are in standby. 1: Operating mode
FORCE_CC	5	R/W	0	Forces the mixed mode relaxation timer to switch to the Coulomb counter mode. Write 1, self clear to 0 Relaxation counter = 0
FORCE_VM	6	R/W	0	Forces the mixed mode relaxation timer to switch to voltage gas gauge mode. Write 1, self clear to 0 Relaxation counter = Relax_max
	7			Unused

Table 14. REG_CTRL - address 1

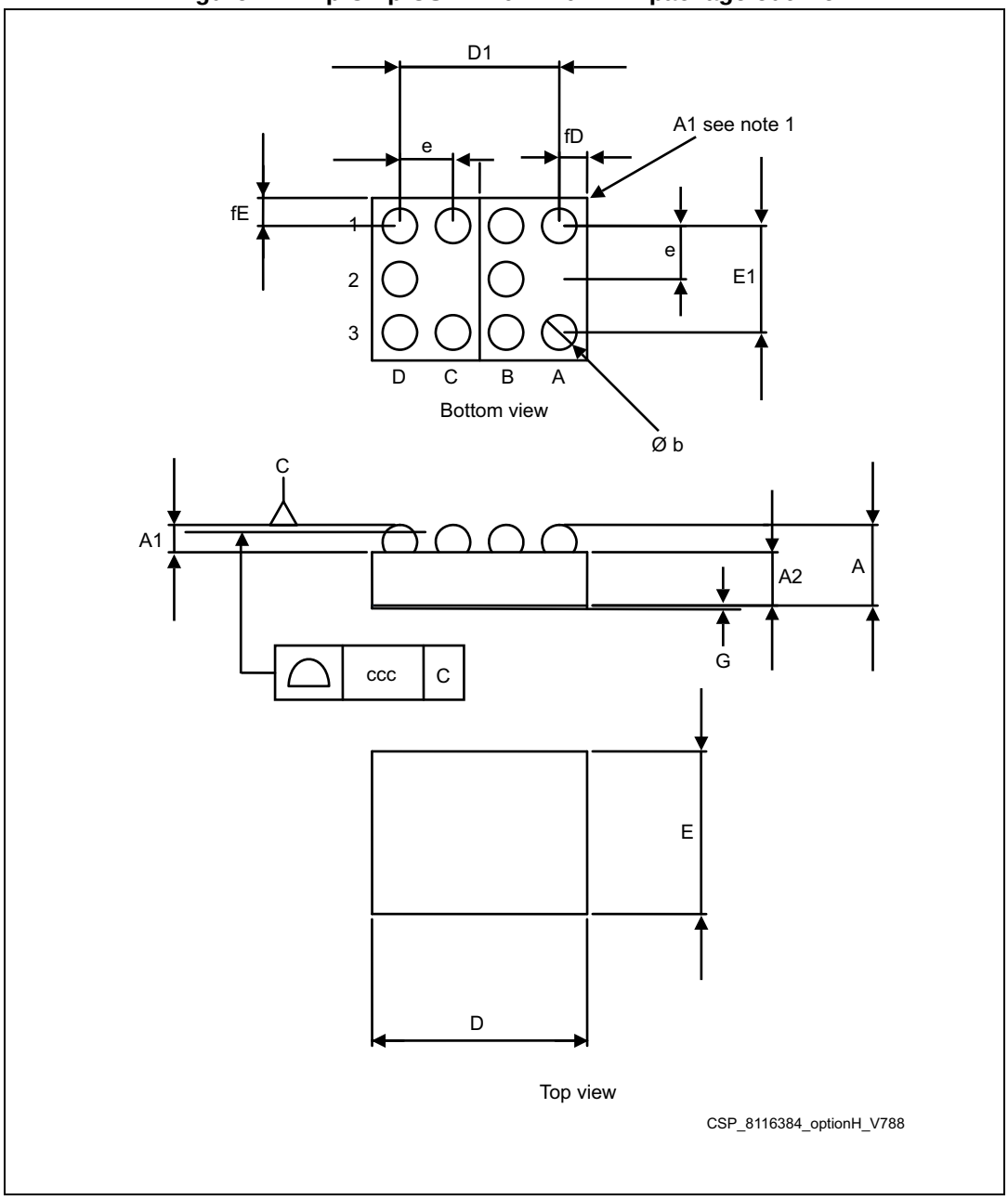
Name	Position	Type	Def.	Description
IO0DATA	0	R	X	ALM pin status 0 = ALM input is low 1 = ALM input is high
		W	1	ALM pin output drive 0 = ALM is forced low 1 = ALM is driven by the alarm conditions
GG_RST	1	W	0	0: no effect 1: resets the conversion counter GG_RST is a self-clearing bit
GG_VM	2	R	0	Voltage mode active 0 = REG_SOC from Coulomb counter mode 1 = REG_SOC from Voltage mode
BATFAIL	3	R/W	0	Battery removal or UVLO detection bit. Write 0 to clear (Write 1 is ignored)
PORDET	4	R	1	Power on reset (POR) detection bit 0 = no POR event occurred 1 = POR event occurred
		W	0	Soft reset 0 = release the soft-reset and clear the POR detection bit 1 = assert the soft-reset and set the POR detection bit. This bit is self clearing.
ALM_SOC	5	R/W	0	Set with a low-SOC condition Cleared by writing 0
ALM_VOLT	6	R/W	0	Set with a low-voltage condition Cleared by writing 0
	7			Unused

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 Flip Chip CSP 1.40 x 2.04 mm package information

Figure 17. Flip Chip CSP 1.40 x 2.04 mm package outline

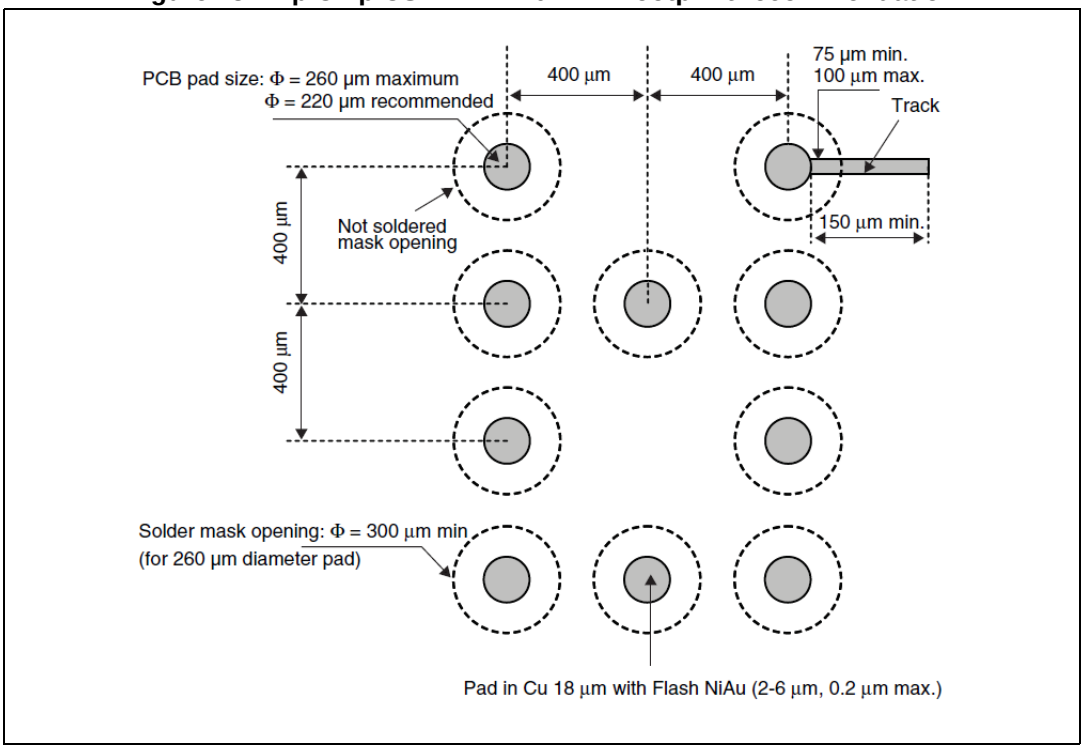


1. The terminal A1 on the bump side is identified by a distinguishing feature - for instance, by a circular “clear area” typically 0.1 mm in diameter and/or a missing bump.
2. The terminal A1, on the back side, is identified by a distinguishing feature - for instance, by a circular “clear area” typically 0.2 mm in diameter depending on the die size.

Table 15. Flip Chip CSP 1.4 x 2.04 mm package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.545	0.600	0.655	0.021	0.024	0.026
A1	0.165	0.200	0.235	0.006	0.008	0.009
A2	0.330	0.350	0.370	0.013	0.014	0.015
b	0.220	0.260	0.300	0.009	0.010	0.012
D	1.98	2.01	2.04	0.078	0.079	0.080
D1		1.20			0.047	
E	1.34	1.37	1.40	0.053	0.054	0.055
E1		0.800			0.031	
e	0.360	0.400	0.440	0.014	0.016	0.017
fD	0.395	0.405	0.415	0.016	0.016	0.016
fE	0.275	0.285	0.295	0.011	0.011	0.012
G		0.025			0.001	
ccc			0.050			0.002

Figure 18. Flip Chip CSP 1.4 x 2.04 mm footprint recommendation



8.2 DFN10 2.0 x 3.0 mm package information

Figure 19. DFN10 2.0 x 3.0 mm package outline

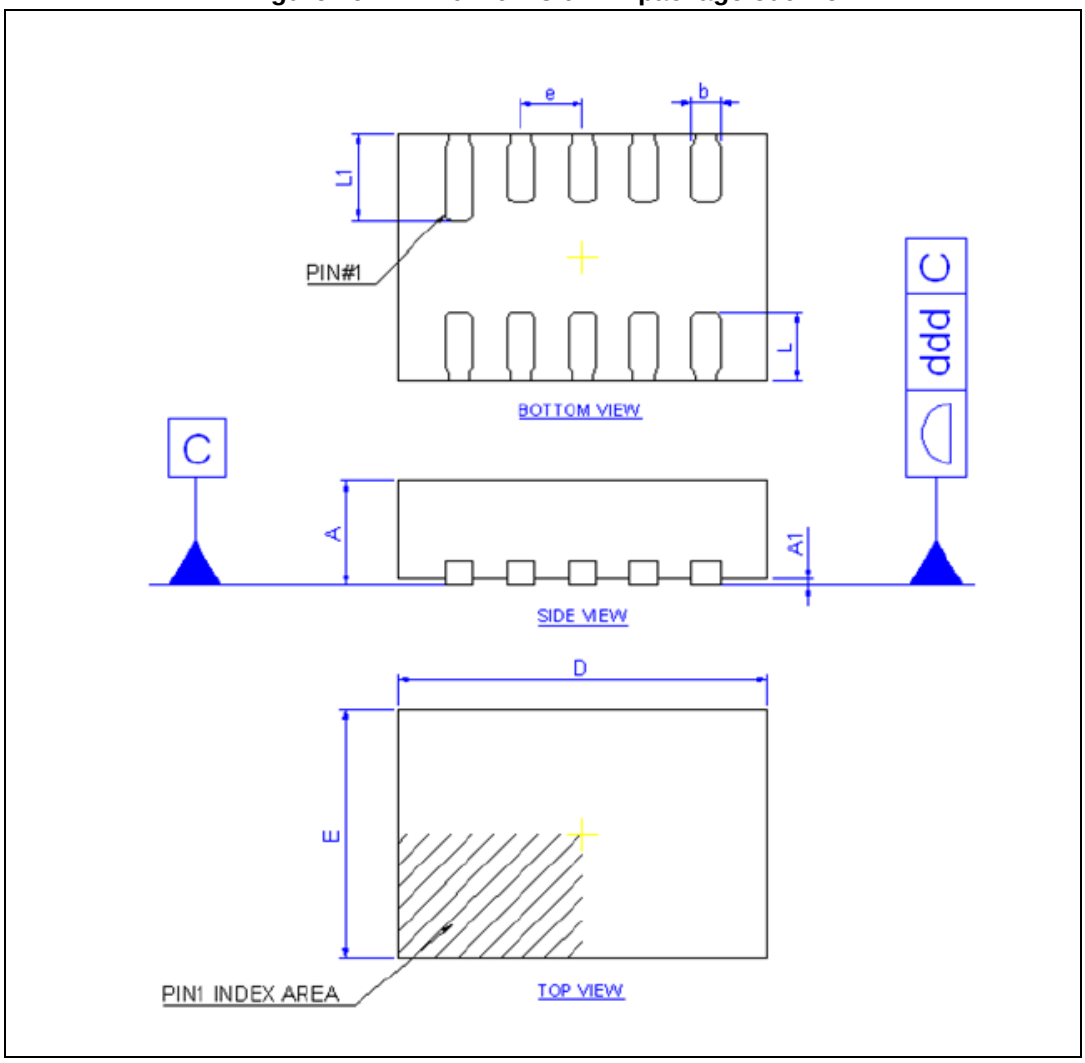
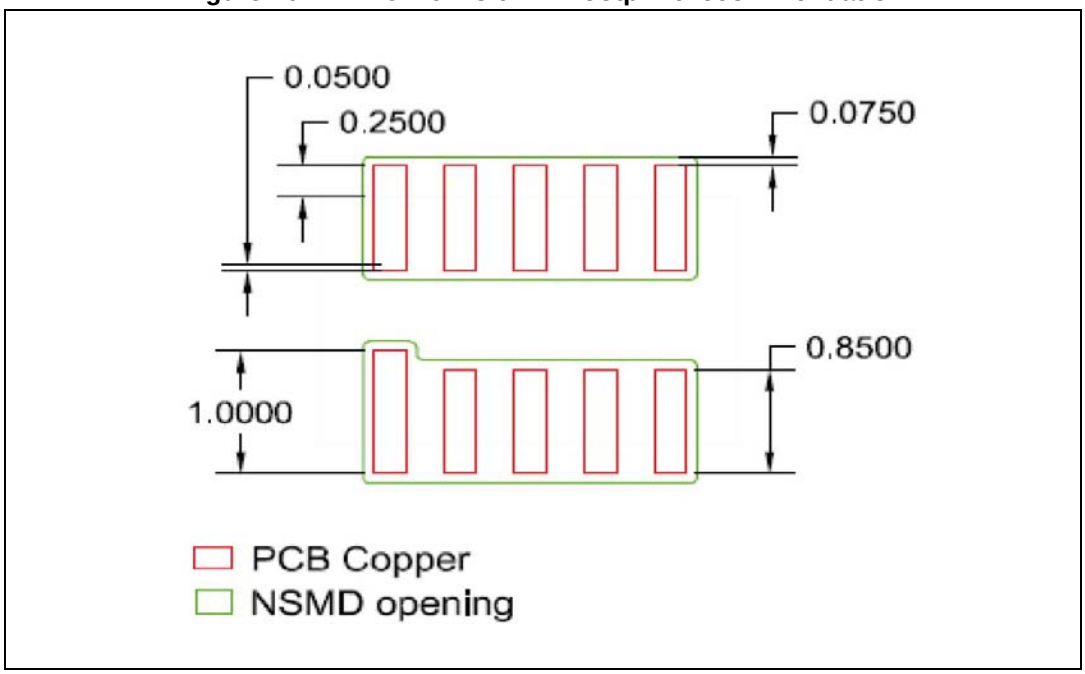


Table 16. DFN10 2.0 x 3.0 mm package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.5	0.55	0.60	0.020	0.022	0.024
A1	0.00		0.05	0.000		0.002
b	0.15	0.23	0.30	0.006	0.009	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.90	2.00	2.10	0.075	0.079	0.083
e		0.50			0.020	
L	0.45	0.505	0.65	0.018	0.020	0.026
L1	0.60	0.70	0.80	0.024	0.028	0.031
ddd			0.080			0.003

Figure 20. DFN10 2.0 x 3.0 mm footprint recommendation



9 Ordering information

Table 17. Order code

Order code	Temperature range	Package	Packing	Marking
STC3115IJT(1)	-40 °C to +85 °C	CSP-10	Tape and reel	O22
STC3115AIJT(2)				O23
STC3115IQT(1)		DFN10 2x3		O204
STC3115AIQT(2)				O205

1. 4.35 V max. battery option (3.8 V typ.).
2. 4.20 V max. battery option (3.7 V typ.).

Note: For a detailed explanation on versions A and non-A, please refer to the AN4324.

10 Revision history

Table 18. Document revision history

Date	Revision	Changes
22-Nov-2012	1	Initial release
07-Feb-2013	2	*Table 4*: added “BATD” and “CD” *Section 6.4*: removed option “RSTIO/BATD” *Section 6.5*: added “BATD” and “CD” *Section 6.5.1*: removed option 2 (BATD/CD is disabled) and 3 (BATD and RSTIO); removed *Figure: BATD and RSTIO - option 2*, *Figure: BATD and RSTIO - option 3*, and *Figure: RSTIO/BATD pin connection when used as battery detector - option 1 and 2*; updated text with respect to BATD/CD. Removed *Section: Register map (Device 0x13) - engineering samples*. Updated *Table 12* Removed *Table: REG_MODE - address 0 (Device 0x13)* Removed *Table: Internal default OCV table and OCV offset registers.* Removed *Equation 3*. Replaced *Figure 17: Flip Chip CSP 1.40 x 2.04 mm package mechanical drawing*. Updated *Table 15: Flip Chip CSP 1.4 x 2.04 mm package mechanical data*. Updated *Table 17: Order code*
30-Oct-2013	3	Replaced silhouette Updated *Features* Updated *Equation 1* Updated example of *Equation 2* Updated disclaimer
28-Jan-2014	4	Corrected typographical error in document title.
08-Aug-2014	5	Added DFN10 2.0 mm x 3.0 mm package
06-Oct-2014	6	*Section 5: Application information*: added *Figure 6* and note relating to AN4324. Updated *Section 7.1: Read and write operations* Updated *Table 12: Register map*
17-Dec-2014	7	Removed the BATD option when it occurred with RSTIO *Figure 13: BATD and RSTIO*: added STC3115 Updated text and *Table 9: Device address format* of *Section 7.1: Read and write operations*. Updated text and *Table 12: Register map* of *Section 7.2.1: Register map*. Updated text of *Section 7.2.2: Register description* Updated *Table 17: Order code*

Table 18. Document revision history (continued)

Date	Revision	Changes
10-Nov-2017	8	Updated $t_{su,sta}$ symbol in *Table 5: I^2C timing - V_{IO}= 2.8 V, T_{amb} = -20 °C to 70 °C (unless otherwise specified)*.
15-Jan-2018	9	Inserted note in *Section 9: Ordering information*.

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