TABLE OF CONTENTS

REVISION HISTORY

7/2019—Rev. A to Rev. B

Changes to Ordering Guide ... 39

4/2019—Rev. 0 to Rev. A

Added 48-lead LQFP ... Universal
Change to General Description Section ... 1
Change to Figure 2 ... 4
Change to DET Output Low Voltage Parameter, Table 1 ... 5
Changes to Switch Node Parameter, Valley Current Limit Parameter, and Reset Threshold Hysteresis Parameter, Table 2 ... 6
Change to Gain Drift Parameter, Table 3 ... 7
Added VTRPL Current Parameter, Table 3 and Endnote 3 to Analog Trip, VTRPL Current Parameter, Table 3; Renumbered Sequentially ... 7
Change to Input Offset Parameter, Table 4 ... 8
Changes to Table 5 and Table 6 ... 9

Added Figure 4; Renumbered Sequentially 10
Changes to Table 7 10
Changes to Typical Performance Characteristics Section, Figure 6, and Figure 9 12
Change to Figure 13 13
Change to Figure 18 and Figure 21 14
Replaced Figure 23 15
Changes to Theory of Operation Section and Power Detection Section 22
Changes to Analog Trip Protection Section and Figure 68 24
Added Endnote 1 and Endnote 2 to Table 13 27
Changes to Boost Shunt Controller Output Voltage Section and Buck Regulator Output Voltage Section 28
Changes to VPTH Resistor Divider Section, Dummy Load Resistor Setting Section, and Sense Resistor Setting Section 31
Changes to Circuit Board Layout Recommendations Section 33
Changes to Figure 75 36
Updated Outline Dimensions 38
Changes to Ordering Guide 38

9/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

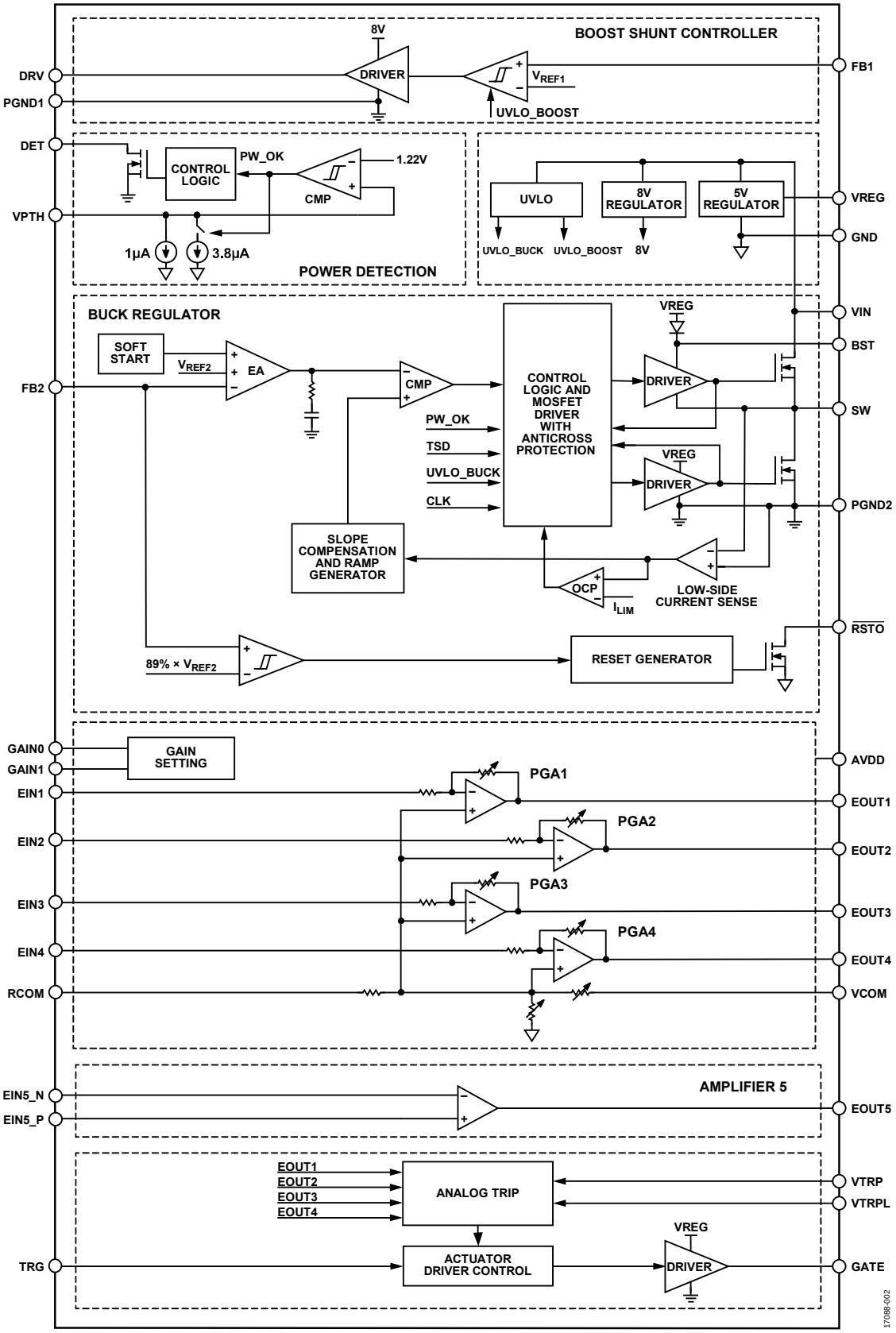


Figure 2. Functional Block Diagram

SPECIFICATIONS

BOOST SHUNT CONTROLLER AND POWER DETECTION SPECIFICATIONS

V_{IN} = 12 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT		VIN pin				
Input Voltage Range	V_{IN}		4.5		36	V
Quiescent Current[1]	I_{Q_VIN}	V_{IN} =12 V, FB1 = GND, FB2 = 0.65 V, no switching		1.35		mA
Undervoltage Lockout Threshold (UVLO)[2]						
VIN Rising				2.5	2.7	V
VIN Falling			2.2	2.4		V
FEEDBACK (FB1)						
FB1 Regulation Voltage	V_{FB1}	Falling	1.182	1.2	1.218	V
FB1 Hysteresis				19		mV
FB1 Bias Current	I_{FB1}			0.01	0.1	µA
Hysteresis Comparator Response Time				100		ns
BOOST SHUNT DRIVER (DRV)						
Rising Time[3]		C_{DRV} = 2.2 nF, from 0.8 V to 7.2 V		80		ns
Falling Time[3]		C_{DRV} = 2.2 nF, from 7.2 V to 0.8 V		35		ns
Sourcing Resistor				4		Ω
Sinking Resistor				2		Ω
Peak Source Current[4]				1		A
Sink Source Current[4]				1		A
DRV Output High Voltage	V_{DRV_H}		7.6	8	8.4	V
INTERNAL REGULATOR (VREG)						
VREG Voltage	V_{VREG}	I_{VREG} = 5 mA	4.7	5	5.3	V
Dropout Voltage		I_{VREG} = 5 mA		27		mV
Regulator Current Limit				200		mA
POWER DETECTION						
VPTH Rising Threshold	V_{PTH_R}			1.22	1.25	V
VPTH Falling Threshold	V_{PTH_F}		1.05	1.09		V
VPTH Source Current		VPTH voltage < 1.09 V		4.8		µA
		VPTH voltage > 1.22 V		1		µA
Power Detection Deglitch Time				10		µs
DET Output Low Voltage		I_{DET} = 20 mA		0.3	0.55	V
Maximum Sink Current on DET	I_{DET_MAX}			100		mA
ACTUATOR DRIVER (TRG AND GATE)						
Input High Voltage		TRG pin	1.2			V
Input Low Voltage		TRG pin			0.4	V
Deglitch Time		TRG pin		30		µs
GATE Maximum Source Current		GATE pin		85		mA
GATE Driver Output Voltage		GATE pin		5		V
THERMAL						
Thermal Shutdown Threshold[4]				150		°C
Thermal Shutdown Hysteresis[4]				15		°C

[1] This current is measured from the VIN pin.
[2] This UVLO threshold is only for the boost control block.
[3] Bench measurement result.
[4] Guaranteed by design, not production tested.

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT		VIN pin				
Undervoltage Lockout Threshold[1]						
VIN Rising				4.2	4.4	V
VIN Falling			3.5	3.65		V
FEEDBACK (FB2)						
FB2 Regulation Voltage	V_{FB2}	Adjustable output version	0.591	0.6	0.609	V
Fixed Output Accuracy		Fixed output version	−1.5		+1.5	%
FB2 Bias Current	I_{FB2}	Adjustable output version		0.01	0.1	µA
		Fixed output version		4.3	5	µA
SWITCH NODE						
High-Side On Resistance (LFCSP)[2]	$R_{DSON\_H\_LFCSP}$	I_{SW_SOURCE} = 0.5 A		700	1070	mΩ
Low-Side On Resistance (LFCSP)[2]	$R_{DSON\_L\_LFCSP}$	I_{SW_SINK} = 0.5 A		380	540	mΩ
High-Side On Resistance (LQFP)[2]	$R_{DSON\_H\_LQFP}$			750	1210	mΩ
Low-Side On Resistance (LQFP)[2]	$R_{DSON\_L\_LQFP}$			430	620	mΩ
SW Leakage Current	$I_{SW\_LK\_HS}$	SW = PGND2		0.1		µA
	$I_{SW\_LK\_LS}$	SW = V_{IN}		42		µA
Minimum On Time	t_{ON_MIN}			42		ns
Minimum Off Time	t_{OFF_MIN}			150		ns
BST						
Bootstrap Voltage	V_{BOOT}		4.7	5	5.3	V
CURRENT LIMIT						
Valley Current Limit			0.65	0.8	0.98	A
Low-Side Sink Current Limit				0.2		A
PWM SWITCHING FREQUENCY	f_{SW}		1.0	1.2	1.4	MHz
SOFT START TIME	t_{SS}	Fixed output version		400		µs
		Adjustable output version		1.6		ms
RESET ($\overline{RSTO}$)						
Reset Rising Threshold Voltage		Refer to V_{FB2}	85	89	94	%
Reset Threshold Hysteresis				1		%
Reset Rising Delay	$t_{RST\_DELAY\_R}$	Option 1, default	0.42	0.5	0.56	ms
		Option 2	0.85	1	1.12	ms
		Option 3	1.72	2	2.3	ms
		Option 4	4.2	5	5.6	ms
Reset Falling Delay	$t_{RST\_DELAY\_F}$			10		µs
$\overline{RSTO}$ Output Low Voltage		I_{RSTO} = 3 mA		40	100	mV
$\overline{RSTO}$ Leakage Current		V_{RSTO} = 5 V		0.01	0.3	µA

[1] This UVLO threshold is only for the buck control block.
[2] Pin to pin measurement.

PROGRAMMABLE GAIN AMPLIFIER AND ANALOG TRIP SPECIFICATIONS

V_{IN} = 12 V, V_{AVDD} = 5 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER INPUT		AVDD pin				
Input Voltage Range	V_{AVDD}		2.7		5.5	V
Quiescent Current	I_{Q_AVDD}			575		µA
Undervoltage Lockout Threshold						

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AVDD Rising				2.6	2.7	V
AVDD Falling			2.4	2.5		V
INPUT CHARACTERISTICS						
Input Voltage Range		V_{VCOM} = GND	−6.6		0	V
		V_{VCOM} = V_{AVDD}	−3.3		+3.3	V
Input Offset	V_{OS_PGA}	T_J = 25°C, trimmed at gain = 1			0.5	mV
Input Offset Temperature Drift		Gain < 4		5.5	17	µV/°C
		Gain ≥ 4		3.5	9.5	µV/°C
Input Capacitance[1]	C_{IN_PGA}			2		pF
Input Impedance	R_{IN_PGA}			1		MΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH_PGA}	I_{OH_PGA} = −250 µA	V_{AVDD} − 0.3 V	V_{AVDD} − 0.1 V		V
Output Voltage Low	V_{OL_PGA}	I_{OL_PGA} = 250 µA		25	40	mV
Short-Circuit Current	$I_{SC\_H\_PGA}$	Short to AVDD		17		mA
	$I_{SC\_L\_PGA}$	Short to GND		10		mA
Close-Loop Output Impedance[2]	Z_{OUT_PGA}	f = 100 Hz, gain = 1		18		Ω
DYNAMIC PERFORMANCE						
Slew Rate[2]	SR_{PGA}	R_{L_PGA} = 10 kΩ , C_{L_PGA} = 35 pF, gain = 1		1.7		V/µs
Gain Bandwidth Product[1]	GBP_{PGA}	R_{L_PGA} = 10 kΩ , C_{L_PGA} = 35 pF		1		MHz
Phase Margin[1]	Φ_{M_PGA}	R_{L_PGA} = 10 kΩ , C_{L_PGA} = 35 pF		60		Degrees
NOISE PERFORMANCE						
Input Voltage Noise Density[2]	e_{ni_PGA}	f = 1 kHz, gain = 1		180		nV/√Hz
Input Voltage Noise[2]	e_{n_PGA} p-p	f = 0.1 Hz to 10 Hz, gain = 1		34		µV p-p
GAIN PROGRAM (GAIN0, GAIN1)						
Input High Voltage		For GAIN0 pin	1.2			V
Input Low Voltage		For GAIN0 pin			0.4	V
Voltage on GAIN1			0.792	0.8	0.808	V
Gain Error		T_J = 25 °C			0.5	%
Gain Drift		Gain < 4		7	12	ppm/°C
		Gain ≥ 4		4	8.5	ppm/°C
ANALOG TRIP						
Analog Trip Disable Voltage Threshold	V_{TRP_DIS}					
Rising				4.75		V
Falling				4.65		V
VTRP Current	I_{TRP}		9.5	10	10.4	µA
VTRPL Current[3]	I_{TRPL}		9.5	10	10.4	µA
Analog Trip Deglitch Time	t_{TRP}	Option 1 (default)	178	200	223	µs
		Option 2	310	350	387	µs
		Option 3	440	500	552	µs
		Option 4	660	750	826	µs
		Option 5	0.88	1	1.1	ms
		Option 6	1.75	2	2.2	ms
		Option 7	2.6	3	3.3	ms
		Option 8	3.5	4	4.4	ms

[1] Guaranteed by design, not production tested.
[2] Bench measurement result.
[3] Only available in the 48-lead LQFP package.

OPERATION AMPLIFIER SPECIFICATIONS

V_{IN} = 12 V, V_{AVDD} = 5 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Voltage Range			0		V_{AVDD}	V
Input Offset	V_{OS_EA}	T_J = 25°C		20	850	µV
Input Offset Temperature Drift				5.5	19	µV/°C
Input Bias Current[1]				1	1000	pA
Input Capacitance[1]	C_{IN_EA}			2		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH_EA}	I_{OH_EA} = −250 µA	V_{AVDD} − 0.3 V	V_{AVDD} − 0.1 V		V
Output Voltage Low	V_{OL_EA}	I_{OL_EA} = +250 µA		15	35	mV
Short-Circuit Current	$I_{SC\_H\_EA}$	Short to AVDD		30		mA
	$I_{SC\_L\_EA}$	Short to GND		15		mA
DYNAMIC PERFORMANCE[2]						
Slew Rate	SR_{EA}	R_{L_EA} = 10 kΩ, C_{L_EA} = 35 pF		0.5		V/µs
Gain Bandwidth Product	GBP_{EA}	R_{L_EA} = 10 kΩ, C_{L_EA} = 35 pF		1.6		MHz
Phase Margin	Φ_{M_EA}	R_{L_EA} = 10 kΩ, C_{L_EA} = 35 pF		56		Degrees
NOISE PERFORMANCE[2]						
Input Voltage Noise Density	e_{ni_EA}	f = 1 kHz		240		nV/√Hz
Input Voltage Noise	e_{n_EA} p-p	f = 0.1 Hz to 10 Hz		46		µV p-p

[1] Guaranteed by design, not production tested.
[2] Bench measurement result.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VIN, SW, DET, VPTH	−0.3 V to +40 V
AVDD	−0.3 V to +6 V
BST	The SW pin voltage (V_{SW}) + 6 V
DRV	−0.3 V to +12 V
EIN1, EIN2, EIN3, EIN4	−8 V to +8 V
EIN5_P, EIN5_N	−8 V to +8 V
EOUT1, EOUT2, EOUT3, EOUT4, EOUT5, VCOM, RCOM	−0.3 V to V_{AVDD}
VREG, FB1, FB2, VTRP, VTRPL, RSTO, TRG, GATE, GAIN0, GAIN1	−0.3 V to +6 V
PGNDx to GND	−0.3 V to +0.3 V
Operating Temperature Range (Junction)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
Electrostatic Discharge (ESD)	
Human Body Mode	4000 V (for EIN1, EIN2, EIN3, EIN4, EIN5_P, and EIN5_N pins), 2000 V (for the rest of pins)
Charged Device Mode	500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-32-7[1]	32.7	1.4	°C/W
ST-48[1]	66.68	3.41	°C/W

[1] θ_{JA} is measured using natural convection on a JEDEC 4-layer board with the exposed pad soldered to the PCB and with thermal vias.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

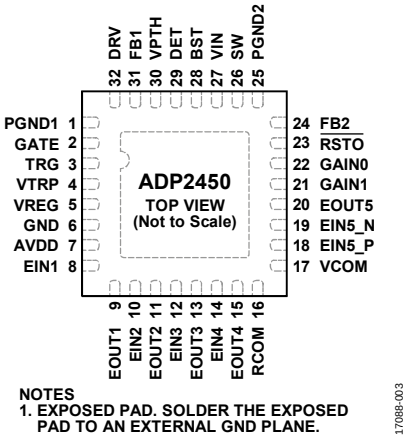


Figure 3. 32-Lead LFCSP Package Pin Configuration (Top View)

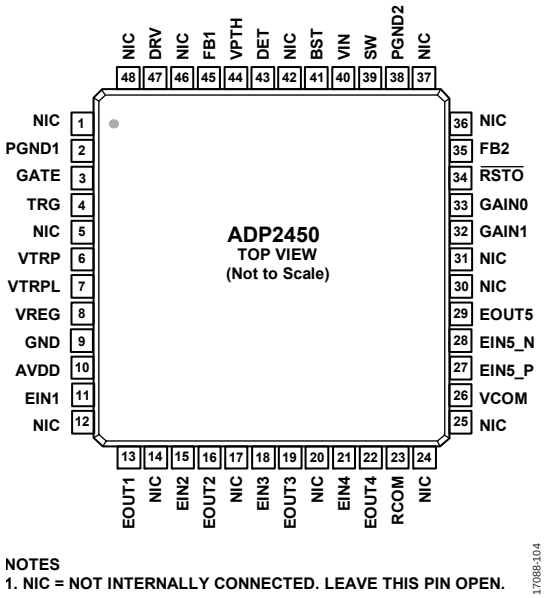


Figure 4. 48-Lead LQFP Package Pin Configuration (Top View)

Table 7. Pin Function Descriptions

Pin No.			
LFCSP 32-Lead	**LQFP 48-Lead**	**Mnemonic**	**Description**
1	2	PGND1	Boost Shunt Driver and Actuator Driver Ground.
2	3	GATE	Actuator Driver. This pin drives the silicon controlled rectifier (SCR), field-effect transistor (FET), or transistor.
3	4	TRG	Actuator Trigger Signal. This signal comes from the microcontroller unit (MCU).
4	6	VTRP	Analog Trip High Threshold Setting. Connect a resistor between this pin and ground to set the analog trip high threshold.
	7	VTRPL	Analog Trip Low Threshold Setting. Connect a resistor between this pin and ground to set the analog trip low threshold.
5	8	VREG	Internal 5 V Regulator Output. The IC control circuits are powered from this voltage. Place a 1 µF ceramic capacitor between VREG and GND.
6	9	GND	Analog Ground. Connect this pin to the ground plane.
7	10	AVDD	Power Supply for the Amplifier Block.
8	11	EIN1	Input of the Programmable Gain Amplifier 1.
9	13	EOUT1	Output of the Programmable Gain Amplifier 1.
10	15	EIN2	Input of the Programmable Gain Amplifier 2.
11	16	EOUT2	Output of the Programmable Gain Amplifier 2.
12	18	EIN3	Input of the Programmable Gain Amplifier 3.
13	19	EOUT3	Output of the Programmable Gain Amplifier 3.
14	21	EIN4	Input of the Programmable Gain Amplifier 4.
15	22	EOUT4	Output of the Programmable Gain Amplifier 4.
16	23	RCOM	External Resistance Compensation for Programmable Gain Amplifier 1 to Amplifier 4.
17	26	VCOM	Setting for the Output Common Voltage of the Programmable Gain Amplifiers. This pin is connected to an external reference voltage.
18	27	EIN5_P	Positive Input of Amplifier 5.
19	28	EIN5_N	Negative Input of Amplifier 5.
20	29	EOUT5	Output of the Amplifier 5.
21	32	GAIN1	Gain Setting for Programmable Gain Amplifier 1 to Amplifier 4. This pin is combined with GAIN0 to set the gain of the amplifier.

Pin No.			
LFCSP 32-Lead	LQFP 48-Lead	Mnemonic	Description
22	33	GAIN0	Gain Setting for Programmable Gain Amplifier 1 to Amplifier 4. This pin is combined with GAIN1 to set the gain of the amplifier.
23	34	$\overline{\text{RSTO}}$	Reset Output (Open Drain). Connect this pin to a resistor to any pull-up voltage < 5.5 V.
24	35	FB2	Feedback Voltage Sense Input for Buck Regulator. Connect this pin to a resistor divider from buck output voltage, $V_{OUT2,}$ for adjustable version. For the fixed output version, connect this pin to V_{OUT2} directly.
25	38	PGND2	Power Ground for Buck Regulator.
26	39	SW	Switch Node for Buck Regulator.
27	40	VIN	Power Input for Buck Regulator and Internal VREG. This voltage is monitored by the power detection circuit. Connect a bypass capacitor between this pin and PGND2.
28	41	BST	Supply Rail for the Gate Drive of Buck. Place a 0.1 µF capacitor between SW and BST.
29	43	DET	Power Detection Output.
30	44	VPTH	Power Detection Voltage Threshold Setting. Connect a resistor between this pin and ground to set the power rating detection voltage threshold.
31	45	FB1	Feedback Voltage Sense Input for boost shunt. Connect this pin to a resistor divider from V_{OUT1}.
32	47	DRV	Boost Shunt Driver.
	1, 5, 12, 14, 17, 20, 24, 25, 30, 31, 36, 37, 42, 46, 48	NIC	Not Internally Connected. Leave the pin open.
33		EP	Exposed Pad. Solder the exposed pad to an external GND plane.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12 V, V_{AVDD} = 5 V, V_{VCOM} = V_{RCOM} (the RCOM pin voltage) = 0 V, unless otherwise noted.

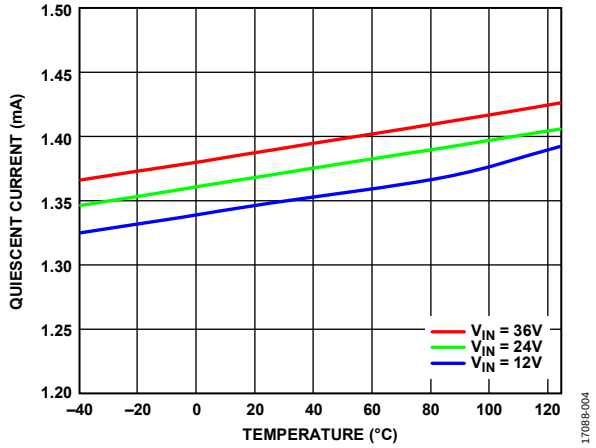


Figure 5. Quiescent Current vs. Temperature

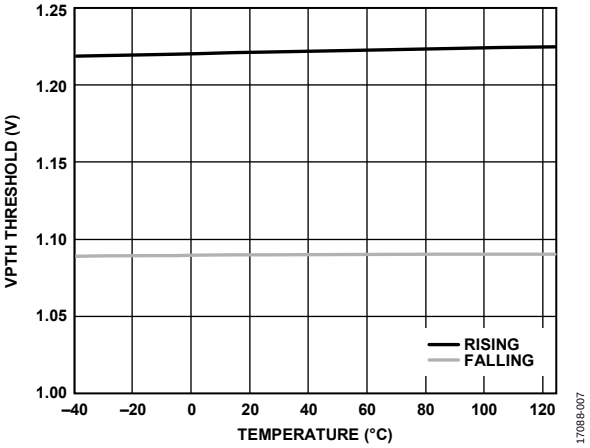


Figure 8. VPTH Threshold vs. Temperature

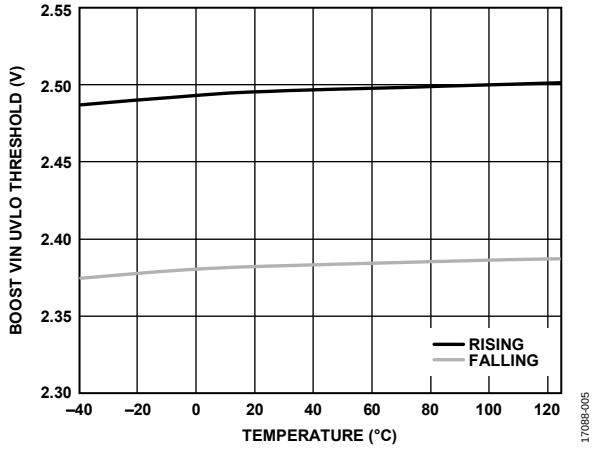


Figure 6. VIN UVLO Threshold for Boost Controller vs. Temperature

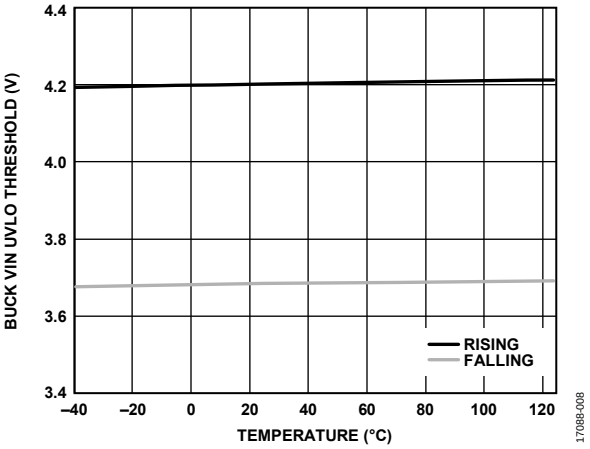


Figure 9. VIN UVLO Threshold for Buck Regulator vs. Temperature

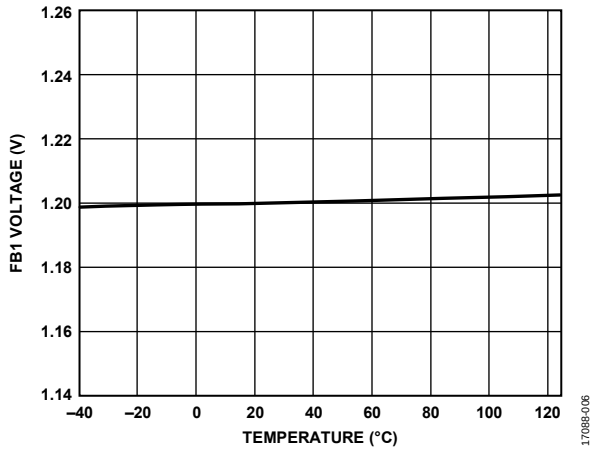


Figure 7. FB1 Voltage vs. Temperature

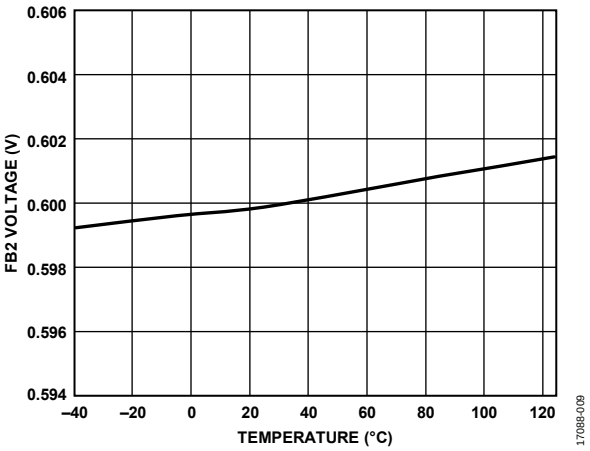


Figure 10. FB2 Voltage vs. Temperature

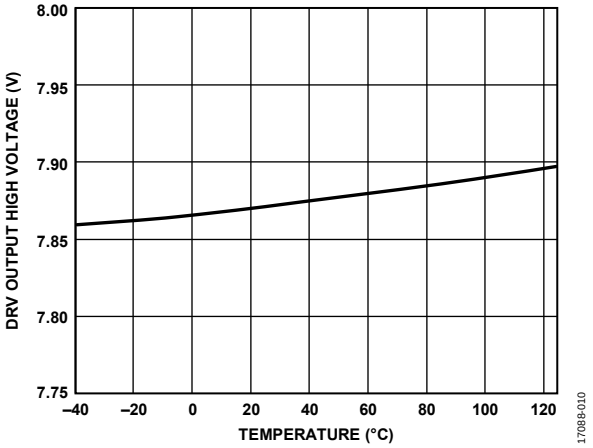


Figure 11. DRV Output High Voltage vs. Temperature

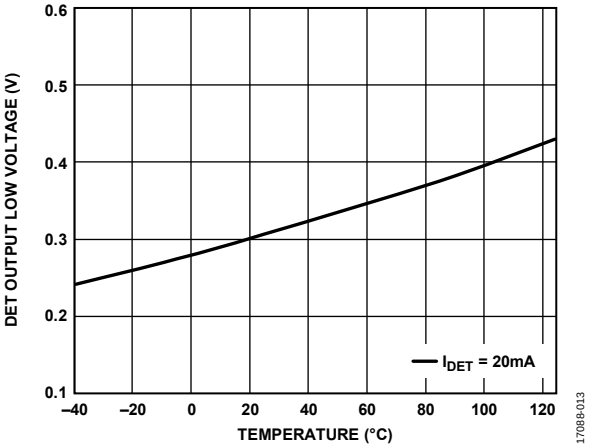


Figure 14. DET Output Low Voltage vs. Temperature

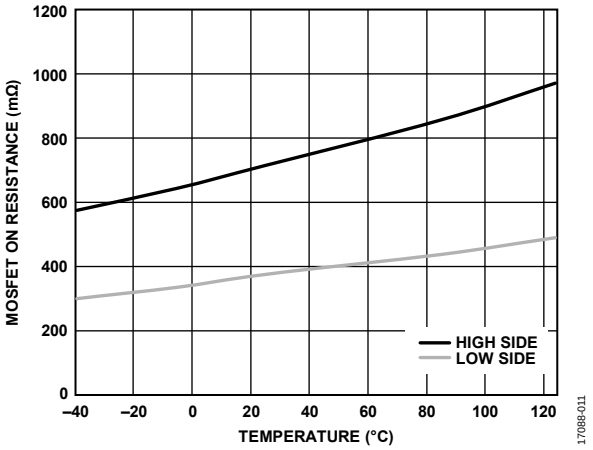


Figure 12. MOSFET On Resistance vs. Temperature

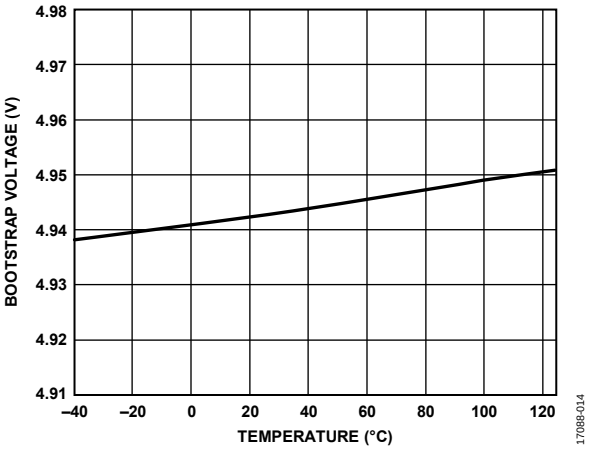


Figure 15. Bootstrap Voltage vs. Temperature

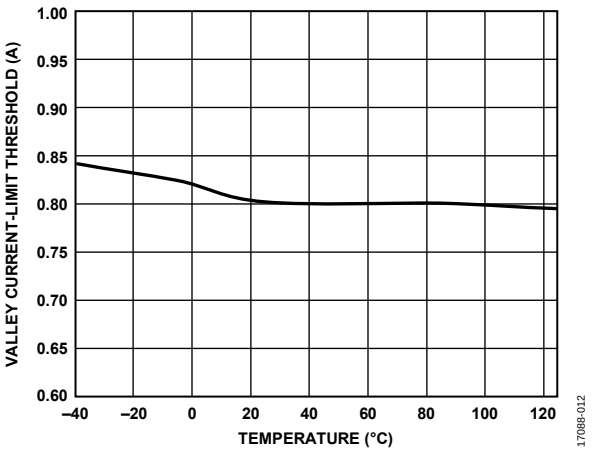


Figure 13. Valley Current-Limit Threshold vs. Temperature

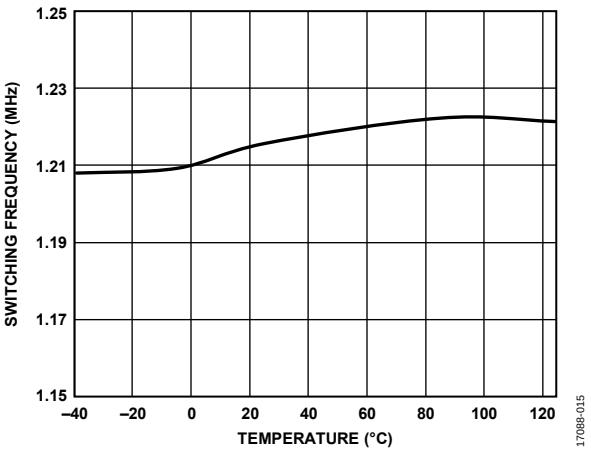


Figure 16. Switching Frequency vs. Temperature

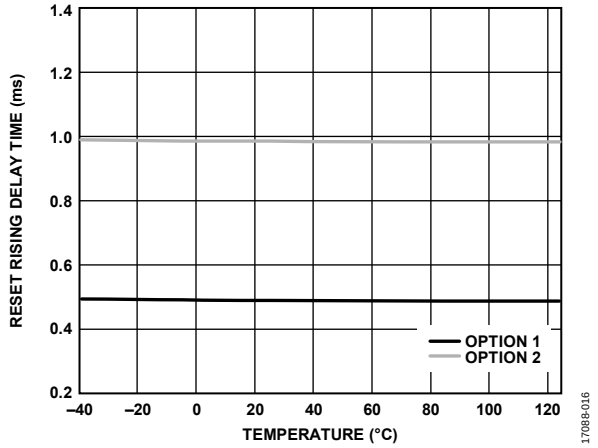


Figure 17. Reset Rising Delay Time (Option1, Option 2) vs. Temperature

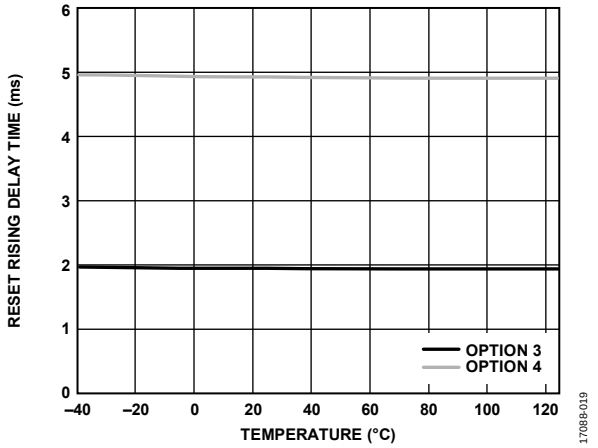


Figure 20. Reset Rising Delay Time (Option 3, Option 4) vs. Temperature

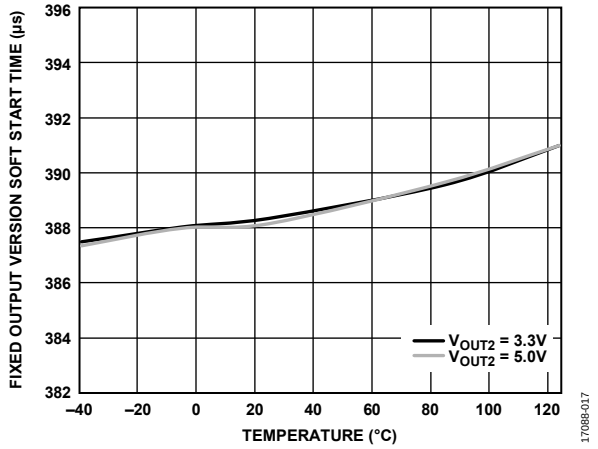


Figure 18. Fixed Output Version Soft Start Time vs. Temperature

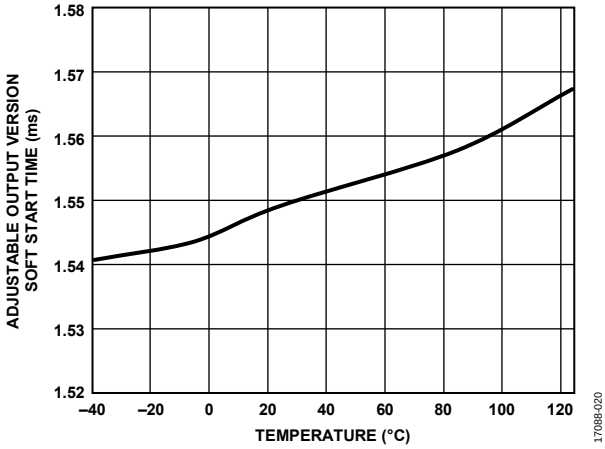


Figure 21. Adjustable Output Version Soft Start Time vs. Temperature

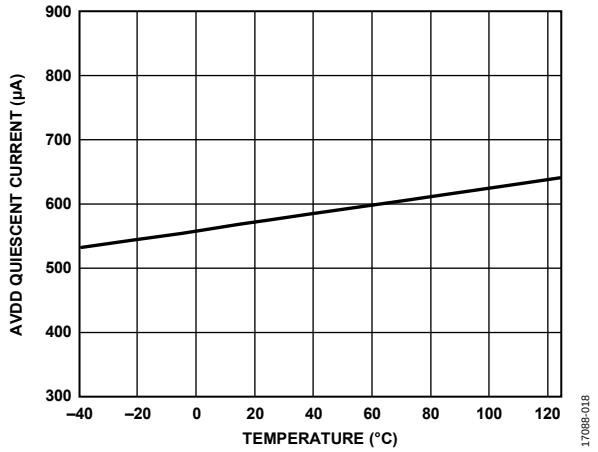


Figure 19. AVDD Quiescent Current vs. Temperature

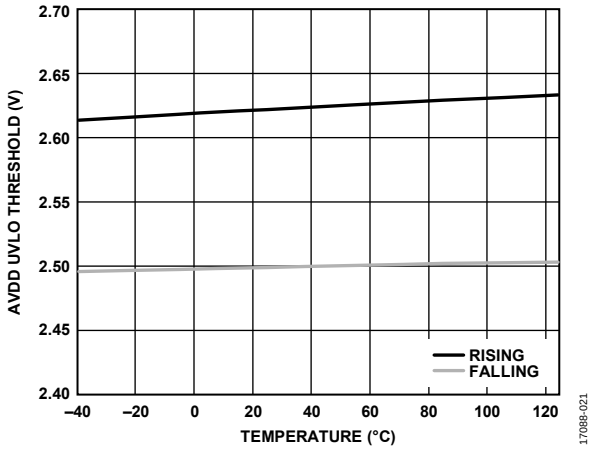


Figure 22. AVDD UVLO Threshold vs. Temperature

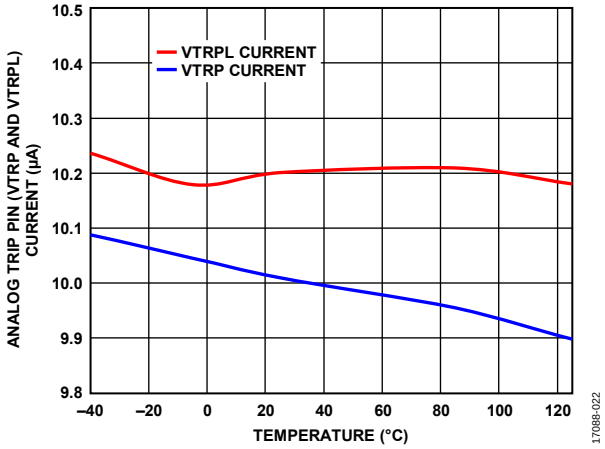


Figure 23. Analog Trip Pin (VTRP and VTRPL) Current vs. Temperature

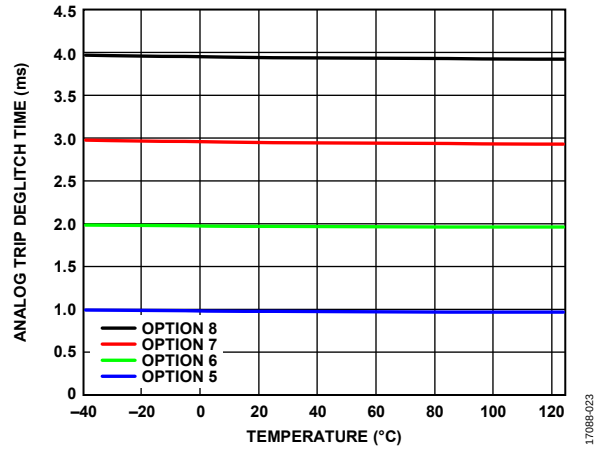


Figure 24. Analog Trip Deglitch Time vs. Temperature (Option 5 to Option 8)

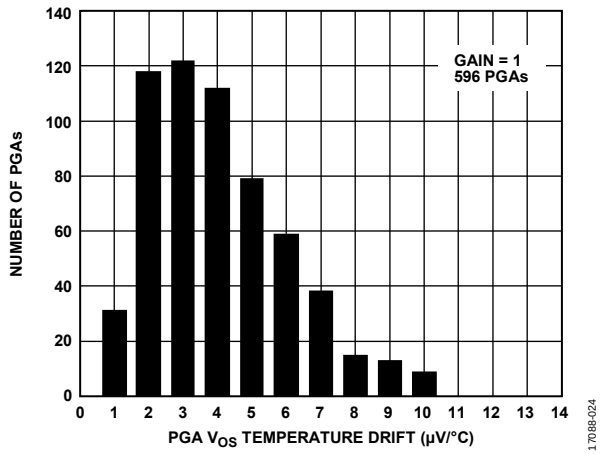


Figure 25. PGA Input Offset Voltage Drift Distribution, Gain = 1

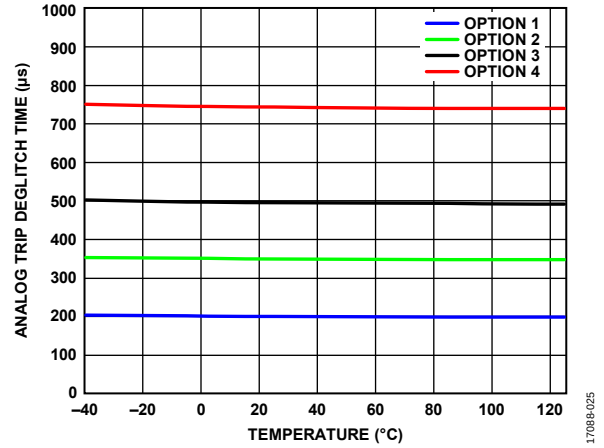


Figure 26. Analog Trip Deglitch Time vs. Temperature (Option 1 to Option 4)

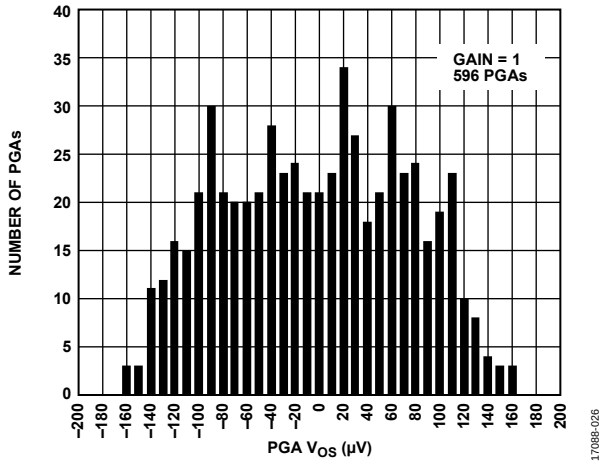


Figure 27. PGA Input Offset Voltage Distribution

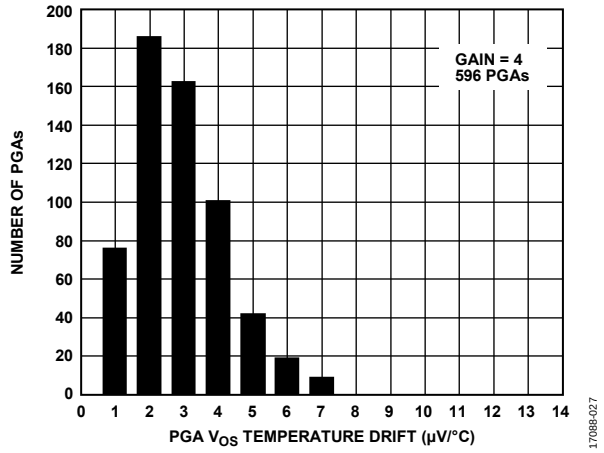


Figure 28. PGA Input Offset Voltage Drift Distribution, Gain = 4

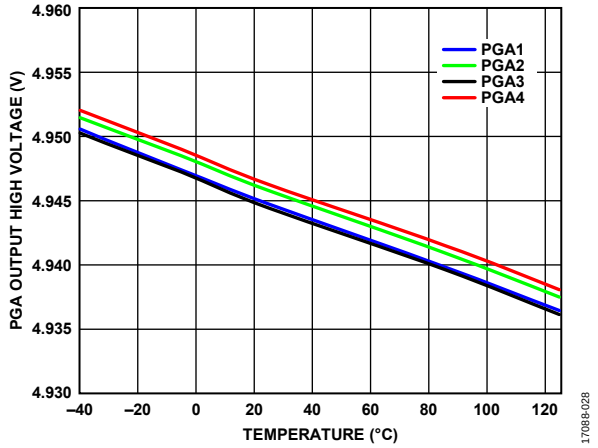


Figure 29. PGA Output High Voltage vs. Temperature

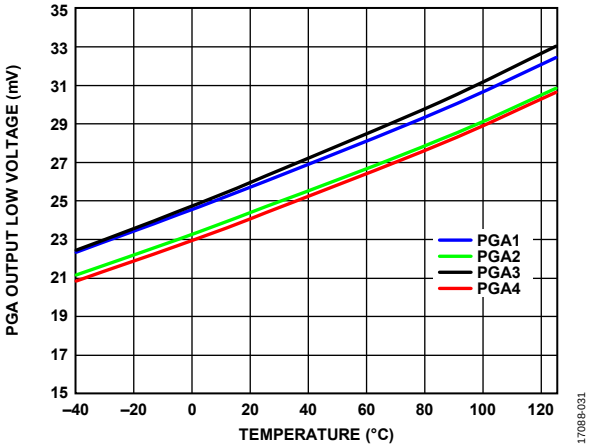


Figure 32. PGA Output Low Voltage vs. Temperature

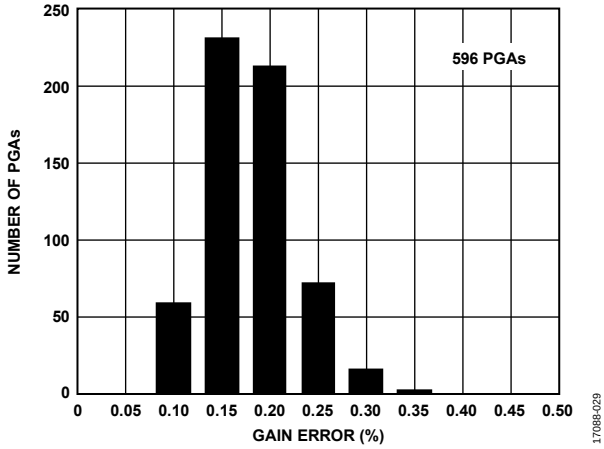


Figure 30. PGA Gain Error Distribution

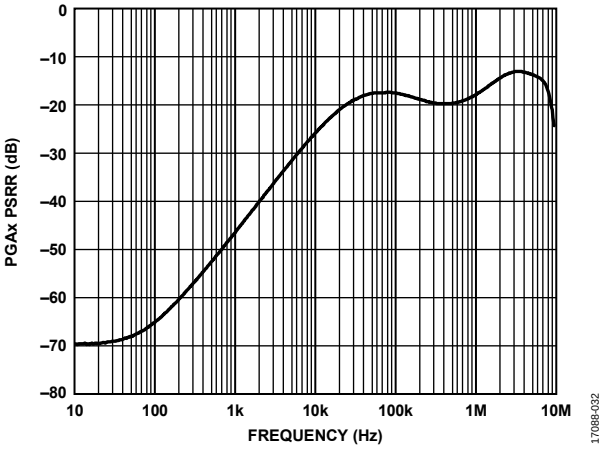


Figure 33. PGAx Power Supply Rejection Ratio (PSRR) vs. Frequency

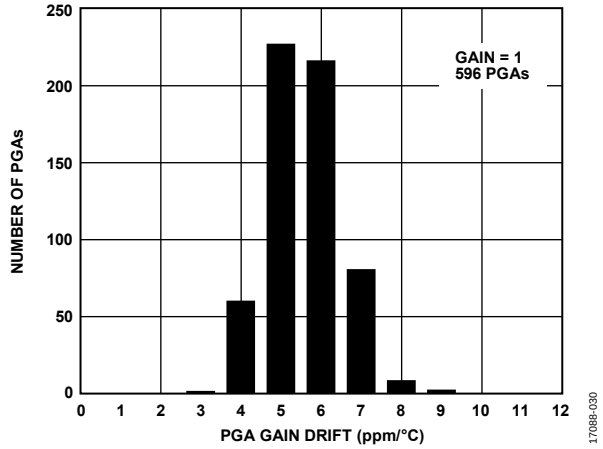


Figure 31. PGA Gain Drift Distribution, Gain = 1

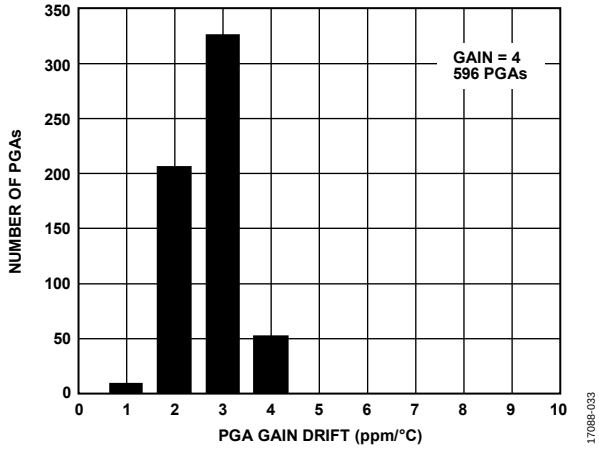


Figure 34. PGA Gain Drift Distribution, Gain = 4

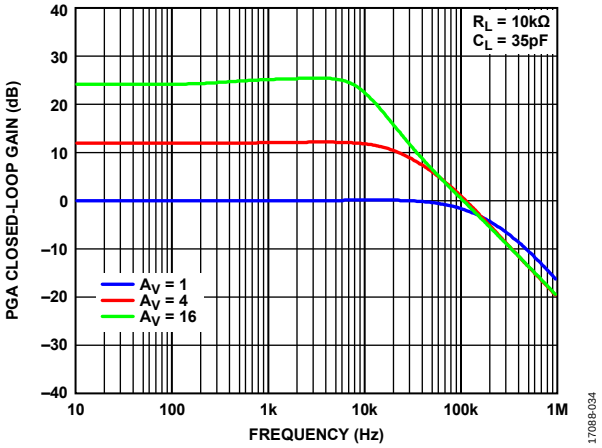


Figure 35. PGA Closed-Loop Gain vs. Frequency

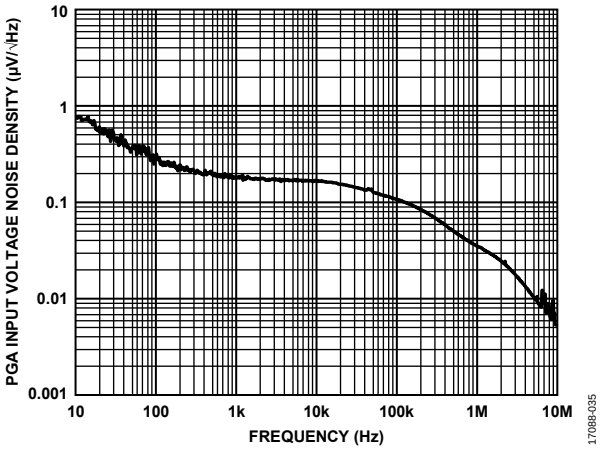


Figure 36. PGA Input Voltage Noise Density vs. Frequency

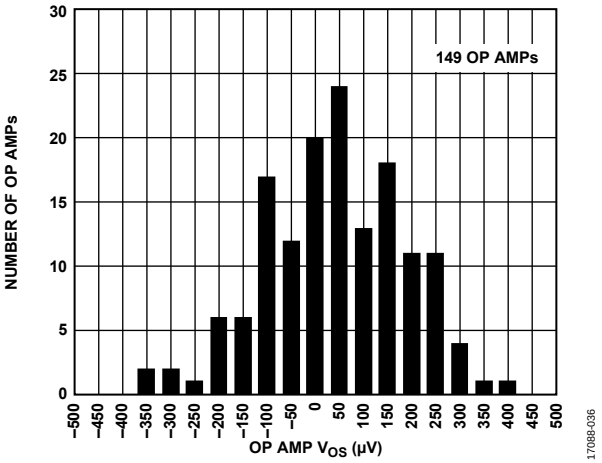


Figure 37. Operational Amplifier (Op Amp) Input Offset Voltage Distribution

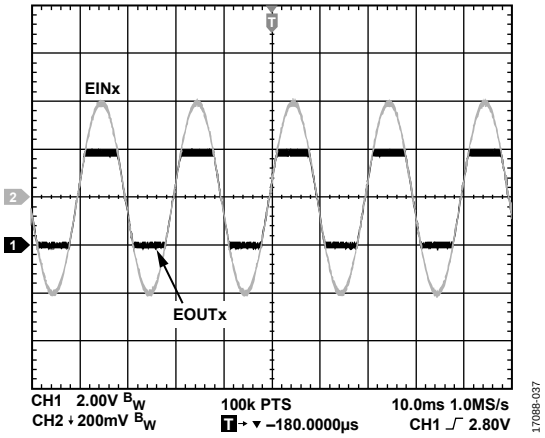


Figure 38. PGA No Phase Reversal, $V_{VCOM} = V_{AVDD} = 4$ V, $A_V = -10$

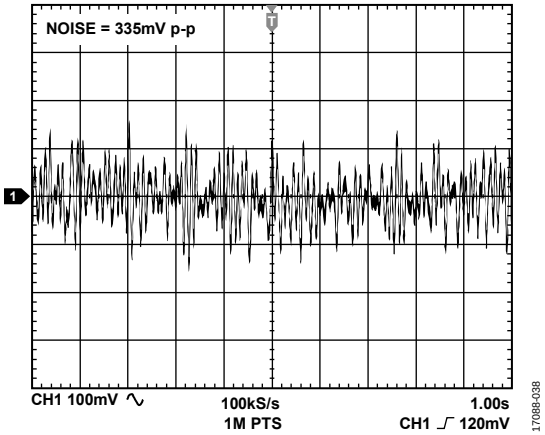


Figure 39. PGA 0.1 Hz to 10 Hz Noise, Amplification = 10,000×

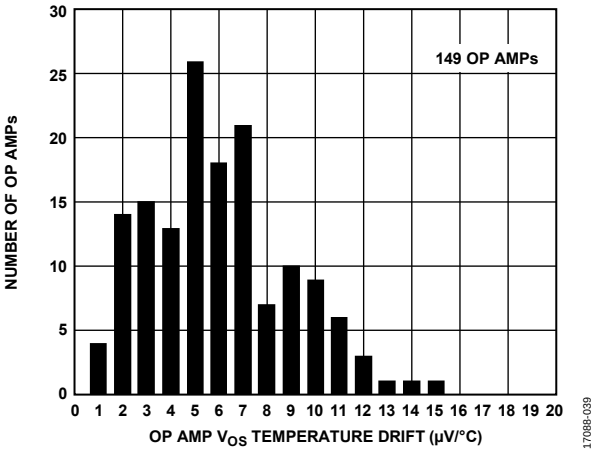


Figure 40. Op Amp Input Offset Voltage Temperature Drift Distribution

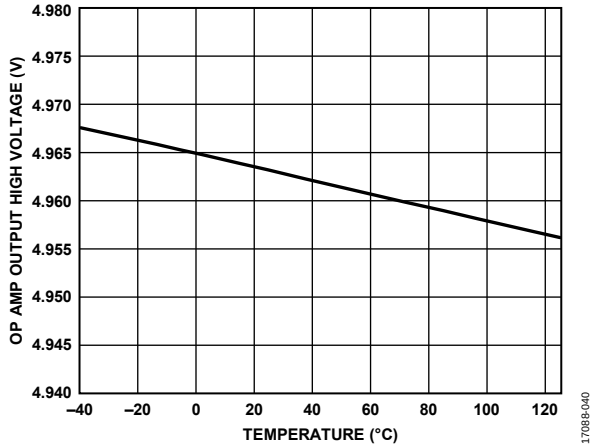


Figure 41. Op Amp Output High Voltage vs. Temperature

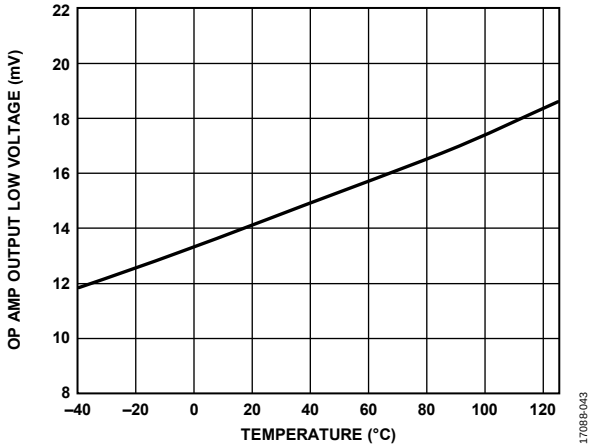


Figure 44. Op Amp Output Low Voltage vs. Temperature

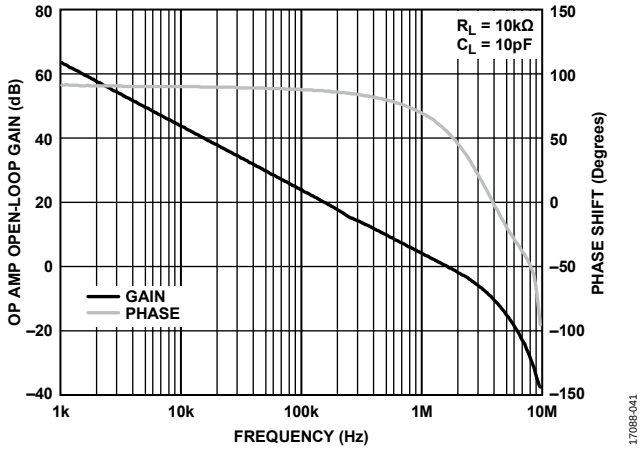


Figure 42. Op Amp Open-Loop Gain and Phase Shift vs. Frequency

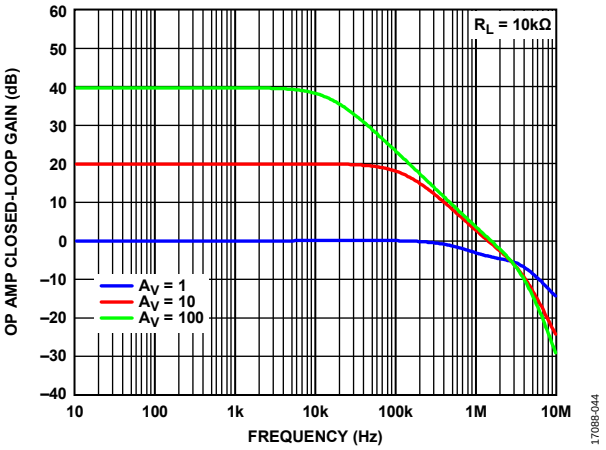


Figure 45. Op Amp Close-Loop Gain vs. Frequency

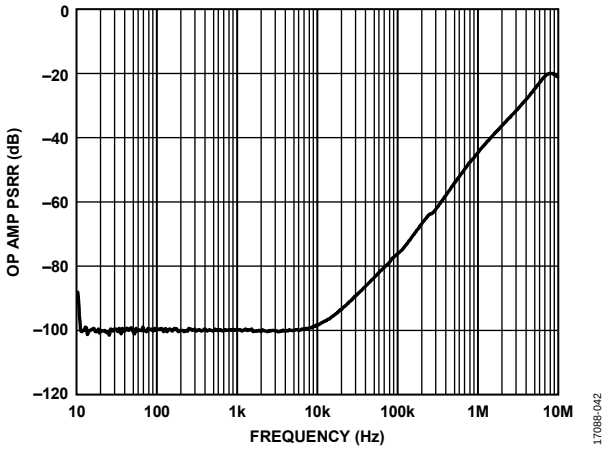


Figure 43. Op Amp PSRR vs. Frequency

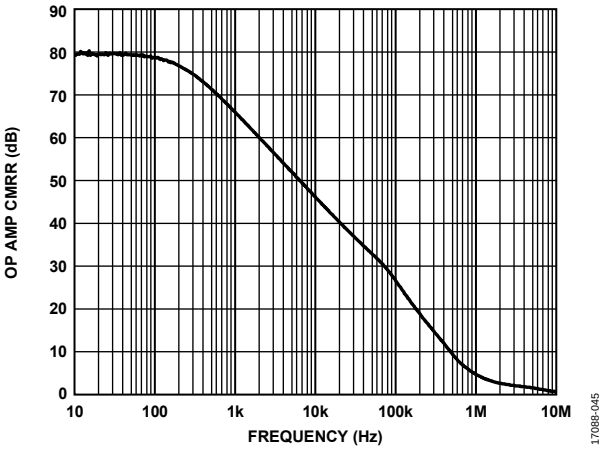


Figure 46. Op Amp Common-Mode Rejection Ratio (CMRR) vs. Frequency

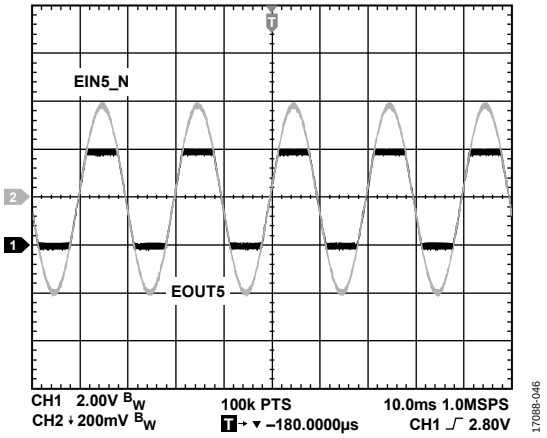


Figure 47. Op Amp No Phase Reversal, V_{AVDD} = 4 V, A_V = −10

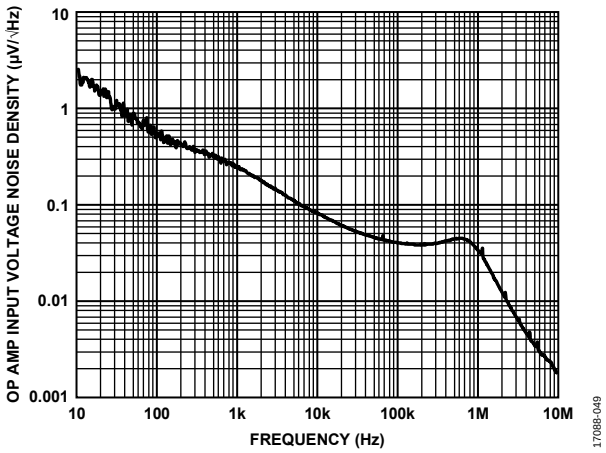


Figure 50. Op Amp Input Voltage Noise Density vs. Frequency

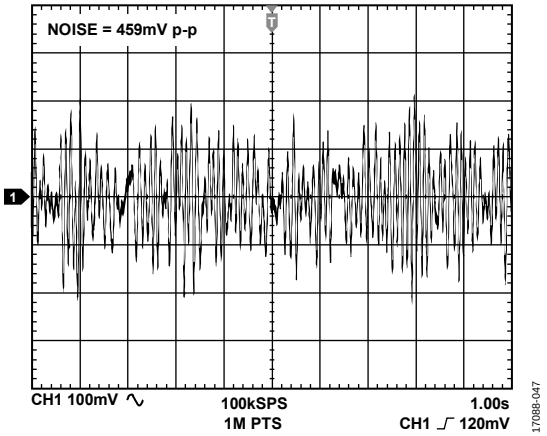


Figure 48. Op Amp 0.1 Hz to 10 Hz Noise, Amplification = 10,000×

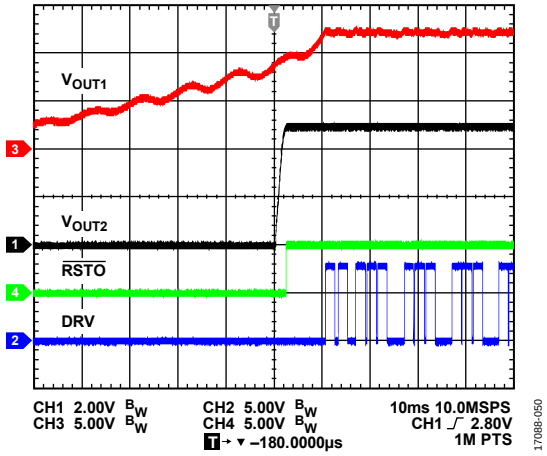


Figure 51. Start Up with AC Current Source, VCOM = GND

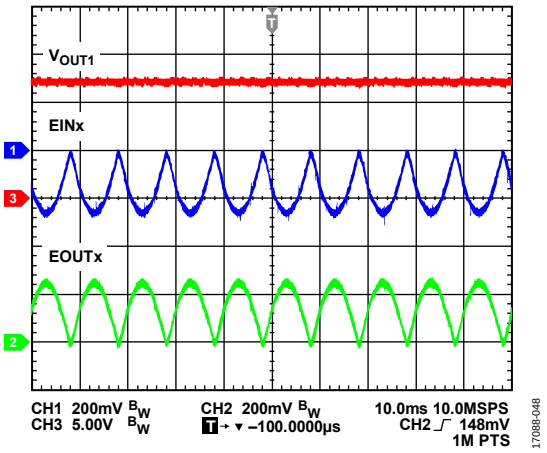


Figure 49. PGA Working Waveform, Gain = 1

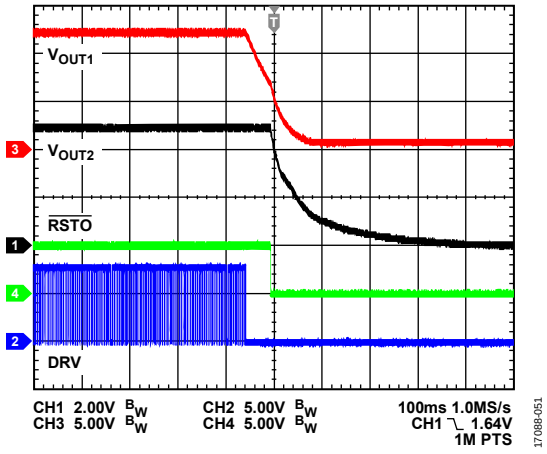


Figure 52. System Shutdown Waveform

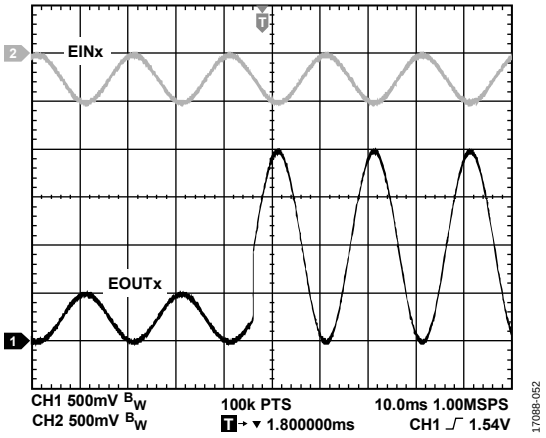


Figure 53. PGA Gain Switching from Gain = 1 to Gain = 4

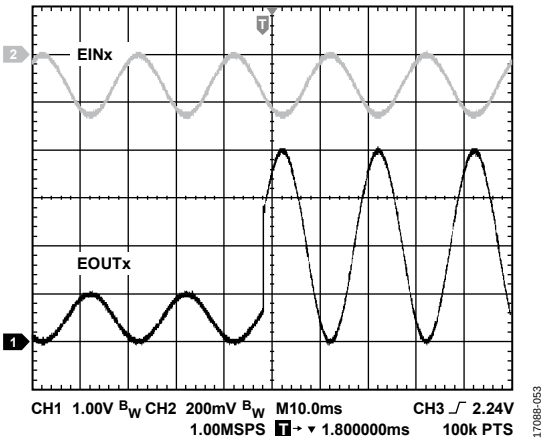


Figure 54. PGA Gain Switching from Gain = 4 to Gain = 16

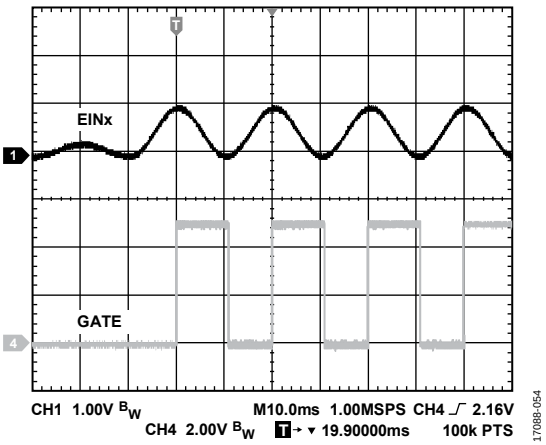


Figure 55. Analog Trip Threshold Triggered, VCOM = RCOM = 0 V

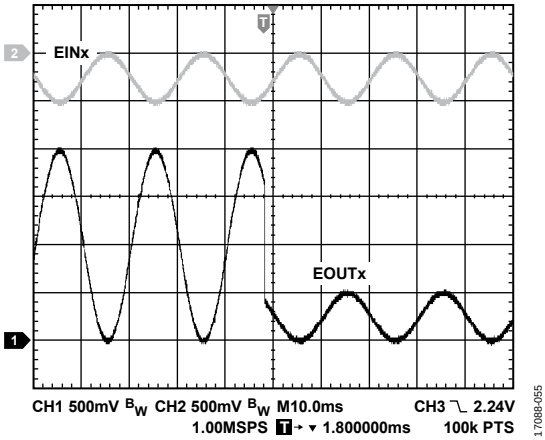


Figure 56. PGA Gain Switching from Gain = 4 to Gain = 1

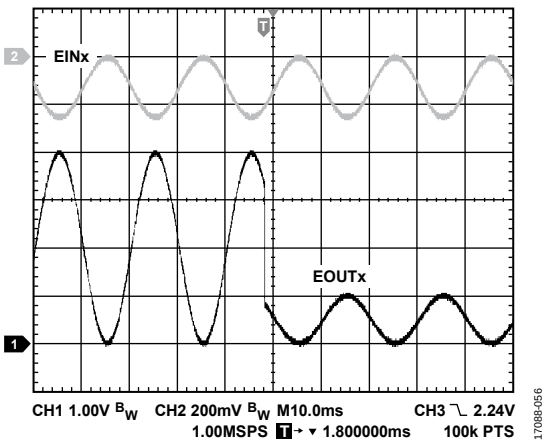


Figure 57. PGA Gain Switching from Gain = 16 to Gain = 4

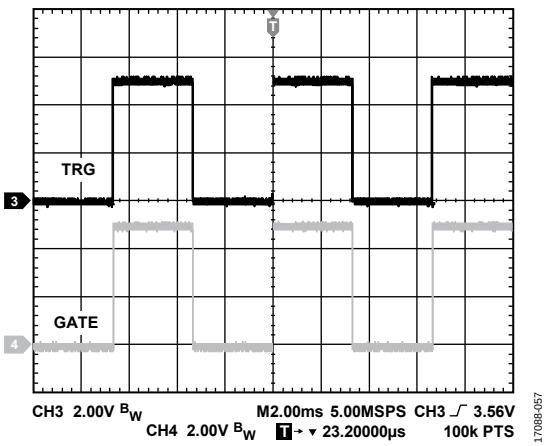


Figure 58. TRG Trigger Analog Trip Function

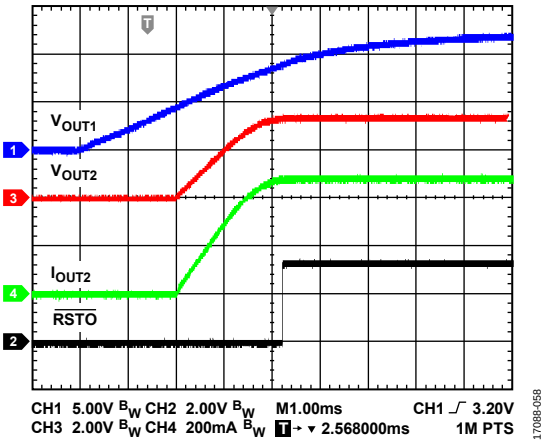


Figure 59. Buck Regulator Soft Start with Full Load
(V_{OUT2} = 3.3 V, Adjustable Version)

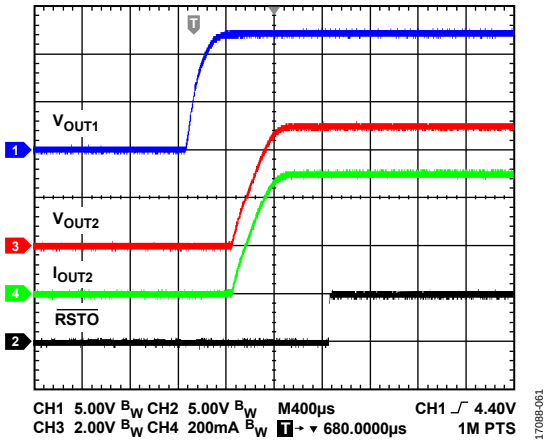


Figure 62. Buck Regulator Soft Start with Full Load
(V_{OUT2} = 5 V, Fixed Version)

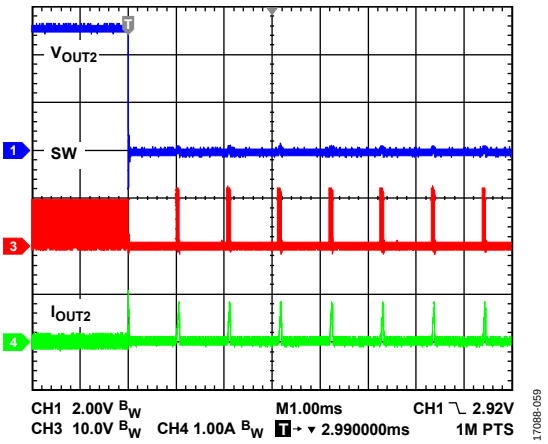


Figure 60. Buck Regulator OCP Triggered

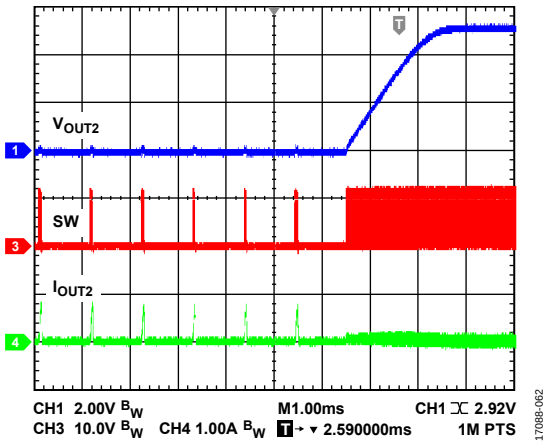


Figure 63. Buck Regulator OCP Recovery

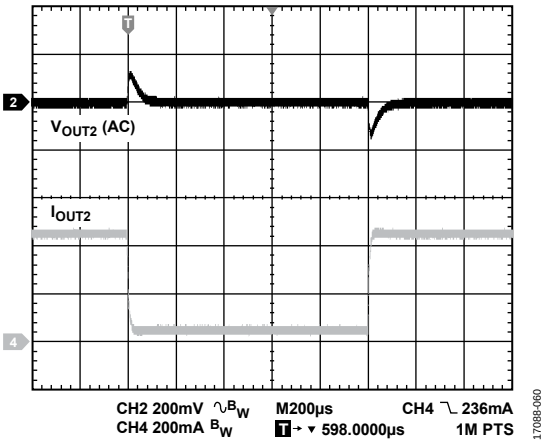


Figure 61. Buck Regulator Load Transient (50 mA to 450 mA)

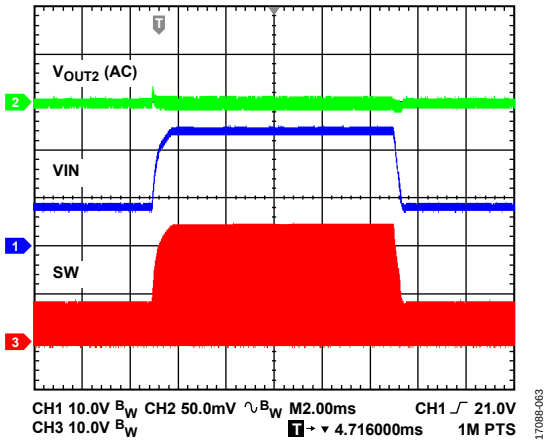


Figure 64. Buck Regulator Line Transient, V_{IN} from 8 V to 24 V, Full Load

THEORY OF OPERATION

The ADP2450 is a power management IC for circuit breaker and CT powered supply applications. The ADP2450 integrates one boost shunt controller with power detection, one high efficiency buck regulator, four programmable gain amplifiers, one low offset operation amplifier, a fast analog trip circuit, and an actuator driver in a 32-lead LFCSP or 48-lead LQFP package. With the high integration rate, the ADP2450 provides a compact, robust power supply and signal conditioning solution for size limited, high reliability systems.

BOOST SHUNT CONTROLLER

The ADP2450 integrates a boost shunt controller with a field-effect transistor (FET) driver. The boost shunt controller uses a hysteresis control scheme to regulate the output voltage. When the feedback voltage on the FB1 pin is lower than the reference voltage (typically 1.2 V), the FET driver turns off the external FET, and then the current from CT charges the output capacitor storing energy in the capacitor. When the output voltage rises and the feedback voltage on the FB1 pin is higher than the rising threshold (typically 1.219 V), the FET driver turns on the external FET and bypasses the CT current to ground through the external FET.

POWER DETECTION

The ADP2450 integrates an input power detection function. During startup, when the voltage on the VPTH pin is lower than the VPTH rising threshold (typically 1.22 V), the power detection FET is turned on and the DET pin is pulled down to ground. Both the 1 µA and 3.8 µA internal current sources are added between VPTH and ground. When the voltage on the VPTH pin rises above the VPTH rising threshold (typical 1.22 V), the power detection FET is turned off and the DET pin is open. The 3.8 µA current source is removed and only the 1 µA current source is added.

When the voltage on the VPTH pin falls below the VPTH falling threshold (typically 1.09 V), the power detection FET is turned on again, which pulls the DET pin to ground, and the 3.8 µA current source is added between VPTH and ground again.

The voltage threshold and hysteresis for power detection is programmable with external resistors on the VPTH pin, as shown in Figure 65.

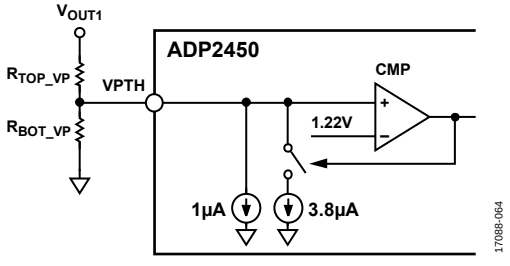


Figure 65. Programmable Voltage of Power Detection

Use the following equation to calculate R_{TOP_VP} and R_{BOT_VP}:

$$R_{TOP\_VP} = \frac{1.09\ \text{V} \times V_{OUT1\_RISING} - 1.22\ \text{V} \times V_{OUT1\_FALLING}}{1.09\ \text{V} \times 4.8\ \mu\text{A} - 1.22\ \text{V} \times 1\ \mu\text{A}}$$

$$R_{BOT\_VP} = \frac{1.22\ \text{V} \times R_{TOP\_VP}}{V_{OUT1\_RISING} - R_{TOP\_VP} \times 4.8\ \mu\text{A} - 1.22\ \text{V}}$$

where:

R_{TOP_VP} is the top side resistor connected between the V_{OUT1} and VPTH pin.

R_{BOT_VP} is the bottom side resistor connected between the VPTH pin and ground.

V_{OUT1_RISING} is the V_{OUT1} rising threshold.

$V_{OUT1\_FALLING}$ is the V_{OUT1} falling threshold.

A dummy resistor load (R_{POWER}) connected between V_{OUT1} and the DET pin ensures that the whole system is not enabled until there is enough power provided to the system by the current transformer, as shown in Figure 66.

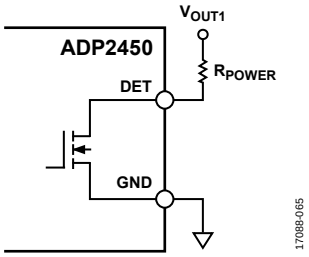


Figure 66. Dummy Load Connection

Calculate the dummy load resistor value using the following equation:

$$R_{POWER} = \frac{V_{OUT1\_RISING}}{I_{DUMMY}}$$

where I_{DUMMY} is the minimum required current value before enabling the system.

Ensure that the selected dummy load resistor can handle the power before the DET pin is open. The power consumption on the dummy load resistor (P_{DUMMY}) is calculated using the following equation:

$$P_{DUMMY} = I_{DUMMY}^{2} \times R_{POWER}$$

INTERNAL REGULATOR

The internal 5 V regulator (VREG) provides a stable voltage supply for the internal control circuits. It is recommended to place a 1 µF ceramic capacitor between VREG and GND. The internal regulator also includes a current-limit circuit for over-current protection.

The internal 8 V regulator provides the voltage supply for the boost shunt driver.

The VIN pin provides power supply for both the 5 V and 8 V internal regulators.

BUCK REGULATOR

The buck regulator in the ADP2450 uses a current mode control scheme for stability and transient response.

The buck regulator operates in a 1.2 MHz fixed switching frequency. The regulator integrates the soft start and compensation circuit to reduce the external components and provide an easy to use solution. The soft-start time is 400 µs for the fixed output version and is 1.6 ms for the adjustable output version.

The ADP2450 uses the emulated current ramp voltage for cycle by cycle current-limit protection to prevent current runaway. When the emulated current ramp voltage reaches the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this cycling process. If the overcurrent does not occur in the next cycle, the overcurrent counter decreases. If the overcurrent counter reaches 10 or the voltage on the FB2 pin drops below 0.2 V after soft start, the buck regulator enters into hiccup mode. During hiccup mode, both the high-side MOSFET and low-side MOSFET are turned off. The buck regulator remains in hiccup mode for 1024 clock cycles and then attempts to restart with a soft start. If the current-limit fault is cleared, the buck regulator resumes normal operation. Otherwise, the buck regulator reenters hiccup mode.

The low-side MOSFET in the buck regulator also sinks current from the load. If the low-side sink current exceeds the sink current-limit threshold, both the low-side and high-side MOSFETs are turned off until the next cycle starts.

The buck regulator only works when the voltage on the VPTH pin is higher than the VPTH rising threshold.

BOOTSTRAP CIRCUIT

The ADP2450 includes a regulator to provide the gate driver voltage for the high-side N-MOSFET of the buck regulator. It uses differential sensing method to generate a 5 V bootstrap voltage between the BST and the SW pins.

It is recommended to place a 0.1 µF, X7R or X5R ceramic capacitor between the BST and the SW pins.

POWER MONITOR AND RESET

The output voltage of the buck regulator is monitored through the FB2 pin. When the voltage on FB2 pin is below the reset threshold, the $\overline{\text{RSTO}}$ pin is pulled down. When the voltage on FB2 pin is above the reset threshold, the $\overline{\text{RSTO}}$ pin is released and can be pulled up by an external voltage source. A delay time is designed for the $\overline{\text{RSTO}}$ pin to ensure that no glitch occurs on the $\overline{\text{RSTO}}$ pin. There are four following options for the rising delay time: 0.5 ms, 1 ms, 2 ms, and 5 ms. The falling delay time is fixed at 10 µs.

PROGRAMMABLE GAIN AMPLIFIER

The ADP2450 integrates four low offset, low power programmable gain amplifiers (PGA1, PGA2, PGA3, and PGA4). The gain of these amplifiers is programmable through the GAIN0 and GAIN1 pins.

Connect a resistor between the GAIN1 pin and ground to set different gains.

Pull up the GAIN0 pin to high or pull down the GAIN0 pin to low to choose different gain ranges.

A total of 15 gains can be obtained via different combinations of GAIN0 and GAIN1 settings. Table 8 shows the relationship between the gain and the GAIN0 and GAIN1 configurations.

Table 8. Gain Setting for PGAx

	GAIN	
Resistance on GAIN1 (kΩ)	**GAIN0 = Low**	**GAIN0 = High**
0	0.75	3
42.2	1	4
63.4	1.25	5
95.3	1.5	6
143	1.75	7
215	2	8
324	2.5	10
AVDD	4	16

The AVDD pin provides the voltage supply for the programmable gain amplifiers, and the output voltage of the amplifiers are clamped between zero and V_{AVDD}.

The output voltage of PGAx is calculated with the following equation:

$$V_{EOUTx} = \frac{V_{VCOM}}{2} - V_{EINx} \times GAIN$$

where:
V_{EOUTx} is the voltage on the EOUTx pin.
V_{VCOM} is the voltage on VCOM pin.
V_{EINx} is the voltage on the EINx pin.
GAIN is the gain value programmed by the GAIN0 and GAIN1 pins according to Table 8.

In a Rogowski application, as shown in Figure 75, connect a resistor between RCOM and ground to compensate for the passive, integrated dc resistor. Connect VCOM to AVDD or to a reference voltage derived from AVDD for the proper start-up sequence.

In the CT current sense application, connect both the VCOM and RCOM pins to ground.

OPERATIONAL AMPLIFIER

The operational amplifier is a low offset amplifier. The amplifier is used for leakage current detection in circuit breaker application.

Figure 67 shows the circuit configuration with the operational amplifier for leakage current detection as well as R1 and R2. The output voltage of the operational amplifier is calculated with the following equation:

$$V_{EOUT5} = \frac{V_{REF}}{2} - \frac{I_{LK}}{N} \times R_{ZCT} \times \frac{R_2}{R_1}$$

where:
V_{EOUT5} is the voltage on the EOUT5 pin.
V_{REF} is the external reference voltage.
I_{LK} is the leakage current.
N is the turn ratio of the zero-current transformer (ZCT).
R_{ZCT} is the current sense resistor at the secondary side of the ZCT.

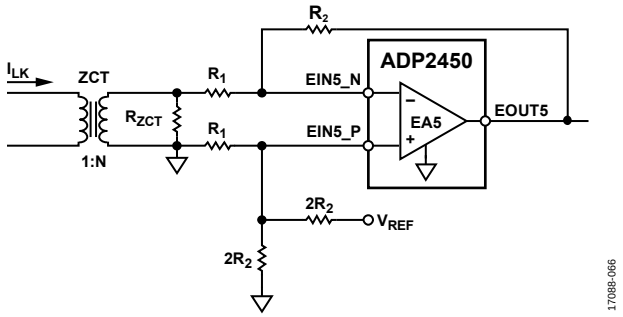


Figure 67. Typical Configuration for Leakage Current Detection

ANALOG TRIP PROTECTION

The ADP2450 integrates an analog trip circuit for fast protection in circuit breaker applications. The analog trip circuit monitors the output of each PGA. When any of the four PGA outputs exceeds the analog trip threshold, V_{TRP} or V_{TRPL}, for the deglitch time, t_{TRP}, the analog trip protection is triggered.

Two programmable analog trip thresholds, V_{TRP} and V_{TRPL}, support both half-sinusoid and bipolar sinusoid input signal application. V_{TRP} is the high threshold and V_{TRPL} is the low threshold. The PGAx output signal is compared with the two analog trip thresholds. If the PGAx output signal is either higher than V_{TRP} or lower than V_{TRPL}, the analog trip protection is triggered as shown in Figure 68.

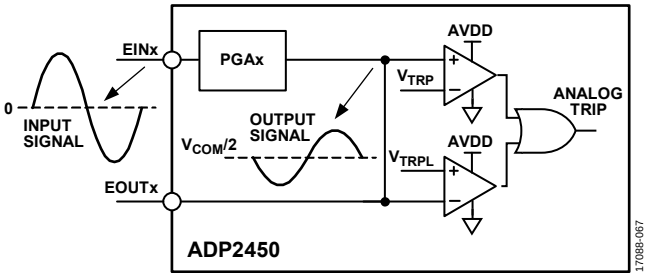


Figure 68. Analog Trip Circuit

The analog trip thresholds are programmable with external resistors and can be calculated using the following equations:

$$V_{TRP}(\mathrm{V}) = 0.01 \times R_{TRP}(\mathrm{k\Omega})$$

$$V_{TRPL}(\mathrm{V}) = 0.01 \times R_{TRPL}(\mathrm{k\Omega})$$

where:
V_{TRP} is the high analog trip threshold voltage.
V_{TRPL} is the low analog trip threshold voltage.
R_{TRP} is the resistance connected between the VTRP pin and ground.
R_{TRPL} is the resistance connected between the VTRPL pin and ground.

Note that there are limitations when choosing the R_{TRP} and R_{TRPL} values to set the analog trip thresholds. The following requirements must be met.

For R_{TRP} selection,

$$R_{TRP} < (V_{VREG} - 0.5) \times 100(\mathrm{k\Omega})$$

and

$$R_{TRP} < (V_{AVDD} - 0.1) \times 100(\mathrm{k\Omega})$$

For R_{TRP} selection,

$$R_{TRPL} > 30(\mathrm{k\Omega})$$

If the analog trip function is not used, connect both V_{TRP} and V_{TRPL} to VREG to disable the analog trip function.

In the CT current sense application where the input signal is half-sinusoid, only V_{TRP}, the high analog trip threshold, is needed. Connect V_{TRPL} to VREG to disable V_{TRPL}, the low analog trip threshold. Connect RCOM and VCOM to ground in this CT current sense application.

ACTUATOR DRIVER

The actuator driver receives the input signal either from the TRG pin or from the output of the analog trip control circuit. The driver also provides the gate drive voltage for the external thyristor through the GATE pin, as shown in Figure 69. When the analog trip protection is triggered, the analog trip control circuit outputs a 10 ms high, 6 ms low pulse signal. This pulse signal performs an OR logic with the signal on the TRG pin and inputs to the actuator driver circuit to provide the gate drive signal for the external thyristor or MOSFET. During this 16 ms period, the 10 ms high, 6 ms low pulse signal, any analog trip signal is ignored. If the analog trip signal is still active after the 16 ms period, another pulse that is 10 ms high, 6 ms low is generated. If the analog trip signal is cleared after the 16 ms period, the output of the analog trip control circuit latches to low. The GATE pin can be pulled up to VREG.

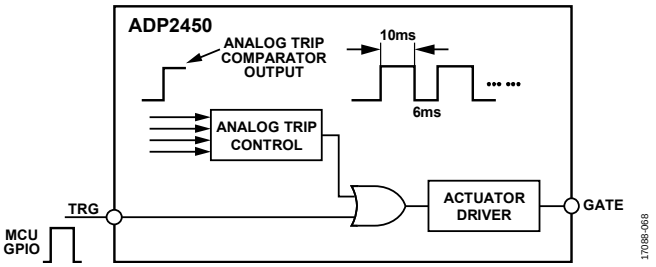


Figure 69. Actuator Driver Control Circuit

THERMAL SHUTDOWN

In the event that the ADP2450 junction temperature exceeds 150°C, the thermal shutdown circuit turns off most of the internal blocks but pulls the boost driver voltage (DRV pin) to high. A 15°C hysteresis is included so that the ADP2450 does not recover from thermal shutdown until the on-chip temperature drops below 135°C. Upon recovery, a soft start and power-up sequence is initiated prior to normal operation.

APPLICATIONS INFORMATION

OUTPUT CAPACITOR OF BOOST SHUNT CONTROLLER

The output capacitor stores the energy coming from the CT and provides the input voltage of the buck regulator as well as power to the actuator. Depending on the V_{OUT1} setting and actuator specification, the capacitance must be large enough so that it can provide sufficient power to trigger the actuator when the analog trip occurs and prevent the V_{OUT1} voltage from dropping.

The voltage rating of the boost shunt output capacitor must be higher than the output voltage of the boost shunt controller (V_{OUT1}). A margin of at least 20% must be reserved. Polymer, tantalum, and aluminum electrolytic capacitors are recommended for the balance between capacitance, voltage rating, and size. It is recommended to use a ceramic capacitor in the range from 1 µF to 10 µF in parallel with the output capacitor to reduce the total effective series resistance (ESR), thus reducing the output voltage ripple. Table 9 lists several recommended output capacitors for the boost shunt controller.

Table 9. Recommended Output Capacitors

Vendor	Part Number	Capacitance (µF)	Voltage (V)
KEMET	T521X336M050ATE075	33	50
	T521X476M035ATE070	47	35
	T494E476M035AT7280	47	35
	A767KN476M1HLAE029	47	50
Panasonic	EEFCX1V220R	22	35
	35SVPF39M	39	35
	50SVPF39M	39	50
	EEHZA1H680P	68	50
	EEHZA1H330XP	33	50

BRIDGE RECTIFIER

The bridge rectifier converts the sinusoid current of the CT secondary side to a half sinusoid current to provide power to the ADP2450. The average forward rectified current of the bridge rectifier diode (I_F) must be higher than the rms current of the CT secondary side during normal operation. The maximum dc blocking voltage of the bridge rectifier diode (V_{DC}) must be higher than the boost shunt controller output voltage (V_{OUT1}) of the ADP2450. Ensure that the peak forward surge current of the bridge rectifier diode (I_{FSM}) can handle the peak current of the CT secondary side when a fault occurs, such as when an analog trip is triggered.

Bridge rectifier diodes with low forward voltage are recommended. A low forward voltage reduces the power loss on the bridge rectifier diodes. However, the package size of the bridge rectifier increases. Table 10 lists several recommended bridge rectifiers for general applications.

Table 10. Recommended Bridge Rectifiers

Vendor	Part Number	I_F (A)	V_{DC} (V)	V_F (V)	I_{FSM} (A)
Bourns	CD2320-B1200	1	200	1	30
	CD2320-B1400	1	400	1	30
	CD2320-B1600	1	600	1	30
	CD2320-B1800	1	800	1	30
	CD2320-B11000	1	1000	1	30
Fairchild	MDB6S	1	600	1.1	30
	MDB8S	1	800	1.1	30
	MDB10S	1	1000	1.1	30

SENSE RESISTOR SELECTION

In a typical MCCB application, a sense resistor is connected between the negative output of the bridge rectifier and ground to convert the half sinusoid current signal to the half sinusoid voltage signal as the PGA input for signal coordination. The resistor value depends on the system rated current (I_N), the turn ratio of the current transformer, the PGA gain setting, and the PGA output low voltage.

A large resistor value provides a large input and output voltage signal of the PGA for easy sampling. However, a large resistor value increases the power loss on the sense resistor. A small resistor value reduces the power loss. However, a small resistor value decreases the PGA input and output voltage signal. Ensure that the lowest PGA output signal for the ADC sampling is higher than the output low voltage of the PGA so that the sampling accuracy of the small signal is not affected.

The resistor power must be high enough to handle the large current flowing through the sense resistor when the analog trip occurs. Table 11 lists several recommended sense resistors.

Table 11. Recommended Sense Resistors

Vendor	Part Number	Value (Ω)	Power (W)
Vishay Dale	WSC2515R5000FEA	0.5	1
	WSC25151R000FEA	1	1
	WSC25152R000FEA	2	1
Rohm	MCR100JZHFLR510	0.51	1
	LTR50UZPF1R00	1	1
	MCR100JZHFL2R00	2	1
Bourns	PWR2615WR500FE	0.5	1
	CRL2512-FW-1R00ELF	1	1
	CRL2512-FW-2R00ELF	2	1
	CRM2512-FX-2R00ELF	2	2

EXTERNAL MOSFET FOR BOOST SHUNT CONTROLLER

An N-channel external MOSFET is needed to control the CT current in the boost shunt controller.

When the external MOSFET is turned off, the current from the CT charges the output capacitor to V_{OUT1} through the boost shunt diode. The voltage added on the drain and source nodes of the MOSFET is equal to V_{OUT1} plus the diode forward voltage.

When the external MOSFET is turned on, it bypasses the CT current to ground. It is recommended to choose a MOSFET with a breakdown voltage (V_{DSS}) at least twice that of the output voltage of boost shunt controller (V_{OUT1}). It is also recommended that the continuous drain current (I_D) be larger than the CT secondary root mean square (rms) current when the analog trip occurs.

The MOFSET driver integrated in the ADP2450 has an 8 V output high voltage (V_{DRV_H}). Ensure that the gate to source voltage (V_{GS}) of the selected MOSFET is greater than 8 V, and that the gate threshold voltage (V_{GS_TH}) is lower than 8 V. Table 12 lists several recommended MOSFETs for the boost shunt controller.

Table 12. Recommended External MOSFETs

Vendor	Part Number	V_{DSS} (V)	I_D (A)
Infineon	IRFR3505PBF	55	30
	IRFR3518TRPBF	80	30
	BSC340N08NS3GATMA1	80	23
DIODES	DMN6068LK3-13	60	8.5
	DMN6013LFG-7	60	10.3
	DMT8012LFG-13	80	35
ON Semiconductor	FDMC86340	80	14
	NTTFS5820NLTAG	60	37
	FDS5670	60	10
	FDS3572	80	8.9

BOOST SHUNT DIODE SELECTION

The ADP2450 integrates a boost shunt controller that requires an external Schottky rectifier to conduct the CT current to the output capacitor of the boost shunt circuit when the external boost shunt MOSFET is turned off. Ensure that the Schottky diode peak current rating is larger than the maximum CT secondary current. The peak reverse voltage of the Schottky diode must be greater than the output voltage of boost shunt controller. To achieve the best efficiency, select a Schottky diode with a low forward voltage (V_F).

Table 13. Recommended Schottky Diodes

Vendor	Part Number	V_{RRM}[1] (V)	I_O[2] (A)
DIODES	B360A	60	3
	B350A	50	3
	B260A	60	2
ON Semiconductor	MBRS360BT3G	60	3
	MBRS260T3G	60	2
	NRVBS260T3G	60	2
Rohm	RB055LAM-60TR	60	3
	RB068LAM-60TR	60	2
Bourns	CD214A-B360LF	60	3

[1] V_{RRM} is the peak repetitive reverse voltage of the diodes.
[2] I_O is the forward current of the diodes.

INPUT CAPACITOR OF BUCK REGULATOR

The input capacitor reduces the input voltage ripple of the buck regulator caused by the switching current on VIN. Place the input capacitor as close as possible to the VIN pin. A 10 µF ceramic capacitor is recommended. The loop that is composed of this input capacitor, the high-side N-MOSFET, and the low-side N-MOSFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than the value calculated from the following equation:

$$I_{CIN\_RMS} = I_{OUT2} \times \sqrt{D \times (1-D)}$$

where:
I_{CIN_RMS} is the rms current of the input capacitor of buck regulator.
I_{OUT2} is the output current of the buck regulator.
D is the duty cycle of the buck regulator ($D = V_{OUT2}/V_{IN}$).

INDUCTOR SELECTION

The inductor value of the buck regulator is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor leads to a faster transient response but degrades efficiency due to a larger inductor ripple current, whereas using a large inductor value leads to smaller ripple current and improved efficiency but results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to one-third of the maximum load current. The inductor value is calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT2}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage of the buck regulator.
V_{OUT2} is the output voltage of the buck regulator.
ΔI_L is the inductor current ripple.
f_{SW} is the switching frequency of buck regulator.

The peak inductor current (I_{PEAK}) is calculated with the following equation:

$$I_{PEAK} = I_{OUT2} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be greater than the current-limit threshold of the switch. This greater saturation current rating prevents the inductor from reaching saturation.

The rms current of the inductor (I_{L_RMS}) is calculated with the following equation:

$$I_{L\_RMS} = \sqrt{{I_{OUT2}}^2 + \frac{{\Delta I_L}^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI).

OUTPUT CAPACITOR OF BUCK REGULATOR

The output capacitor selection affects the output ripple voltage of the buck regulator.

The output ripple is determined by the ESR and the capacitance value. Use the following equation to select a capacitor that meets the output ripple requirements (C_{OUT2_RIPPLE}):

$$C_{OUT2\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT2\_RIPPLE}}$$

where:
ΔV_{OUT2_RIPPLE} is the allowable output ripple voltage of the buck regulator.

$$R_{ESR} = \frac{\Delta V_{OUT2\_RIPPLE}}{\Delta I_L}$$

where R_{ESR} is the maximum equivalent series resistance of the buck regulator output capacitor in ohms (Ω).

Select the output capacitance to be larger than C_{OUT2_RIPPLE} and select the ESR value to be smaller than R_{ESR} to meet the output ripple.

The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor (I_{COUT2_RMS}) must be greater than the value that is calculated using the following equation:

$$I_{COUT2\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

OUTPUT VOLTAGE SETTING

Both the output voltage of boost shunt controller (V_{OUT1}) and buck regulator (V_{OUT2}) are set by the external resistor dividers, as shown in Figure 70 and Figure 71.

Boost Shunt Controller Output Voltage

The resistor values are calculated using the following equation:

$$V_{OUT1} = 1.2 \times \left(1 + \frac{R_{TOP1}}{R_{BOT1}}\right)$$

where:
R_{TOP1} is the top side feedback resistor of V_{OUT1}.
R_{BOT1} is the bottom side feedback resistor of V_{OUT1}.

To limit the output voltage accuracy degradation due to the FB1 bias current (0.1 μA maximum) to less than 0.5% (maximum), ensure that R_{BOT1} < 60 kΩ.

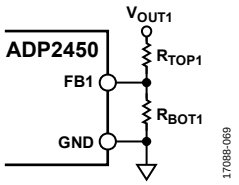


Figure 70. Boost Shunt Controller Output Voltage Setting

Buck Regulator Output Voltage

The buck regulator has the following two output voltage settings: adjustable output and fixed output.

For adjustable output voltage, connect the external resistor divider as shown Figure 71. The resistor values are calculated using the following equation:

$$V_{OUT2} = 0.6 \times \left(1 + \frac{R_{TOP2}}{R_{BOT2}}\right)$$

where:
R_{TOP2} is the top side feedback resistor of V_{OUT2}.
R_{BOT2} is the bottom side feedback resistor of V_{OUT2}.

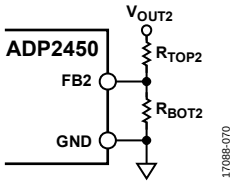


Figure 71. Buck Regulator Adjustable Output Voltage Setting

To limit the output voltage accuracy degradation due to FB2 bias current (0.1 μA maximum) to less than 0.5% (maximum), ensure that R_{BOT2} < 30 kΩ.

For fixed output voltage, connect FB2 to V_{OUT2} directly.

Buck Regulator Voltage Conversion Limitations

The minimum output voltage of a buck regulator for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2450 buck regulator is typically 50 ns. The minimum output voltage at a given input voltage and frequency is calculated using the following equation:

$$V_{OUT2\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT2\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT2\_MIN} \quad (1)$$

where:
V_{OUT2_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
I_{OUT2_MIN} is the minimum output current.
R_L is the series resistance of the output inductor.

The maximum output voltage of a buck regulator for a given input voltage and switching frequency is constrained by the minimum off time. The minimum off time of the ADP2450 buck regulator is typically 150 ns.

The maximum output voltage, limited by the minimum off time at a given input voltage and frequency, is calculated using the following equation:

$$V_{OUT2\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT2\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT2\_MAX} \quad (2)$$

where:
V_{OUT2_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT2_MAX} is the maximum output current.

EXTERNAL MOSFET FOR ACTUATOR

The ADP2450 has an integrated actuator driver. When the analog trip is triggered or the TRG pin is pulled up high, the internal actuator driver outputs a 5 V driver signal on the GATE pin and turns on the external MOSFET to trigger the actuator. The instantaneous current when the actuator is triggered is equal to V_{OUT1} divided by the resistance of the actuator. The continuous drain current of the MOSFET must be larger than the instantaneous current when the actuator is triggered. In normal operation where the MOSFET is turned off, V_{OUT1} the voltage added onto the drain and source nodes of the MOSFET. It is recommended to select a MOSFET with a V_{DSS} that is twice as large as V_{OUT1} to provide enough margin.

The recommended MOSFETs listed in Table 12 can also be used as the MOSFET for the actuator.

DESIGN EXAMPLE

This section describes the procedures for selecting the external components, based on a typical MCCB design example. The system specifications are listed in Table 14. See Figure 72 for the schematic for this design example.

Table 14. MCCB System Requirements

Parameter	Specification
Boost Shunt Controller Output Voltage	V_{OUT1} = 12 V
System Enable Threshold Voltage	V_{SYS_RISING} = 9 V
System Disable Threshold Voltage	$V_{SYS\_FALLING}$ = 7 V
Minimum System Consumption Current	I_{SYS_MIN} = 15 mA
Buck Regulator Output Voltage	V_{OUT2} = 3.3 V
Buck Regulator Output Voltage Ripple	V_{OUT2_RIPPLE} = 10 mV
Buck Regulator Output Current	I_{OUT2} = 100 mA
Single CT Secondary Current Under I_N (Rated Current)	I_{N_SEC} = 75 mA
Actuator Resistance	R_{ACT} = 4 Ω
Analog Trip Current at CT Secondary Side	I_{TRP_SEC} = 11 × I_{N_SEC}

BOOST SHUNT OUTPUT VOLTAGE SETTING

Choose a 11.3 kΩ resistor as the bottom feedback resistor (R_{BOT1}), and calculate the top feedback resistor using the following equation:

$$R_{TOP1} = \frac{V_{OUT1} \times R_{BOT1}}{1.2} - R_{BOT1}$$

To set the output voltage of boost shunt controller to 12 V, the resistor values are as follows: R_{TOP1} = 102 kΩ, and R_{BOT1} = 11.3 kΩ.

BOOST SHUNT OUTPUT CAPACITOR SETTING

The output capacitor of the boost shunt controller provides energy to the actuator. The value of the capacitor depends on the actuator specification and requirement. The capacitor value also affects the total system start-up time. A small value capacitor has fast system start-up time but may not provide enough energy for the actuator when the trip occurs. A large value capacitor has sufficient energy for the actuator but extends the system start-up time.

A capacitor value from 100 µF to 220 µF satisfies most of the actuator requirements in the MCCB application.

BOOST SHUNT MOSFET SETTING

The V_{DSS} of the MOSFET must be twice as large as V_{OUT1} to provide enough margin. Choose a MOSFET with V_{DSS} > 24 V.

In a worst case scenario where the analog trip occurs on all three phases, the current flowing through the MOSFET is 3 × I_{TRP_SEC} = 2.475 A. Choose a MOSFET with I_D > 3 A.

The V_{GS} voltage of the MOSFET must be higher than 8 V.

It is recommended to select the FDMC86340 from ON Semiconductor as the boost shunt MOSFET.

BOOST SHUNT DIODE SETTING

The V_{RRM} of the diode must be twice as large as V_{OUT1} to provide enough margin. Choose a Schottky diode with V_{RRM} > 24 V.

The peak current rating of the diode must be higher than 3 × I_{TRP_SEC} = 2.475 A to cover the worst case scenario. Choose a Schottky diode with $I_O \geq 3$ A.

It is recommended to select the MBRAF360T3G from ON Semiconductor as the boost shunt diode.

BUCK REGULATOR OUTPUT VOLTAGE SETTING

According to the system requirement, the output voltage of the buck regulator is 3.3 V. Select the ADP2450ACPZ-1-R7 model for a fixed 3.3 V output voltage of the buck regulator.

INDUCTOR SETTING

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the rated output current of the buck regulator. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN2} - V_{OUT2}) \times D}{\Delta I_L \times f_{SW}}$$

where:
$V_{IN2} = V_{OUT1}$ = 12 V.
V_{OUT2} = 3.3 V.
D = 0.275.
ΔI_L = 0.15 A.
f_{SW} = 1.2 MHz.

This calculation results in L = 13.3 µH. Choose the standard inductor value of 15 µH.

The inductor peak current is calculated by using the following equation:

$$I_{PEAK} = I_{OUT2} + \frac{(V_{IN2} - V_{OUT2}) \times D}{15\ \mu H \times f_{SW}} \times \frac{1}{2}$$

This calculation results in I_{PEAK} = 166 mA.

Based on the calculated current value, select an inductor with a minimum rms current rating of 200 mA. A shield inductor is preferred for improved system EMI performance.

It is recommended to select the LPS3015-153 from Coilcraft as the inductor of the buck regulator.

BUCK REGULATOR OUTPUT CAPACITOR SETTING

The output of the buck regulator provides the power supply for the PGAs, MCU, and LCD display. In most MCCB applications, the output voltage ripple requirement is important.

To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance values of the output capacitor of buck regulator:

$$C_{OUT2\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT2\_RIPPLE}}$$

$$ESR = \frac{V_{OUT2\_RIPPLE}}{\Delta I_L}$$

This calculation results in C_{OUT2_RIPPLE} = 1.56 µF and ESR = 66 mΩ. The output capacitance must be larger than 1.56 µF, and the output capacitor ESR value must be smaller than 66 mΩ to meet the output voltage ripple requirement. It is recommended to use a one piece, 10 µF ceramic capacitor (such as the GRM21BR70J106KE76 from Murata) as the output capacitor of the buck regulator.

VPTH RESISTOR DIVIDER SETTING

According to the system enable and disable voltage threshold requirements, use the following equation to calculate the VPTH resistor divider values (see Table 14 for the V_{SYS_RISING} and $V_{SYS\_FALLING}$ values):

$$R_{TOP\_VP} = \frac{1.09\ \text{V} \times V_{SYS\_RISING} - 1.22\ \text{V} \times V_{SYS\_FALLING}}{1.09\ \text{V} \times 4.8\ \mu\text{A} - 1.22\ \text{V} \times 1\ \mu\text{A}}$$

$$R_{BOT\_VP} = \frac{1.22\ \text{V} \times R_{TOP\_VP}}{V_{SYS\_RISING} - R_{TOP\_VP} \times 4.8\ \mu\text{A} - 1.22\ \text{V}}$$

This calculation results in R_{TOP_VP} = 316.6 kΩ and R_{BOT_VP} = 61.7 kΩ. Select a standard resistor value of 316 kΩ for R_{TOP_VP} and 61.9 kΩ for R_{BOT_VP}.

DUMMY LOAD RESISTOR SETTING

The dummy load, together with the power detection function, ensures that the system is not enabled until there is sufficient current provided by the CT.

Calculate the dummy load resistor value using the following equation:

$$R_{POWER} = \frac{V_{SYS\_RISING}}{I_{SYS\_MIN}}$$

This calculation results in R_{POWER} = 600 Ω. Choose the standard resistor value 604 Ω for R_{POWER}.

Calculate the power consumption on the dummy load resistor using the following equation (see Table 14 for the I_{SYS_MIN} value):

$$P_{DUMMY} = I_{SYS\_MIN}^{2} \times R_{POWER}$$

This calculation results in P_{DUMMY} = 0.136 W. Select one 604 Ω resistor with a 0805 package or two parallel 1.21 kΩ resistors with 0603 packages as the dummy load.

PGA GAIN SETTING

Set the PGA gain to ×1 as a start point. According to Table 8, connect a 42.2 kΩ resistor between the GAIN1 pin and ground. Connect the GAIN0 pin to an input/output (I/O) pin of the MCU. If needed, switch the PGA gain between ×1 and ×4 by setting the GAIN0 pin to low and high, respectively.

SENSE RESISTOR SETTING

Choose a 2 Ω resistor as the sense resistor for each phase to set the input voltage of PGA to 150 mV under the rated current, I_N.

The power consumption on the sense resistor (P_{SENSE_MAX}) when the analog trip occurs is calculated using the following equation (see Table 14 for the I_{TRP_SEC} value):

$$P_{SENSE\_MAX} = I_{TRP\_SEC}^{2} \times R_{SENSE}$$

where:
R_{SENSE} is the sense resistor value.

This calculation results in P_{SENSE_MAX} = 1.36 W. Select a 2 Ω, 2 W resistor, such as the CRM2512-FX-2R00ELF from Bourns, as the sense resistor.

ANALOG TRIP THRESHOLD SETTING

The PGA output voltage is a half-sinusoid waveform. Calculate the PGA output voltage peak value (V_{PGA_PEAK}) when the analog trip is triggered by using the following equation:

$$V_{PGA\_PEAK} = I_{TRP\_SEC} \times R_{SENSE} \times \sqrt{2} \times GAIN$$

where $GAIN$ = 1.

This calculation results in V_{PGA_PEAK} = 2.333 V.

Consider that the analog trip has a default 200 µs delay time, which results in a 3.6° phase delay of the half-sinusoid waveform. Set the analog trip threshold voltage using the following equation:

$$V_{TRP} = V_{PGA\_PEAK} \times \sin 86.4°$$

This calculation results in V_{TRP} = 2.328 V.

Calculate the trip resistor value (R_{TRP}) using the following equation:

$$R_{TRP} = \frac{V_{TRP}}{I_{TRP}}$$

This calculation results in R_{TRP} = 232.8 kΩ. Choose a standard resistor value of 232 kΩ as the analog trip resistor.

ACTUATOR MOSFET SETTING

The V_{DSS} of the MOSFET must be twice as large as V_{OUT1} to provide enough margin. Choose a MOSFET with V_{DSS} > 24 V.

When the actuator is triggered, the instantaneous current flowing through the MOSFET is V_{OUT1}/R_{ACT} = 3 A. Select a MOSFET with I_D > 3 A.

The V_{GS} voltage of the MOSFET must be higher than 5 V.

It is recommended to select the FDMC86340 from ON Semiconductor as the actuator MOSFET.

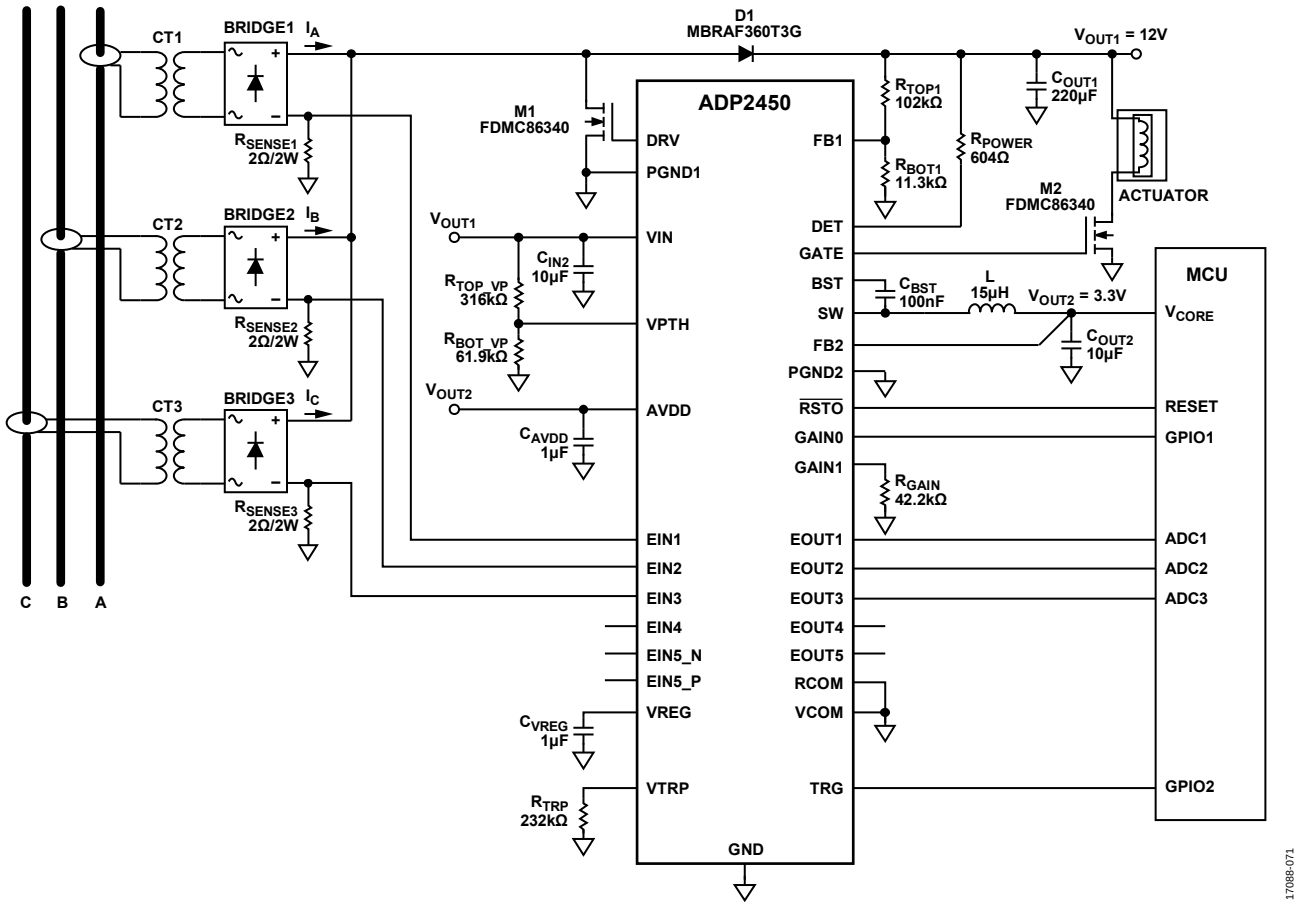


Figure 72. Schematic for Design Example, Single Coil, Three Phases Sense

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

In any switching power supply, there are some circuit paths that carry high dI/dt, the current changing rate, which creates spikes and noises. Some circuit paths are sensitive to noise, such as feedback traces, error amplifier input and output traces, which must be devoid of spikes and noises. The key to proper PCB layout is to identify these critical paths and arrange the components and the copper area accordingly to keep the paths away from noise sources. When designing PCB layouts, be sure to keep high current loops small. In addition, keep sensitive trances and components away from the switching nodes and their associated components.

The following sections describe the recommended layout rules for the ADP2450. Figure 73 shows a recommended PCB layout for single coil application.

GROUND PLANES

Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, amplifier output resistor and capacitor (RC) filters, and a common voltage reference, to analog ground. Connect the ground reference of the power components, such as input and output capacitors, and external MOSFETs to power ground. Use internal ground planes to connect the analog ground plane and the power ground plane together.

In addition, connect the exposed pad of the ADP2450 to a large, external copper ground plane to maximize the power dissipation capability and minimize junction temperature.

SWITCH NODE

The switch node is the noisiest location in the switch power supply circuit with large ac and dc voltages and currents. The following two switch nodes are in the ADP2450 circuit: the external MOSFET drain of the boost shunt controller and the SW pin of the buck regulator. These nodes must be wide to prevent the resistive voltage from dropping. To minimize the generation of capacitively coupled noise, the total area of each switch node must be small.

For the boost shunt controller, place the bridge rectifiers, the MOSFET, the rectifier diode, and the output capacitors as close as possible to each other, and use wide short traces or copper planes. Ensure that the high current loop traces are as short and as wide as possible.

For the buck regulator, place the input capacitor, the inductor, and the output capacitor as close as possible to the IC, and use short traces. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. In addition, ensure that the high current path from the power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the ADP2450 PGND2 pin to the power ground plane as close as possible to the input and output capacitors.

FEEDBACK PATHS

The feedback traces of FB1 and FB2 are very sensitive to noise. Place the feedback resistor divider networks as close as possible to the FBx pins to prevent noise pickup. Minimize the length of the feedback traces that connect the top of the feedback resistor dividers to the output while keeping these traces away from the high current traces and the switching nodes to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FBx traces and ensure that the traces are as short as possible to reduce the parasitic capacitance pickup.

POWER TRACES

In the ADP2450 circuit design, the output of the boost shunt controller, V_{OUT1}, is connected to the input of buck regulator. The output of buck regulator, V_{OUT2}, is connected to the AVDD providing power to the internal PGAs. These two traces are power traces and may carry high currents. Use internal power planes for the power trace connections and keep these power traces as short and wide as possible to minimize the voltage drops on them under high current situations.

SIGNAL PATHS

The input and output of all the amplifiers, the common voltage input, the TRG trace, and the VTRP signals are all signal paths. Keep these signal paths away from switch nodes and high current paths to avoid noise pickup. Connect the ground reference of these signal paths to the analog ground plane using short and wide traces.

GATE DRIVER PATHS

The gate drive traces, DRV and GATE, of external MOSFETs handle high dI/dt and tend to produce noise and ringing. The gate drive traces must be as short and direct as possible. Avoid using feedthrough vias in the gate drive traces. If vias are needed, it is recommended to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can help reduce noise and ringing. It may be helpful to place small value resistors, between 2 Ω and 10 Ω, on the DRV and GATE pins. These locations can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times, as well as switching power loss in the MOSFETs.

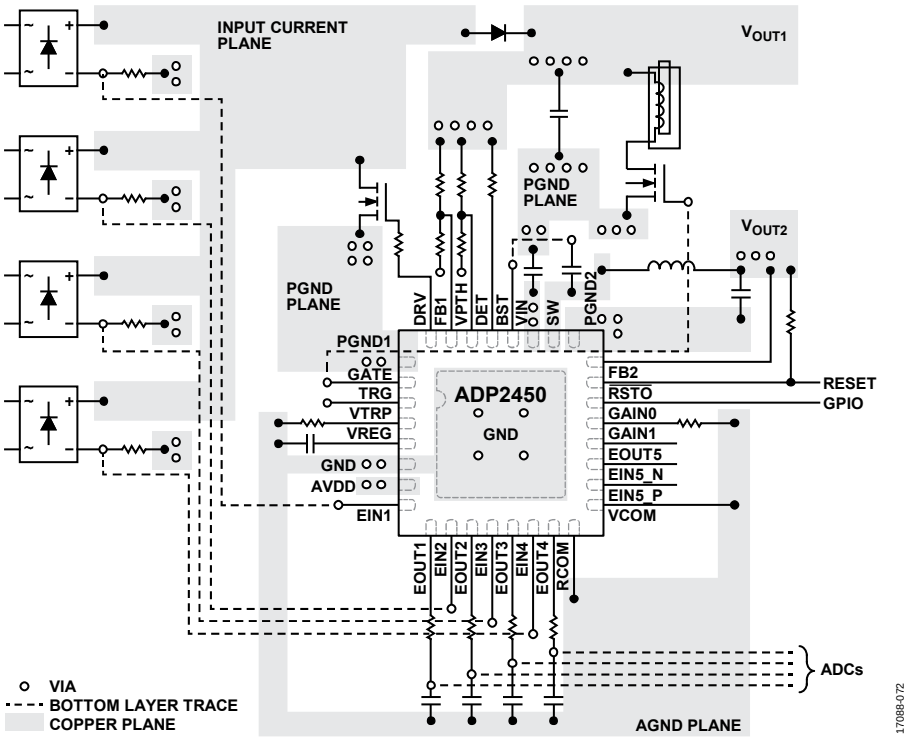


Figure 73. Recommended PCB Layout for Single Coil Application, 32-Lead LFCSP Package

TYPICAL APPLICATION CIRCUITS

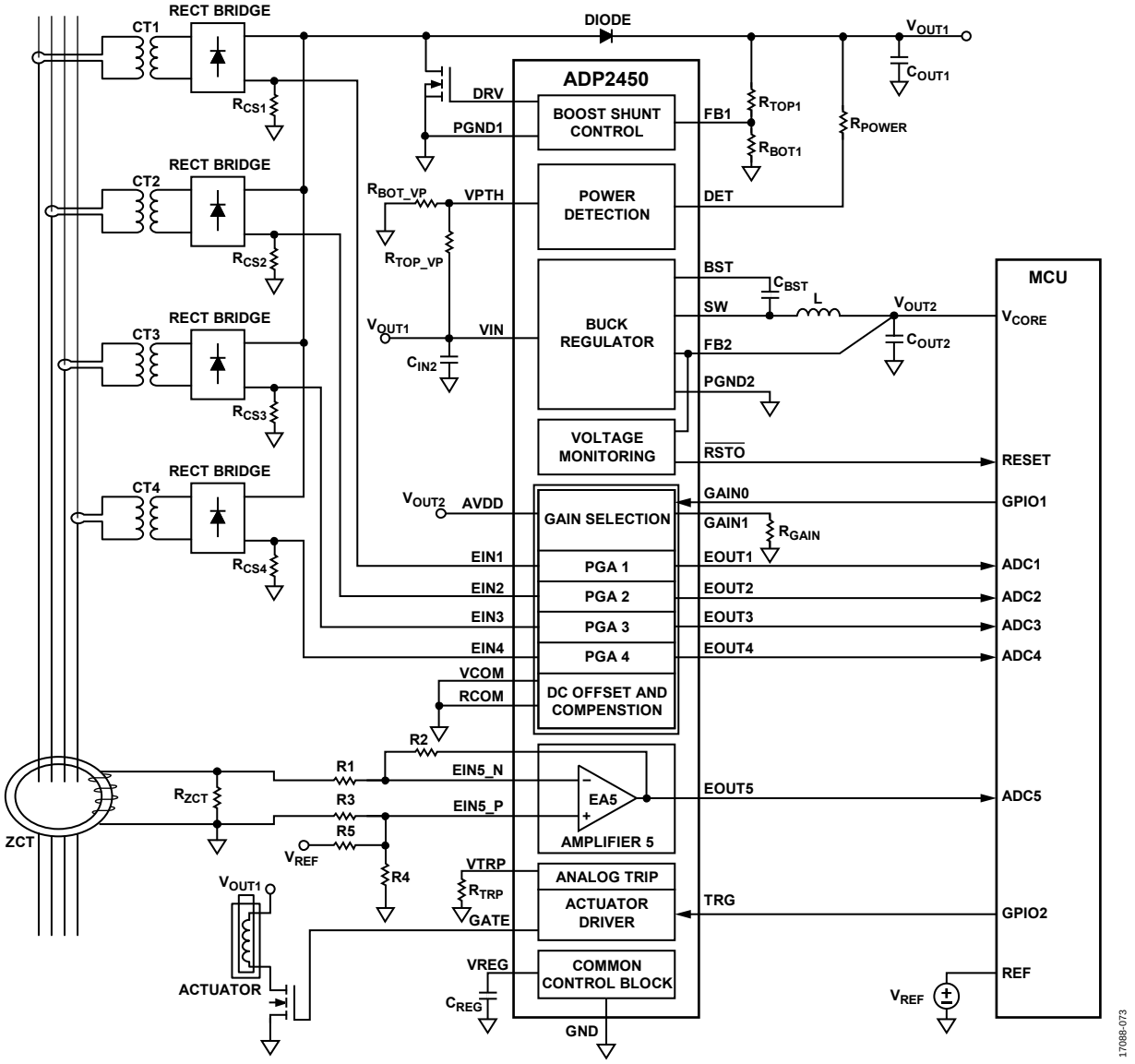


Figure 74. Application Circuit—Single Coil, Signal and Power Share the Same CT

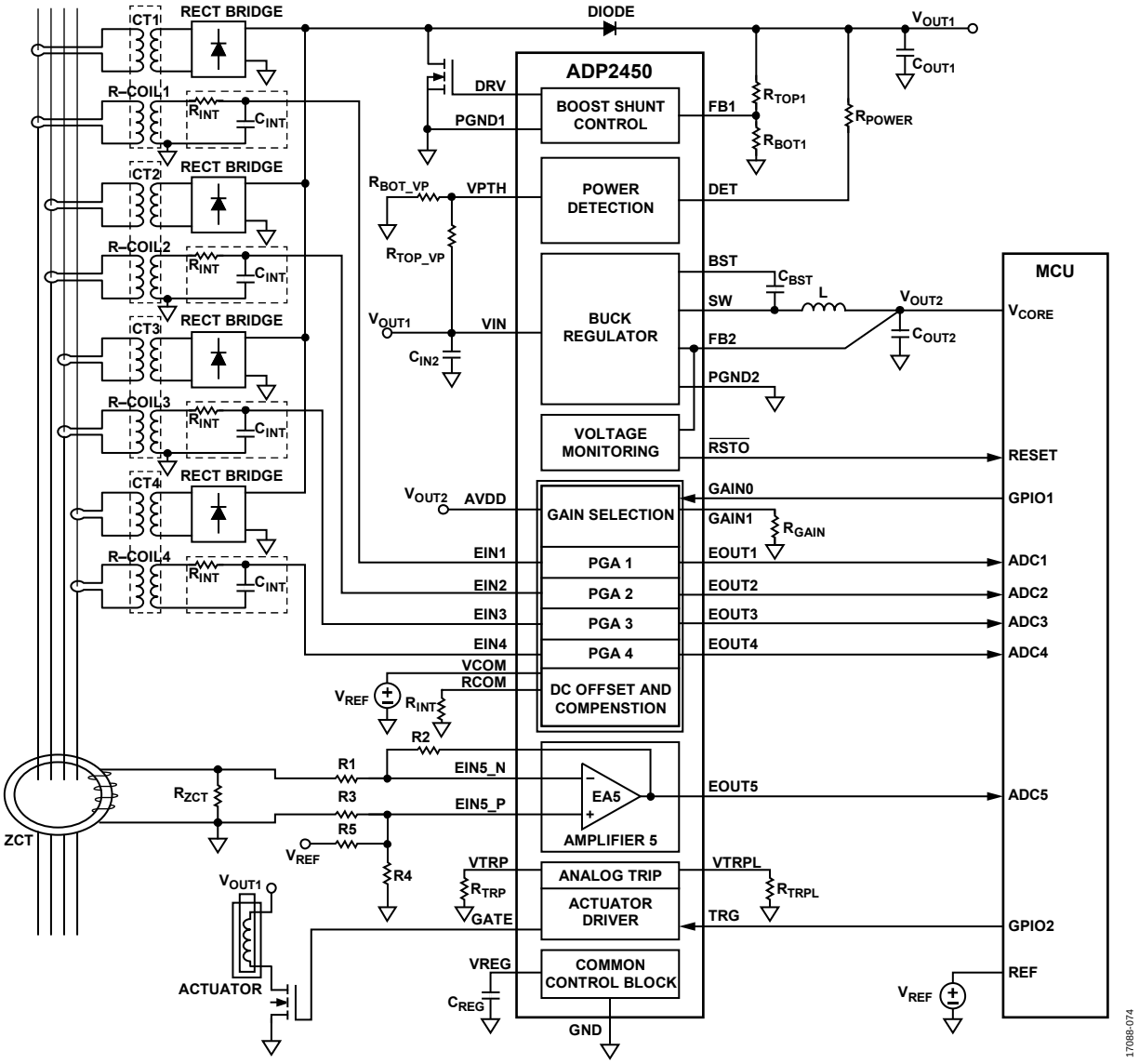


Figure 75. Application Circuit—Dual Coil, CT Provides Power and Rogowski Coils Provide Signal

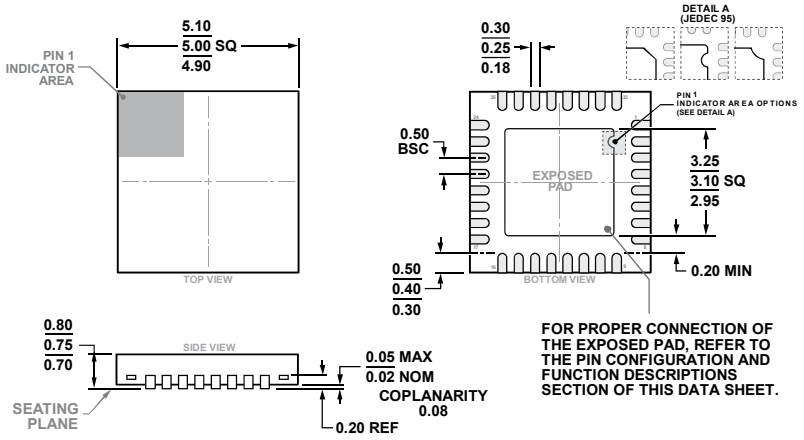
FACTORY-PROGRAMMABLE OPTIONS

The output voltage of the buck regulator, the reset rising delay time ($t_{RST\_DELAY\_R}$), and the analog trip deglitch time (t_{TRP}) can be preset to one of the options listed in Table 15. To order a device with options other than the default options, contact a local Analog Devices, Inc., sales or distribution representative.

Table 15. Fuse Selectable Trim Options

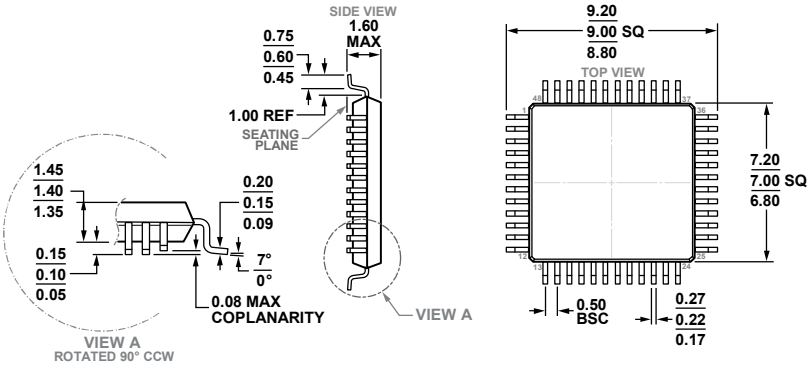
Parameter	Options
Buck Regulator Output Voltage	Adjustable, 3.3 V, 5 V
Reset Rising Delay Time ($t_{RST\_DELAY\_R}$)	0.5 ms (default), 1 ms, 2 ms, 5 ms
Analog Trip Deglitch Time (t_{TRP})	200 µs (default), 350 µs, 500 µs, 750 µs, 1 ms, 2 ms, 3 ms, 4 ms

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD

Figure 76. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 77. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Buck Output Voltage	Analog Trip Deglitch Time	Reset Rising Delay Time	Package Description	Package Option
ADP2450ACPZ-1-R7	−40°C to +125°C	3.3 V	200 µs	0.5 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-2-R7	−40°C to +125°C	5 V	200 µs	0.5 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-3-R7	−40°C to +125°C	Adjustable	200 µs	0.5 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-4-R7	−40°C to +125°C	Adjustable	200 µs	2 ms	32-Lead LFCSP	CP-32-7
ADP2450ACPZ-5-R7	−40°C to +125°C	5 V	500 µs	5 ms	32-Lead LFCSP	CP-32-7
ADP2450ASTZ-1-R7	−40°C to +125°C	3.3 V	500 µs	0.5 ms	48-Lead LQFP	ST-48
ADP2450ASTZ-2-R7	−40°C to +125°C	5 V	500 µs	0.5 ms	48-Lead LQFP	ST-48
ADP2450ASTZ-3-R7	−40°C to +125°C	Adjustable	500 µs	0.5 ms	48-Lead LQFP	ST-48
ADP2450ASTZ-4-R7	−40°C to +125°C	Adjustable	500 µs	2 ms	48-Lead LQFP	ST-48
ADP2450ASTZ-5-R7	−40°C to +125°C	5 V	500 µs	2 ms	48-Lead LQFP	ST-48
ADP2450ACPZ-3-EVBZ		Adjustable	200 µs	0.5 ms	32-Lead LFCSP Evaluation Board	
ADP2450ASTZ-3-EVBZ		Adjustable	500 µs	0.5 ms	48-Lead LQFP Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D17088-0-7/19(B)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADP2450ACPZ-3-R7 ADP2450ACPZ-1-R7 ADP2450ACPZ-2-R7 ADP2450ACPZ-4-R7 ADP2450ASTZ-3-EVBZ ADP2450ACPZ-3-EVBZ ADP2450ASTZ-1-R7 ADP2450ASTZ-5-R7 ADP2450ASTZ-2-R7 ADP2450ASTZ-3-R7 ADP2450ASTZ-4-R7 ADP2450ACPZ-5-R7