Dual-Phase, Quick-PWM Controllers for Programmable CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
V_{CC} to GND .....-0.3V to +6V
V_{DD} to PGND .....-0.3V to +6V
$\overline{SKIP}$, SUS, D0–D4 to GND .....-0.3V to +6V
ILIM, FB, OFS, CCV, CCI, REF, OAIN+,
OAIN- to GND .....-0.3V to (V_{CC} + 0.3V)
CMP, CSP, CMN, CSN, GNDS to GND .....-0.3V to (V_{CC} + 0.3V)
TON, TIME, VROK, S0–S1, CODE to GND .-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 1) .....-0.3V to +18V
DLM, DLS to PGND .....-0.3V to (V_{DD} + 0.3V)
BSTM, BSTS to GND .....-0.3V to +36V
DHM to LXM .....-0.3V to (V_{BSTM} + 0.3V)
LXM to BSTM .....-6V to +0.3V
DHS to LXS .....-0.3V to (V_{BSTS} + 0.3V)
LXS to BSTS .....-6V to +0.3V
GND to PGND .....-0.3V to +0.3V
REF Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin 6mm × 6mm Thin QFN
(derate 23.2mW/°C above +70°C) 1.860W
Operating Temperature Range .....-40°C to +100°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ may be forced to 12V for the purpose of debugging prototype boards using the no-fault test mode, which disables fault protection and overlapping operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery voltage, V+		4		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy (Note 2)		V+ = 4.5V to 28V, includes load regulation error	DAC codes ≥ 1V	-10		+10	mV
			DAC codes from 0.60V to 1V	-15		+15	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
Input Bias Current	I_{FB}, I_{GNDS}	FB, GNDS		-2		+2	µA
	I_{OFS}	OFS		-0.1		+0.1	
OFS Input Range				0		2	V
OFS Gain	A_{OFS}	$\Delta V_{OUT}/\Delta V_{OFS}$; ΔV_{OFS} = V_{OFS}, V_{OFS} = 0 to 1V		-0.129	-0.125	-0.117	V/V
		$\Delta V_{OUT}/\Delta V_{OFS}$; ΔV_{OFS} = V_{OFS} - V_{REF}, V_{OFS} = 1V to 2V		-0.129	-0.125	-0.117	
GNDS Input Range				-20		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	0.99	1.01	V/V
TIME Frequency Accuracy	f_{TIME}	1000kHz nominal, R_{TIME} = 15kΩ		900	1000	1100	kHz
		500kHz nominal, R_{TIME} = 30kΩ		460	500	540	
		250kHz nominal, R_{TIME} = 60kΩ		225	250	275	
		Shutdown, R_{TIME} = 30kΩ			125		

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time (Note 3)	t_{ON}	V+ = 12V, V_{FB} = V_{CCI} = 1.2V	TON = GND (550kHz)	155	180	205	ns
			TON = REF (300kHz)	320	355	390	
			TON = open (200kHz)	475	525	575	
			TON = V_{CC} (100kHz)	920	1000	1140	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	TON = GND			300	375	ns
		TON = V_{CC}, open, or REF			400	480	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point, OAIN- = FB, V_{OAIN+} = 1.3V			1.70	3.20	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			<1	5	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+			25	40	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			4	10	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND			<1	5	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.990	2.000	2.010	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to +100µA		-10		+10	mV
FAULT PROTECTION							
Output Overvoltage Protection Threshold (MAX1545 Only)	V_{OVP}	$\overline{SKIP}$ = V_{CC}, measured at FB with respect to unloaded output voltage		13	16	19	%
		$\overline{SKIP}$ = REF or GND			2.00		V
Output Overvoltage Propagation Delay (MAX1545 Only)	t_{OVP}	FB forced 2% above trip threshold			10		µs
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		67	70	73	%
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 2% below trip threshold			10		µs
VROK Threshold		Measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-12	-10	-8	%
			Upper threshold (overvoltage) $\overline{SKIP}$ = V_{CC}	+8	+10	+12	

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage Fault and VROK Transition Blanking Time (Note 4)	t_{BLANK}	Measured from the time when FB reaches the voltage set by the DAC code; clock speed set by R_{TIME}			24		Clks
VROK Startup Delay		Measured from the time when FB first reaches the voltage set by the DAC code after startup		3	5	7	ms
VROK Delay	t_{VROK}	FB forced 2% outside the VROK trip threshold			10		µs
VROK Output Low Voltage		I_{SINK} = 3mA				0.4	V
VROK Leakage Current		High state, VROK forced to 5.5V				1	µA
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 90mV, PWM disabled below this level		4.0	4.25	4.4	V
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 10°C			160		°C
CURRENT LIMIT AND BALANCE							
Current-Limit Threshold Voltage (Positive, Default)	V_{LIMIT}	CMP - CMN, CSP - CSN; ILIM = V_{CC}		28	30	32	mV
Current-Limit Threshold Voltage (Positive, Adjustable)	V_{LIMIT}	CMP - CMN, CSP - CSN	V_{ILIM} = 0.2V	8	10	12	mV
			V_{ILIM} = 1.5V	73	75	77	
Current-Limit Threshold Voltage (Negative)	$V_{LIMIT(NEG)}$	CMP - CMN, CSP - CSN; ILIM = V_{CC}, $\overline{SKIP}$ = V_{CC}		-41	-36	-31	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	CMP - CMN, CSP - CSN; $\overline{SKIP}$ = GND			1.5		mV
CMP, CMN, CSP, CSN Input Ranges				0		2	V
CMP, CMN, CSP, CSN Input Current		V_{CSP} = V_{CSN} = 0 to 5V		-2		+2	µA
Secondary Driver-Disable Threshold	V_{CSP}			3	V_{CC} - 1	V_{CC} - 0.4	V
ILIM Input Current	I_{ILIM}	V_{ILIM} = 0 to 5V			0.1	200	nA
Current-Limit Default Switchover Threshold	V_{ILIM}			3	V_{CC} - 1	V_{CC} - 0.4	V
Current-Balance Offset	$V_{OS(IBAL)}$	(V_{CMP} - V_{CMN}) - (V_{CSP} - V_{CSN}); I_{CCI} = 0, -20mV < (V_{CMP} - V_{CMN}) < 20mV, 1.0V < V_{CCI} < 2.0V		-2		+2	mV
Current-Balance Transconductance	$G_{m(IBAL)}$				400		µS

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V			1.0	4.5	Ω
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			1.0	4.5	Ω
		Low start (pulldown)			0.4	2	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			1.6		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 5V			4		A
DL_ Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			1.6		A
Dead Time	t_{DEAD}	DL_ rising			35		ns
		DH_ rising			26		
VOLTAGE-POSITIONING AMPLIFIER							
Input Offset Voltage	V_{OS}			-1		+1	mV
Input Bias Current	I_{BIAS}	OAIN+, OAIN-			0.1	200	nA
Op Amp Disable Threshold	V_{OAIN-}			3	V_{CC} - 1	V_{CC} - 0.4	V
Common-Mode Input Voltage Range	V_{CM}	Guaranteed by CMRR test		0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{OAIN+} = V_{OAIN-} = 0 to 2.5V		70	115		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V		75	100		dB
Large-Signal Voltage Gain	A_{OA}	R_L = 1kΩ to V_{CC}/2		80	112		dB
Output Voltage Swing		$\lvert V_{OAIN+} - V_{OAIN-} \rvert \geq$ 10mV, R_L = 1kΩ to V_{CC}/2	$V_{CC} - V_{FBH}$		77	300	mV
			V_{FBL}		47	200	
Input Capacitance					11		pF
Gain-Bandwidth Product					3		MHz
Slew Rate					0.3		V/µs
Capacitive-Load Stability		No sustained oscillations			400		pF
LOGIC AND I/O							
$\overline{SHDN}$ Input High Voltage	V_{IH}			0.8			V
$\overline{SHDN}$ Input Low Voltage	V_{IL}					0.4	V
$\overline{SHDN}$ No-Fault Threshold	$V_{\overline{SHDN}}$			12		15	V
Three-Level Input Logic Levels		SUS, $\overline{SKIP}$	High	2.7			V
			REF	1.2		2.3	
			Low			0.8	
Logic Input Current		$\overline{SHDN}$, SUS, $\overline{SKIP}$		-1		+1	µA
D0–D4 Logic Input High Voltage				1.6			V
D0–D4 Logic Input Low Voltage						0.8	V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
D0–D4 Input Current		D0–D4		-2		+2	µA
CODE Input High Voltage				2.4			V
CODE Input Low Voltage						0.8	V
CODE Input Current				-1		+1	µA
Four-Level Input Logic Levels		TON, S0–S1	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.4	
Four-Level Input Current		TON, S0–S1 forced to GND or V_{CC}		-3		+3	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery voltage, V+		4		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy (Note 2)		V+ = 4.5V to 28V, includes load regulation error	DAC codes ≥ 1V	-13		+13	mV
			DAC codes from 0.60V to 1V	-20		+20	
OFS Input Range				0		2	V
OFS Gain	A_{OFS}	$\Delta V_{OUT}/\Delta V_{OFS}$; ΔV_{OFS} = V_{OFS}, V_{OFS} = 0 to 1V		-0.131		-0.115	V/V
		$\Delta V_{OUT}/\Delta V_{OFS}$; ΔV_{OFS} = V_{OFS} - V_{REF}, V_{OFS} = 1V to 2V		-0.131		-0.115	
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.94		1.01	V/V
TIME Frequency Accuracy	f_{TIME}	1000kHz nominal, R_{TIME} = 15kΩ		880		1120	kHz
		500kHz nominal, R_{TIME} = 30kΩ		450		550	
		250kHz nominal, R_{TIME} = 60kΩ		220		280	
On-Time (Note 3)	t_{ON}	V+ = 12V, V_{FB} = V_{CCI} = 1.2V	TON = GND (550kHz)	150		210	ns
			TON = REF (300kHz)	315		395	
			TON = open (200kHz)	470		580	
			TON = V_{CC} (100kHz)	910		1150	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	TON = GND				380	ns
		TON = V_{CC}, open, or REF				490	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point, OAIN- = FB, V_{OAIN+} = 1.3V				3.2	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point				20	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+				50	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND				20	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND				20	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0 or 5V				20	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.985		2.015	V
FAULT PROTECTION							
Output Overvoltage Protection Threshold (MAX1545 Only)	V_{OVP}	$\overline{SKIP}$ = V_{CC}, measured at FB with respect to unloaded output voltage		13		19	%
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		67		73	%
VROK Threshold		Measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-13		-7	%
			Upper threshold (overvoltage) $\overline{SKIP}$ = V_{CC}	+7		+13	
VROK Startup Delay		Measured from the time when FB first reaches the voltage set by the DAC code after startup		3			ms
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 90mV, PWM disabled below this level		3.90		4.45	V
CURRENT LIMIT AND BALANCE							
Current-Limit Threshold Voltage (Positive, Default)	V_{LIMIT}	CMP - CMN, CSP - CSN; ILIM = V_{CC}		27		33	mV
Current-Limit Threshold Voltage (Positive, Adjustable)	V_{LIMIT}	CMP - CMN, CSP - CSN	V_{ILIM} = 0.2V	7		13	mV
			V_{ILIM} = 1.5V	72		78	
Current-Limit Threshold Voltage (Negative)	$V_{LIMIT(NEG)}$	CMP - CMN, CSP - CSN; ILIM = V_{CC}, $\overline{SKIP}$ = V_{CC}		-30		-42	mV
Current-Balance Offset	$V_{OS(IBAL)}$	(V_{CMP} - V_{CMN}) - (V_{CSP} - V_{CSN}); I_{CCI} = 0, -20mV < (V_{CMP} - V_{CMN}) < 20mV, 1.0V < V_{CCI} < 2.0V		-3		+3	mV

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{TON} = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = V_{CODE} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D4 = GND; **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V				4.5	Ω
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				4.5	Ω
		Low start (pulldown)				2	
VOLTAGE-POSITIONING AMPLIFIER							
Input Offset Voltage	V_{OS}			-2.0		+2.0	mV
Common-Mode Input Voltage Range	V_{CM}	Guaranteed by CMRR test		0		2.5	V
Output Voltage Swing		$\lvert V_{OAIN+} - V_{OAIN-} \rvert \geq 10mV$, R_L = 1kΩ to $V_{CC}/2$	V_{CC} - V_{FBH}			300	mV
			V_{FBL}			200	
LOGIC AND I/O							
$\overline{SHDN}$ Input High Voltage	V_{IH}			0.8			V
$\overline{SHDN}$ Input Low Voltage	V_{IL}					0.4	V
Three-Level Input Logic Levels		SUS, $\overline{SKIP}$	High	2.7			V
			REF	1.2		2.3	
			Low			0.8	
D0–D4 Logic Input High Voltage				1.6			V
D0–D4 Logic Input Low Voltage						0.8	V
CODE Input High Voltage				2.4			V
CODE Input Low Voltage						0.8	V
Four-Level Input Logic Levels		TON, S0–S1	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.4	

Note 2: DC output accuracy specifications refer to the trip level of the error amplifier. When pulse skipping, the output slightly rises (< 0.5%) when transitioning from continuous conduction to no load.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DHM and DHS pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

Note 4: The output fault-blanking time is measured from the time when FB reaches the regulation voltage set by the DAC code. During normal operation (SUS = GND), regulation voltage is set by the VID DAC inputs (D0–D4). During suspend mode (SUS = REF or high), the regulation voltage is set by the suspend DAC inputs (S0–S1).

Note 5: Specifications to T_A = -40°C and +100°C are guaranteed by design and are not production tested.

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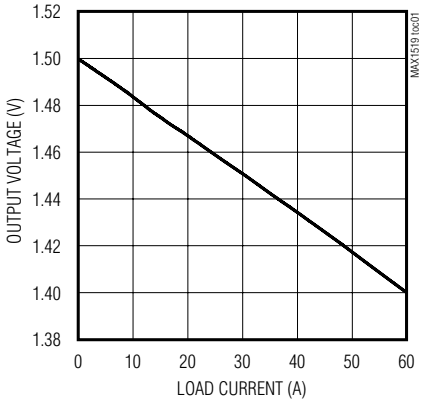
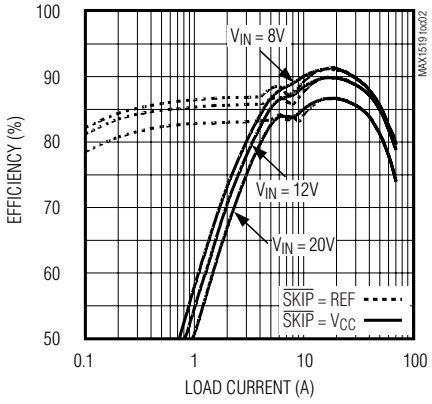
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D4 set for 1.5V (SUS = GND), S0–S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

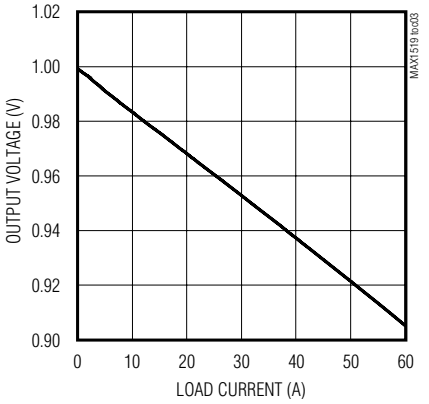
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.50V)



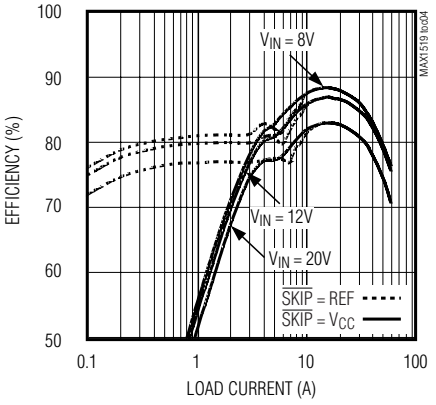
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.50V)



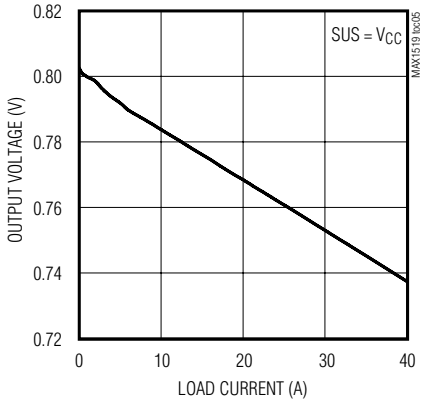
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.00V)



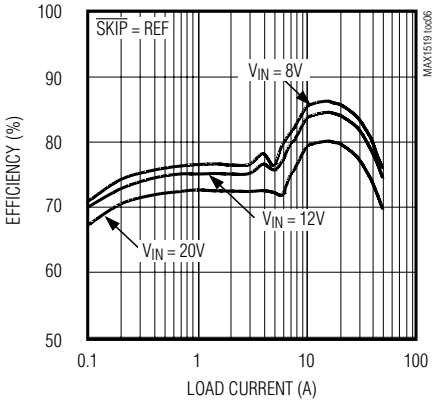
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.00V)



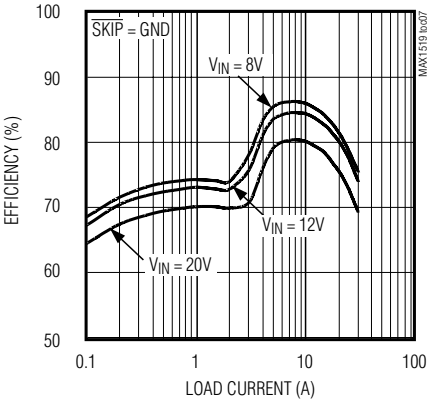
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.80V)



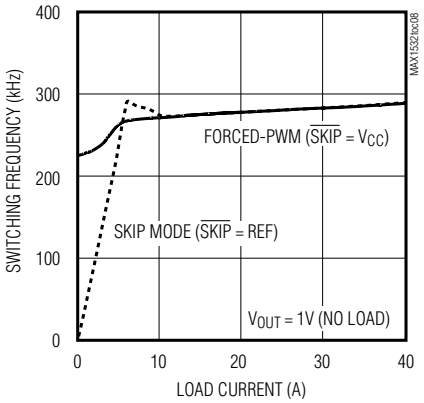
DUAL-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.80V)



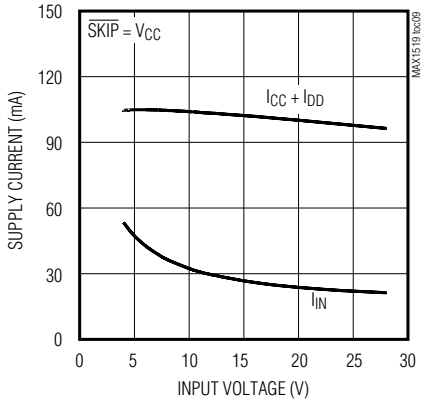
SINGLE-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.80V)



SWITCHING FREQUENCY vs. LOAD CURRENT



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM MODE)

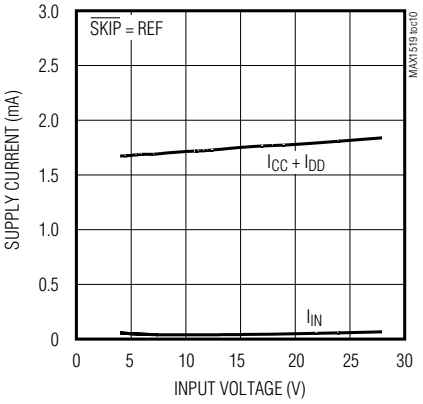


Dual-Phase, Quick-PWM Controllers for Programmable CPU Core Power Supplies

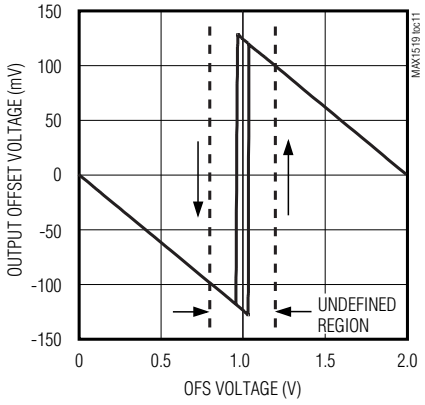
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D4 set for 1.5V (SUS = GND), S0–S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

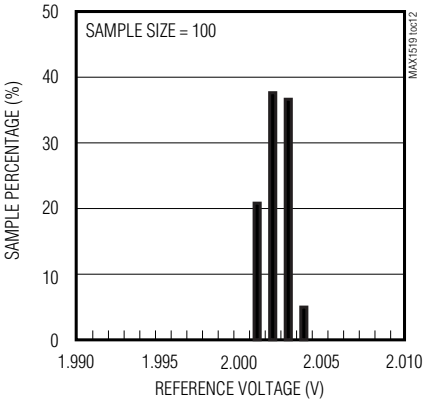
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PULSE SKIPPING)



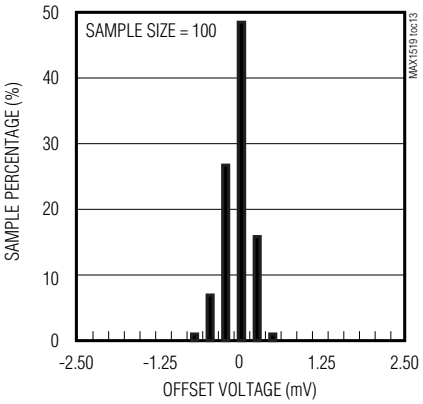
OUTPUT OFFSET VOLTAGE vs. OFS VOLTAGE



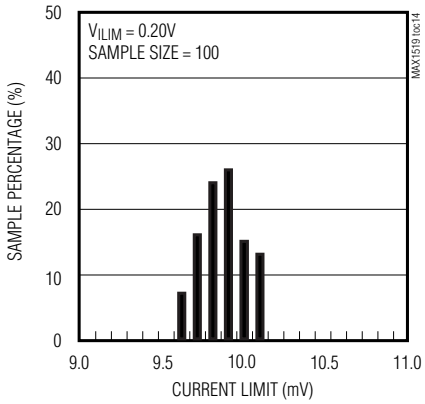
REFERENCE VOLTAGE DISTRIBUTION



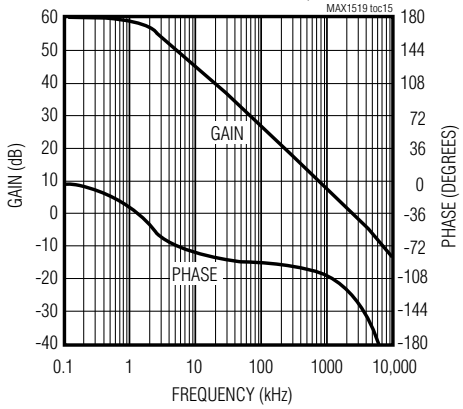
CURRENT-BALANCE OFFSET VOLTAGE DISTRIBUTION



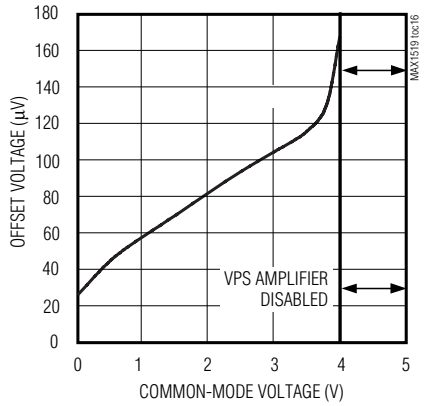
CURRENT-LIMIT THRESHOLD DISTRIBUTION



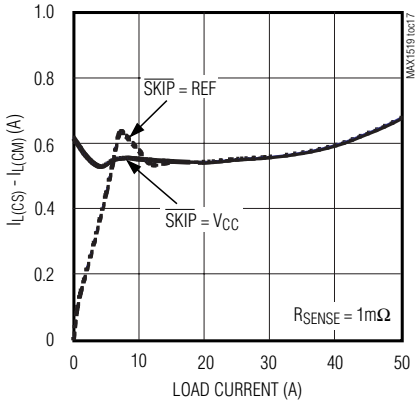
VOLTAGE-POSITIONING AMPLIFIER GAIN AND PHASE vs. FREQUENCY



VPS AMPLIFIER OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



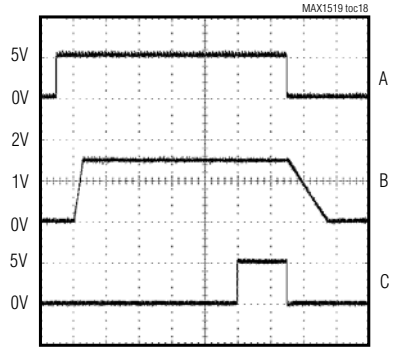
INDUCTOR CURRENT DIFFERENCE vs. LOAD CURRENT



Typical Operating Characteristics (continued)

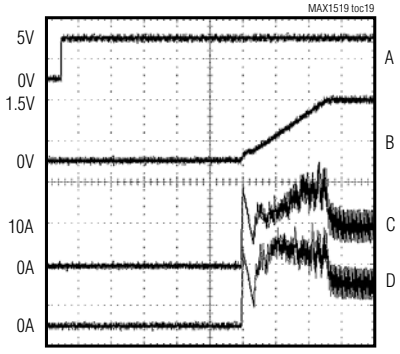
(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D4 set for 1.5V (SUS = GND), S0–S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

POWER-UP SEQUENCE



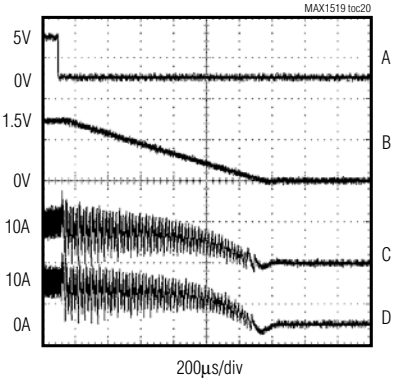
A. $\overline{SHDN}$, 5V/div
B. 1.5V OUTPUT, 1V/div
C. VROK, 5V/div
R_{TIME} = 64.9kΩ

SOFT-START



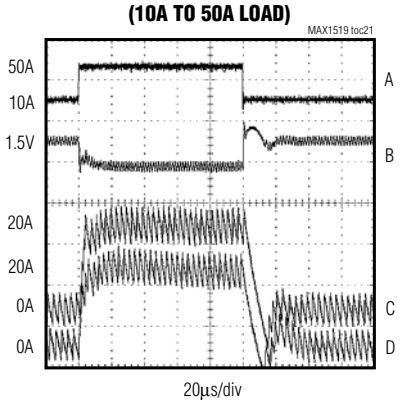
A. $\overline{SHDN}$, 5V/div
B. 1.5V OUTPUT, 1V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
R_{LOAD} = 75mΩ, R_{TIME} = 64.9kΩ

SOFT-SHUTDOWN



A. $\overline{SHDN}$, 5V/div
B. 1.5V OUTPUT, 1V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
R_{LOAD} = 75mΩ, R_{TIME} = 64.9kΩ

1.50V LOAD TRANSIENT (10A TO 50A LOAD)



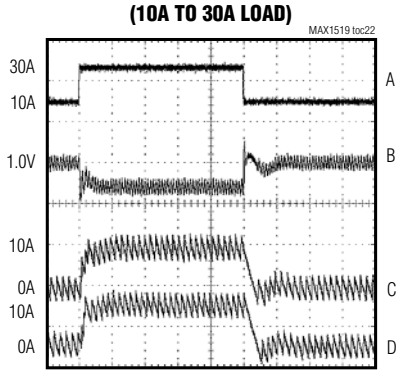
A. LOAD CURRENT, (I_{LOAD} = 10A TO 50A), 50A/div
B. OUTPUT VOLTAGE (1.5V NO LOAD), 100mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div

Dual-Phase, Quick-PWM Controllers for Programmable CPU Core Power Supplies

Typical Operating Characteristics (continued)

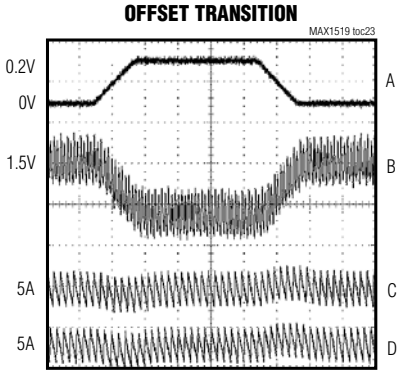
(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D4 set for 1.5V (SUS = GND), S0–S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

1.00V LOAD TRANSIENT (10A TO 30A LOAD)



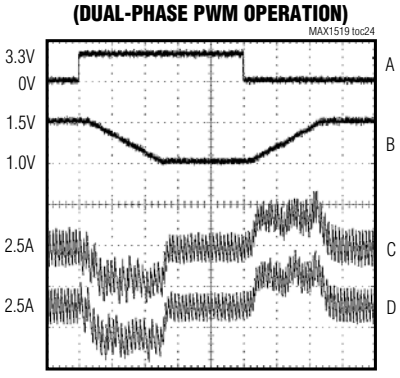
A. LOAD CURRENT, (I_{LOAD} = 10A TO 30A), 25A/div
B. OUTPUT VOLTAGE (1.00V NO LOAD), 50mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div

OFFSET TRANSITION



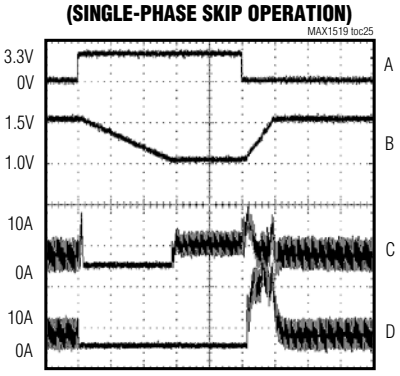
A. V_{OFS} = 0 TO 200mV, 0.2V/div
B. V_{OUT} = 1.500V TO 1.475V, 20mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
10A LOAD

SUSPEND TRANSITION (DUAL-PHASE PWM OPERATION)



A. SUS, 5V/div
B. V_{OUT} = 1.5V TO 1.0V, 0.5V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
5A LOAD, $\overline{SKIP}$ = V_{CC}, R_{TIME} = 64.9kΩ

SUSPEND TRANSITION (SINGLE-PHASE SKIP OPERATION)

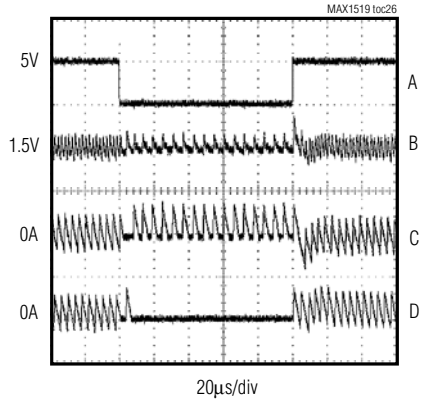


A. SUS, 5V/div
B. V_{OUT} = 1.5V TO 1.0V, 0.5V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
5A LOAD, C_{OUT} = (4) 680µF, $\overline{SKIP}$ = $\overline{SUS}$, R_{TIME} = 64.9kΩ

Typical Operating Characteristics (continued)

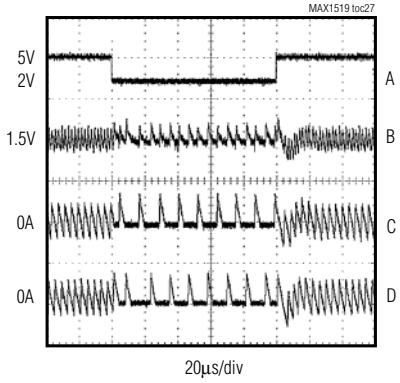
(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D4 set for 1.5V (SUS = GND), S0–S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

SINGLE-PHASE SKIP TO DUAL-PHASE PWM TRANSITION



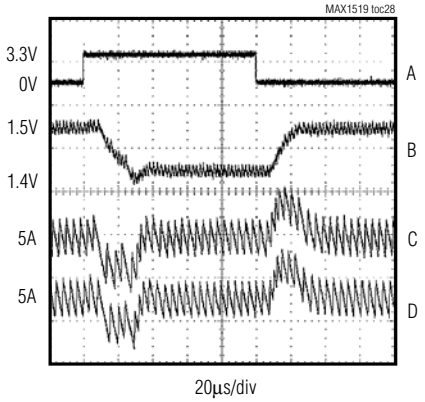
A. $\overline{SKIP}$ = V_{CC} TO GND, 5V/div
B. 1.5V OUTPUT, 50mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
2A LOAD

DUAL-PHASE SKIP TO DUAL-PHASE PWM TRANSITION



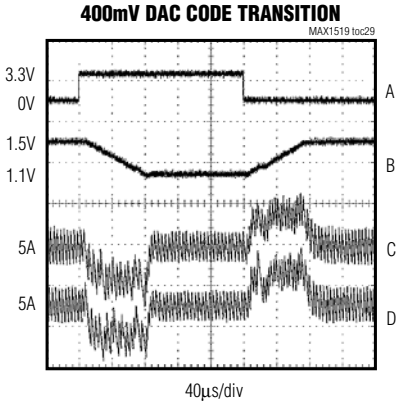
A. $\overline{SKIP}$ = V_{CC} TO REF, 5V/div
B. 1.5V OUTPUT, 50mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
2A LOAD

100mV DAC CODE TRANSITION



A. D1, 5V/div
B. V_{OUT} = 1.50V TO 1.40V, 100mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
10A LOAD

400mV DAC CODE TRANSITION



A. D3, 5V/div
B. V_{OUT} = 1.50V TO 1.10V, 0.5V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
10A LOAD

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Pin Description

PIN	NAME	FUNCTION
1	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 150kΩ to 15kΩ resistor sets the clock from 100kHz to 1MHz, f_{SLEW} = 500kHz × 30kΩ/R_{TIME}.
2	TON	On-Time Selection Control Input. This four-level input sets the K-factor value used to determine the DH_ on-time (see the *On-Time One-Shot TON* section): GND = 550kHz, REF = 300kHz, OPEN = 200kHz, V_{CC} = 100kHz.
3	SUS	Suspend Input. SUS is a three-level logic input. When the controller detects on-transition on SUS, the controller slews the output voltage to the new voltage level determined by SUS, S0–S1, and D0–D4. The controller blanks VROK during the transition and another 24 R_{TIME} clock cycles after the new DAC code is reached. Connect SUS as follows to select which multiplexer sets the nominal output voltage: 3.3V or V_{CC} (high) = suspend mode; S0–S1 low-range suspend code (Table 5), REF = suspend mode; S0–S1 high-range suspend code (Table 5), GND = normal operation; D0–D4 VID DAC code (Table 4).
4, 5	S0, S1	Suspend-Mode Voltage Select Inputs. S0–S1 are four-level digital inputs that select the suspend mode VID code (Table 5) for the suspend mode multiplexer inputs. If SUS is high, the suspend mode VID code is delivered to the DAC (see the *Internal Multiplexers* section), overriding any other voltage setting (Figure 3).
6	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA (typ) shutdown state. During the transition from normal operation to shutdown, the output voltage ramps down at 4 times the output-voltage slew rate programmed by the TIME pin. In shutdown mode, DLM and DLS are forced to V_{DD} to clamp the output to ground. Forcing $\overline{SHDN}$ to 12V ~ 15V disables both overvoltage protection and undervoltage protection circuits, disables overlap operation, and clears the fault latch. Do not connect $\overline{SHDN}$ to >15V.
7	OFS	Voltage-Divider Input for Offset Control. For 0 < V_{OFS} < 0.8V, 0.125 times the voltage at OFS is subtracted from the output. For 1.2V < V_{OFS} < 2V, 0.125 times the difference between REF and OFS is added to the output. Voltages in the range of 0.8V < V_{OFS} < 1.2V are undefined. The controller disables the offset amplifier during suspend mode (SUS = REF or high).
8	REF	2V Reference Output. Bypass to GND with a 0.22µF or greater ceramic capacitor. The reference can source 100µA for external loads. Loading REF degrades output voltage accuracy according to the REF load regulation error.
9	ILIM	Current-Limit Adjustment. The current-limit threshold defaults to 30mV if ILIM is tied to V_{CC}. In adjustable mode, the current-limit threshold voltage is precisely 1/20 the voltage seen at ILIM over a 0.2V to 1.5V range. The logic threshold for switchover to the 30mV default value is approximately V_{CC} - 1V.
10	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) with a series 10Ω resistor. Bypass to GND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
11	GND	Analog Ground. Connect the MAX1519/MAX1545's exposed pad to analog ground.
12	CCV	Voltage Integrator Capacitor Connection. Connect a 47pF to 1000pF (47pF, typ) capacitor from CCV to analog ground (GND) to set the integration time constant.

Pin Description (continued)

PIN	NAME	FUNCTION
13	GNDS	Ground Remote-Sense Input. Connect GNDS directly to the CPU ground-sense pin. GNDS internally connects to an amplifier that adjusts the output voltage, compensating for voltage drops from the regulator ground to the load ground.
14	CCI	Current-Balance Compensation. Connect a 470pF capacitor between CCI and FB (see the *Current-Balance Compensation (CCI)* section).
15	FB	Feedback Input. FB is internally connected to both the feedback input and the output of the voltage-positioning op amp. See the *Setting Voltage Positioning* section to set the voltage-positioning gain.
16	OAIN-	Op Amp Inverting Input and Op Amp Disable Input. When using the internal op amp for additional voltage-positioning gain, connect to the negative terminal of the current-sense resistor through a resistor as described in the *Setting Voltage Positioning* section. Connect OAIN- to V_{CC} to disable the op amp. The logic threshold to disable the op amp is approximately V_{CC} - 1V.
17	OAIN+	Op Amp Noninverting Input. When using the internal op amp for additional voltage-positioning gain, connect to the positive terminal of the current-sense resistor through a resistor as described in the *Setting Voltage Positioning* section.
18	$\overline{SKIP}$	Pulse-Skipping Select Input. When pulse skipping, the controller blanks the VROK upper threshold: 3.3V or V_{CC} (high) = Dual-phase forced-PWM operation, REF = Dual-phase pulse-skipping operation, GND = Single-phase pulse-skipping operation.
19	CODE	VID DAC Code Selection Output. Connect CODE to GND to select the desktop P4 code set, or connect CODE to V_{CC} to select the mobile P4 code set (Table 4).
20–24	D4–D0	Low-Voltage VID DAC Code Inputs. The D0–D4 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. In normal mode (Table 4, SUS = GND), the output voltage is set by the VID code indicated by the logic-level voltages on D0–D4. In suspend mode (Table 5, SUS = REF or high), the decoded state of the four-level S0–S1 inputs sets the output voltage.
25	VROK	Open-Drain Power-Good Output. After output voltage transitions, except during power-up and power-down, if OUT is in regulation, then VROK is high impedance. The controller blanks VROK whenever the slew-rate control is active (output voltage transitions). VROK is forced low in shutdown. A pullup resistor on VROK causes additional finite shutdown current. During power-up, VROK includes a 3ms (min) delay after the output reaches the regulation voltage.
26	BSTM	Main Boost Flying Capacitor Connection. An optional resistor in series with BSTM allows the DHM pullup current to be adjusted.
27	LXM	Main Inductor Connection. LXM is the internal lower supply rail for the DHM high-side gate driver.
28	DHM	Main High-Side Gate-Driver Output. Swings LXM to BSTM.
29	DLM	Main Low-Side Gate-Driver Output. DLM swings from PGND to V_{DD}. DLM is forced high after the MAX1519/MAX1545 power down.
30	V_{DD}	Supply Voltage Input for the DLM and DLS Gate Drivers. Connect to the system supply voltage (4.5V to 5.5V). Bypass V_{DD} to PGND with a 2.2µF or greater ceramic capacitor as close to the IC as possible.

Dual-Phase, Quick-PWM Controllers for Programmable CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
31	PGND	Power Ground. Ground connection for low-side gate drivers DLM and DLS.
32	DLS	Secondary Low-Side Gate-Driver Output. DLS swings from PGND to V_{DD}. DLS is forced high after the MAX1519/MAX1545 power down.
33	DHS	Secondary High-Side Gate-Driver Output. Swings LXS to BSTS.
34	LXS	Secondary Inductor Connection. LXS is the internal lower supply rail for the DHS high-side gate driver.
35	BSTS	Secondary Boost Flying Capacitor Connection. An optional resistor in series with BSTS allows the DHS pullup current to be adjusted.
36	V+	Battery Voltage-Sense Connection. Used only for PWM one-shot timing. DH_ on-time is inversely proportional to input voltage over a range of 4V to 28V.
37	CMP	Main Inductor Positive Current-Sense Input
38	CMN	Main Inductor Negative Current-Sense Input
39	CSN	Secondary Inductor Positive Current-Sense Input
40	CSP	Secondary Inductor Negative Current-Sense Input

Detailed Description

Dual 180° Out-of-Phase Operation

The two phases in the MAX1519/MAX1545 operate 180° out-of-phase ($\overline{SKIP}$ = REF or high) to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX1519/MAX1545 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide transfer power using only one phase instead of dividing the power among several phases. In these applications, the input capacitors must support high instantaneous current requirements. The high-RMS ripple current can lower efficiency due to I^2R power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input voltage ripple, reduce ESR-related power losses, and to meet the necessary RMS ripple current rating.

With the MAX1519/MAX1545, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively cut in half, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). As a result, the same performance can be achieved with fewer or less expensive input capacitors.

Transient Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. In order to provide fast transient response, the MAX1519/MAX1545 support a phase-overlap mode, which allows the dual regulators to operate in-phase when heavy load transients are detected, reducing the response time. After either high-side MOSFET turns off and if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on both high-side MOSFETs during the next on-time cycle. This maximizes the total inductor-current slew rate. The phases remain overlapped until the output voltage exceeds the regulation voltage and after the minimum off-time expires.

After the phase-overlap mode ends, the controller automatically begins with the opposite phase. For example, if the secondary phase provided the last on-time pulse before overlap operation began, the controller starts switching with the main phase when overlap operation ends.

Table 1. Component Selection for Standard Multiphase Applications*

DESIGNATION	MAX1519/MAX1545 2-PHASE DESKTOP P4	MAX1519/MAX1545 4- PHASE DESKTOP P4
	Circuit of Figure 1	Circuit of Figure 12
Input Voltage Range	7V to 24V	7V to 24V
VID Output Voltage (D4–D0)	1.5V (CODE = GND, D4–D0 = 01110)	1.5V (CODE = GND, D4–D0 = 01110)
Suspend Voltage (SUS, S0–S1)	Not Used (SUS = GND)	Not Used (SUS = GND)
Maximum Load Current	60A	60A
Number of Phases (η_{TOTAL})	Two phases (1) MAX1519/MAX1545	Four phases (1) MAX1519/MAX1545 + (2) MAX1980
Inductor (per phase)	0.6µH Panasonic ETQP1H0R6BFA	0.7µH Panasonic ETQP2H0R7BFA or 0.8µH Sumida CDEP105L-0R8
Switching Frequency	300kHz (TON = REF)	300kHz (TON = REF)
High-Side MOSFET (N_H, per phase)	Siliconix (1) Si7886DP International Rectifier (2) IRF6604	International Rectifier (1) IRF7811W or Fairchild (1) FDS6694
Low-Side MOSFET (N_L, per phase)	Siliconix (2) Si7442DP or International Rectifier (2) IRF6603	Fairchild (2) FDS6688 or Siliconix (1) Si7442DP
Total Input Capacitance (C_{IN})	(6) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M	(6) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Total Output Capacitance (C_{OUT})	(4) 680µF, 2.5V Sanyo 2R5TPD680M	(4) 680µF, 2.5V Sanyo 2R5TPD680M
Current-Sense Resistor (R_{SENSE}, per phase)	1.0mΩ Panasonic ERJM1WTJ1M0U	1.5mΩ Panasonic ERJM1WTJ1M5U

**Contact Intel for the Mobile P4 specifications and contact Maxim for a reference schematic.*

Power-Up Sequence

The MAX1519/MAX1545 are enabled when $\overline{SHDN}$ is driven high (Figure 2). The reference powers up first. Once the reference exceeds its undervoltage lockout threshold, the PWM controller evaluates the DAC target and starts switching.

For the MAX1519/MAX1545, the slew-rate controller ramps up the output voltage in 25mV increments to the proper operating voltage (see Tables 3 and 4) set by either D0–D4 (SUS = GND) or S0–S1 (SUS = REF or high). The ramp rate is set with the R_{TIME} resistor (see the *Output Voltage Transition Timing* section). The controller pulls VROK low until at least 3ms after the MAX1519/MAX1545 reach the target DAC code.

Shutdown

When $\overline{SHDN}$ goes low, the MAX1519/MAX1545 enter low-power shutdown mode. VROK is pulled low immediately, and the output voltage ramps down to 0V in 25mV increments at 4 times the clock rate set by R_{TIME}:

$$t_{SHDN} \le \frac{4}{f_{SLEW}} \left(\frac{V_{DAC}}{V_{LSB}} \right)$$

Dual-Phase, Quick-PWM Controllers for Programmable CPU Core Power Supplies

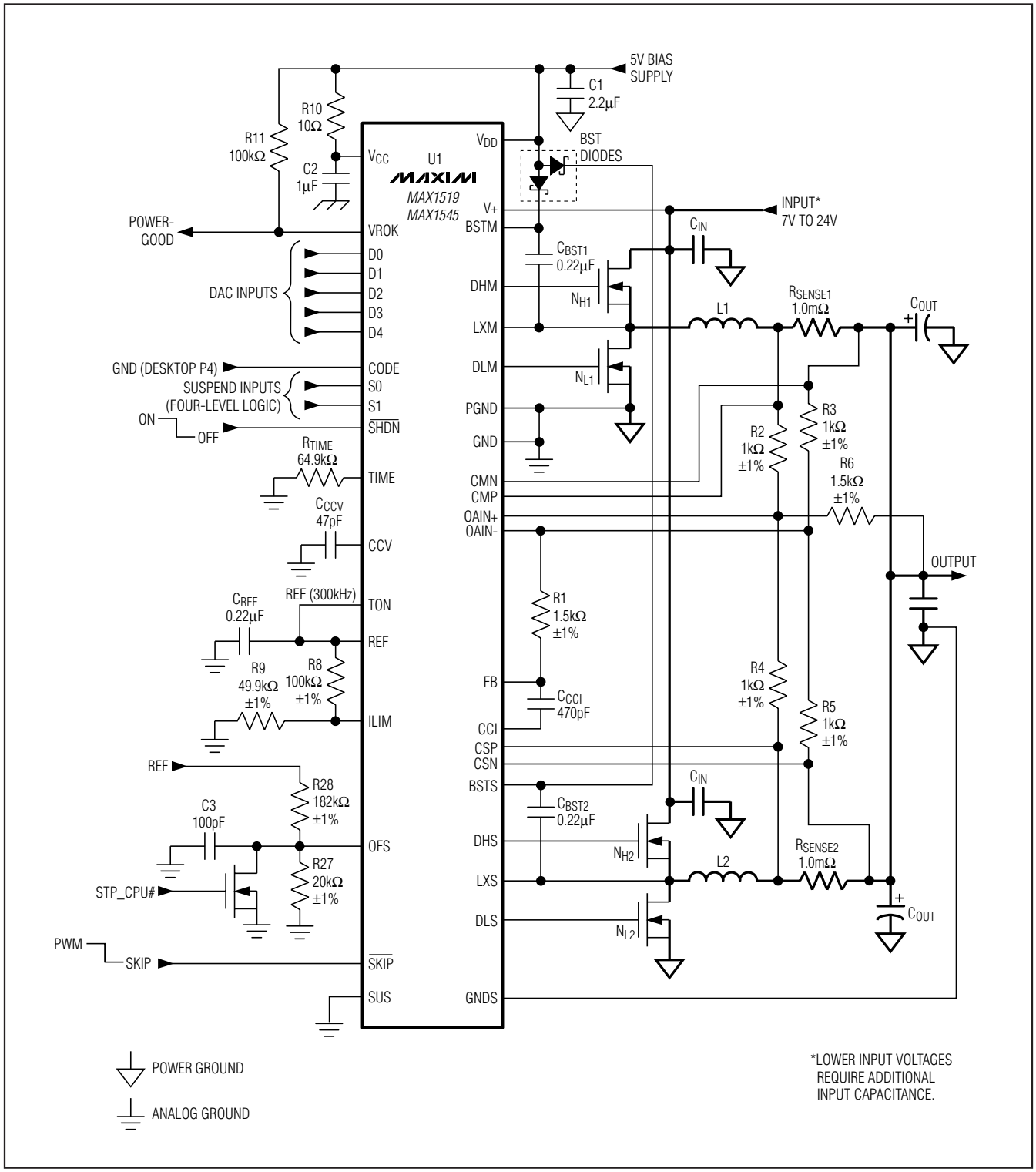

Figure 1. Standard Two-Phase Desktop P4 Application Circuit

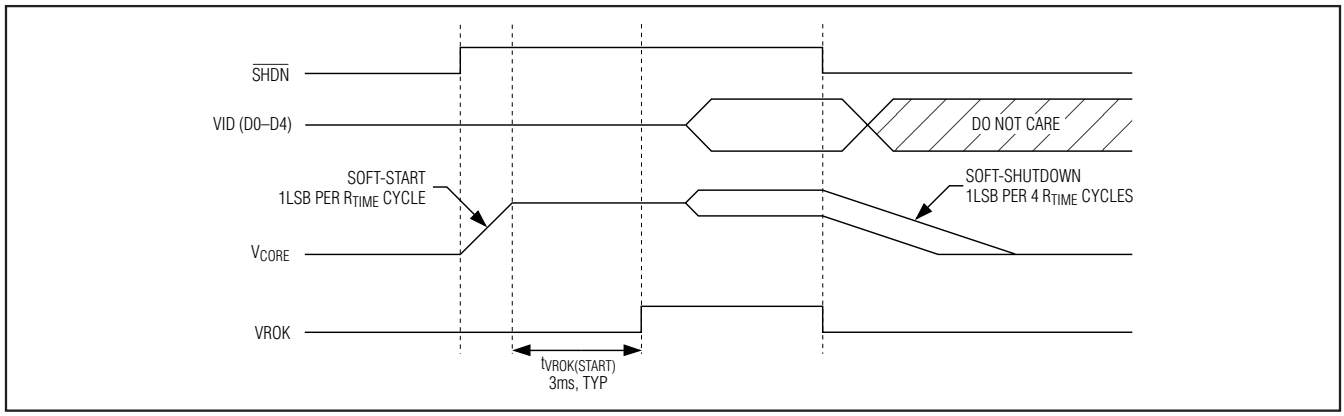

Figure 2. Power-Up and Shutdown Sequence Timing Diagram

Table 2. Component Suppliers

MANUFACTURER	PHONE	WEBSITE
BI Technologies	714-447-2345 (USA)	www.bitechnologies.com
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	561-752-5000 (USA)	www.coiltronics.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	847-468-5624 (USA)	www.panasonic.com
Sanyo	65-6281-3226 (Singapore)	www.secc.co.jp
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	03-3667-3408 (Japan) 408-573-4150 (USA)	www.t-yuden.com
TDK	847-803-6100 (USA) 81-3-5201-7241 (Japan)	www.component.tdk.com
TOKO	858-675-8013 (USA)	www.tokoam.com

where f_{SLEW} = 500kHz × 30kΩ/R_{TIME}, V_{DAC} is the DAC setting when the controller begins the shutdown sequence, and V_{LSB} = 25mV is the DAC's smallest voltage increment. Slowly discharging the output capacitors by slewing the output over a long period of time (4/f_{SLEW}) keeps the average negative inductor current low (damped response), thereby eliminating the negative output voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response).

This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output voltage excursion. When the DAC reaches the 0V setting, DL_ goes high, DH_ goes low, the reference turns off, and the supply current drops to about 1µA. When a fault condition—output undervoltage lockout, output overvoltage lockout (MAX1545), or thermal shutdown—activates the shutdown sequence, the controller sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V.

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Table 3. Operating Mode Truth Table

$\overline{SHDN}$	SUS	$\overline{SKIP}$	OFS	OUTPUT VOLTAGE	OPERATING MODE
GND	x	x	x	GND	Low-Power Shutdown Mode. DL_ is forced high, DH_ is forced low, and the PWM controller is disabled. The supply current drops to 1µA (typ).
V_{CC}	GND	V_{CC}	GND or REF	D0–D4 (no offset)	Normal Operation. The no-load output voltage is determined by the selected VID DAC code (CODE and D0–D4, Table 4).
V_{CC}	x	REF or GND	GND or REF	D0–D4 (no offset)	Pulse-Skipping Operation. When $\overline{SKIP}$ is pulled low, the MAX1519/MAX1545 immediately enter pulse-skipping operation, allowing automatic PWM/PFM switchover under light loads. The VROK upper threshold is blanked.
V_{CC}	GND	x	0 to 0.8V or 1.2V to 2V	D0–D4 (plus offset)	Deep-Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (CODE and D0–D4, Table 4), plus the offset voltage set by OFS.
V_{CC}	REF or high	x	x	SUS, S0–S1 (no offset)	Suspend Mode. The no-load output voltage is determined by the selected suspend code (SUS, S0–S1, Table 5), overriding all other active modes of operation.
V_{CC}	x	x	x	GND	Fault Mode. The fault latch has been set by either UVP, OVP (MAX1545 only), or thermal shutdown. The controller remains in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

When $\overline{SHDN}$ goes high, the reference powers up. Once the reference voltage exceeds its UVLO threshold, the controller evaluates the DAC target and starts switching. The slew-rate controller ramps up from 0V in 25mV increments to the currently selected output-voltage setting (see the *Power-Up Sequence* section). There is no traditional soft-start (variable current-limit) circuitry, so full output current is available immediately.

Internal Multiplexers

The MAX1519/MAX1545 have a unique internal DAC input multiplexer (muxes) that selects one of three different DAC code settings for different processor states (Figure 3). On startup, the MAX1519/MAX1545 select the DAC code from the D0–D4 (SUS = GND) or S0–S1 (SUS = REF or high) input decoders.

DAC Inputs (CODE, D0–D4)

During normal forced-PWM operation (SUS = GND), the DAC programs the output voltage using code and the D0–D4 inputs. Connect CODE to V_{CC} or GND for the mobile or desktop P4 setting, respectively. Do not leave D0–D4 unconnected. D0–D4 can be changed while the MAX1519/MAX1545 are active, initiating a transition to a new output voltage level. Change D0–D4 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings can cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with desktop and mobile P4 (Table 4) specifications.

Four-Level Logic Inputs

TON and S0–S1 are four-level logic inputs. These inputs help expand the functionality of the controller without adding an excessive number of pins. The four-level inputs are intended to be static inputs. When left open, an internal resistive voltage-divider sets the input voltage to approximately 3.5V. Therefore, connect the four-level logic inputs directly to V_{CC}, REF, or GND when selecting one of the other logic levels. See *Electrical Characteristics* for exact logic level voltages.

Suspend Mode

When the processor enters low-power suspend mode, it sets the regulator to a lower output voltage to reduce power consumption. The MAX1519/MAX1545 include

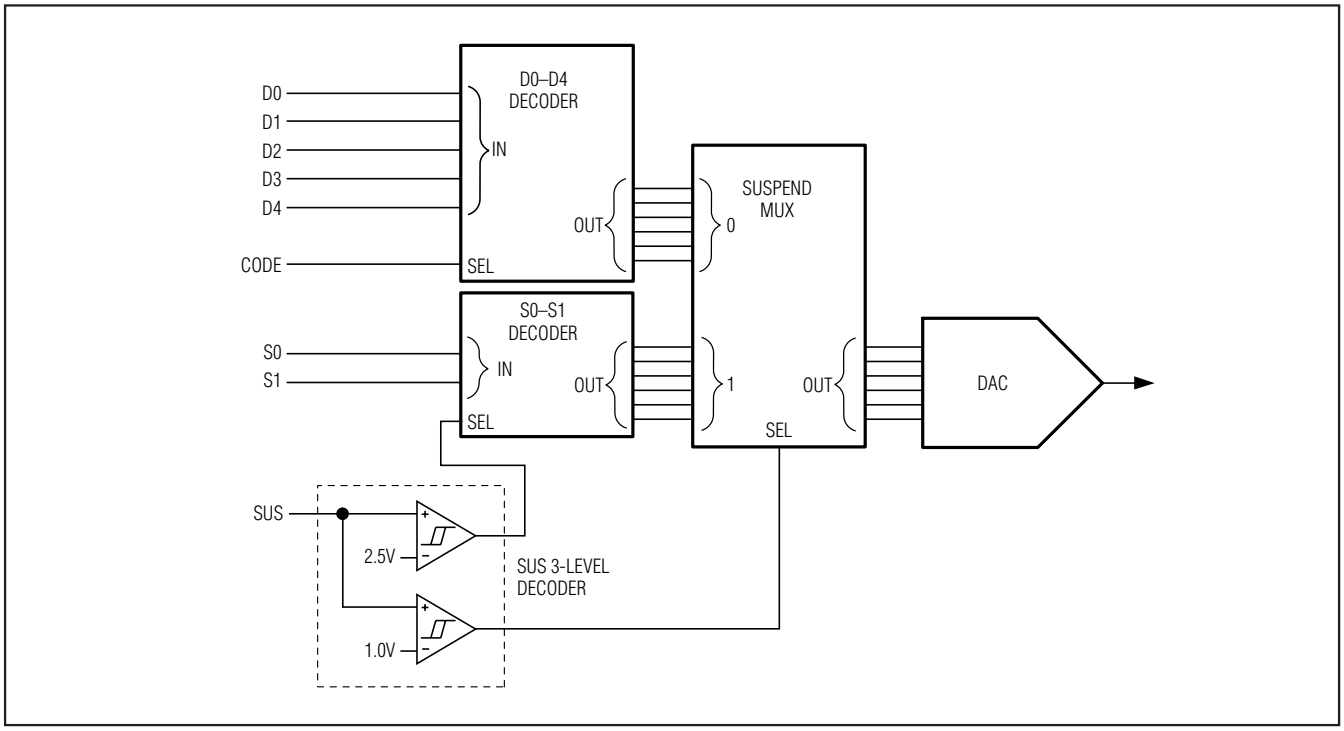

Figure 3. Internal Multiplexers Functional Diagram

independent suspend-mode output voltage codes set by the four-level S0–S1 inputs and the three-level SUS input. When the CPU suspends operation (SUS = REF or high), the controller disables the offset amplifier and overrides the 5-bit VID DAC code set by D0–D4 (normal operation). The master controller slews the output to the selected suspend-mode voltage. During the transition, the MAX1519/MAX1545 blank VROK and the UVP fault protection until 24 R_{TIME} clock cycles after the slew-rate controller reaches the suspend-mode voltage.

SUS is a three-level logic input: GND, REF, or high. This expands the functionality of the controller without adding an additional pin. This input is intended to be driven by a dedicated open-drain output with the pullup resistor connected either to REF (or a resistive-divider from V_{CC}) or to a logic-level bias supply (3.3V or greater). When pulled up to REF, the MAX1519/MAX1545 select the upper suspend voltage range. When pulled high (2.7V or greater), the controller selects the lower suspend voltage range. See *Electrical Characteristics* for exact logic level voltages.

Output Voltage Transition Timing

The MAX1519/MAX1545 are designed to perform mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance.

At the beginning of an output voltage transition, the MAX1519/MAX1545 blank the VROK output, preventing them from changing states. VROK remains blanked during the transition and is enabled 24 clock cycles after the slew-rate controller has set the final DAC code value. The slew-rate clock frequency (set by resistor R_{TIME}) must be set fast enough to ensure that the transition is completed within the maximum allotted time.

The slew-rate controller transitions the output voltage in 25mV steps during soft-start, soft-shutdown, and suspend-mode transitions. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX1519/MAX1545s' slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX1519/MAX1545 automatically control the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less

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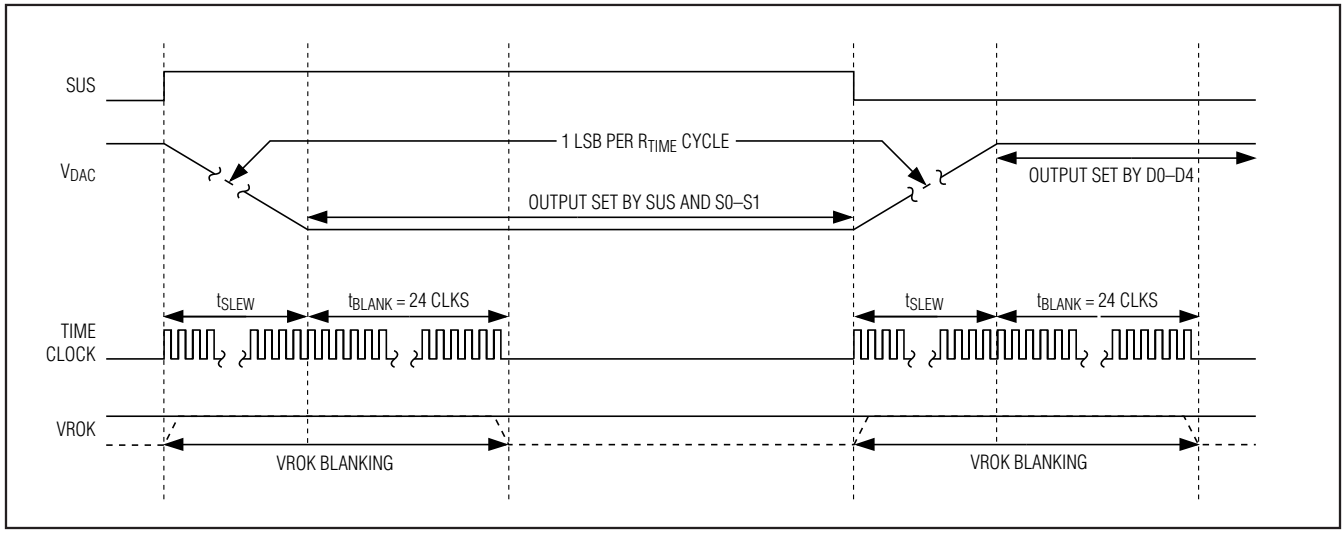

Figure 4. Suspend Transition

than the current limit set by ILIM. The transition time is given by:

$$t_{SLEW} \approx \frac{1}{f_{SLEW}}\left(\frac{V_{OLD} - V_{NEW}}{V_{LSB}}\right) \text{ for } V_{OUT} \text{ rising}$$

$$t_{SLEW} \approx \frac{1}{f_{SLEW}}\left[\left(\frac{V_{OLD} - V_{NEW}}{V_{LSB}}\right) + 2\right] \text{ for } V_{OUT} \text{ falling}$$

where f_{SLEW} = 500kHz x 30kΩ / R_{TIME}, V_{OLD} is the original DAC setting, V_{NEW} is the new DAC setting, and V_{LSB} is the DAC's smallest voltage increment. The additional two clock cycles on the falling edge time are due to internal synchronization delays. See TIME Frequency Accuracy in the *Electrical Characteristics* for f_{SLEW} limits.

The practical range of R_{TIME} is 15kΩ to 150kΩ corresponding to 1.0µs to 10µs per 25mV step. Although the DAC takes discrete steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times V_{LSB} \times f_{SLEW}$$

Fault Protection

Output Overvoltage Protection (MAX1545 Only)

The overvoltage protection (OVP) circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX1519/MAX1545 continuously monitor the output for an overvoltage fault. During normal forced-PWM operation ($\overline{SKIP}$ = high), the controller detects an OVP fault if the output voltage exceeds the set DAC voltage by more than 13% (min). During pulse-skipping operation ($\overline{SKIP}$ = REF or GND), the controller detects an OVP fault if the output voltage exceeds the fixed 2V (typ) threshold. When the OVP circuit detects an overvoltage fault, it immediately sets the fault latch, pulls VROK low, and activates the shutdown sequence.

This action discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 1V.

Overvoltage protection can be disabled through the "no-fault" test mode (see the *No-Fault Test Mode* section).

Output Undervoltage Shutdown

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX1519/MAX1545 output voltage is under 70% of the nominal value, the controller activates the shutdown sequence and sets the fault latch.

Once the controller ramps down to the 0V DAC code setting, it forces the DL_ low-side gate-driver high, and pulls the DH_ high-side gate-driver low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller. UVP is ignored during output voltage transitions and remains blanked

Table 4. Output Voltage VID DAC Codes (SUS = GND)

CODE = V_{CC}					
D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	1.750
0	0	0	0	1	1.700
0	0	0	1	0	1.650
0	0	0	1	1	1.600
0	0	1	0	0	1.550
0	0	1	0	1	1.500
0	0	1	1	0	1.450
0	0	1	1	1	1.400
0	1	0	0	0	1.350
0	1	0	0	1	1.300
0	1	0	1	0	1.250
0	1	0	1	1	1.200
0	1	1	0	0	1.150
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.900
1	0	1	0	0	0.875
1	0	1	0	1	0.850
1	0	1	1	0	0.825
1	0	1	1	1	0.800
1	1	0	0	0	0.775
1	1	0	0	1	0.750
1	1	0	1	0	0.725
1	1	0	1	1	0.700
1	1	1	0	0	0.675
1	1	1	0	1	0.650
1	1	1	1	0	0.625
1	1	1	1	1	0.600

CODE = GND					
D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500
0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	0	1	1.125
1	1	1	1	0	1.100
1	1	1	1	1	Shutdown

for an additional 24 clock cycles after the controller reaches the final DAC code value.

UVP can be disabled through the "no-fault" test mode (see the *No-Fault Test Mode* section).

Thermal-Fault Protection

The MAX1519/MAX1545 feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch and activates the soft-shutdown sequence. Once the con-

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Table 5. Suspend Mode DAC Codes

LOWER SUSPEND CODES			
SUS*	S1	S0	OUTPUT VOLTAGE (V)
High	GND	GND	0.675
High	GND	REF	0.700
High	GND	OPEN	0.725
High	GND	V_{CC}	0.750
High	REF	GND	0.775
High	REF	REF	0.800
High	REF	OPEN	0.825
High	REF	V_{CC}	0.850
High	OPEN	GND	0.875
High	OPEN	REF	0.900
High	OPEN	OPEN	0.925
High	OPEN	V_{CC}	0.950
High	V_{CC}	GND	0.975
High	V_{CC}	REF	1.000
High	V_{CC}	OPEN	1.025
High	V_{CC}	V_{CC}	1.050

UPPER SUSPEND CODES			
SUS*	S1	S0	OUTPUT VOLTAGE (V)
REF	GND	GND	1.075
REF	GND	REF	1.100
REF	GND	OPEN	1.125
REF	GND	V_{CC}	1.150
REF	REF	GND	1.175
REF	REF	REF	1.200
REF	REF	OPEN	1.225
REF	REF	V_{CC}	1.250
REF	OPEN	GND	1.275
REF	OPEN	REF	1.300
REF	OPEN	OPEN	1.325
REF	OPEN	V_{CC}	1.350
REF	V_{CC}	GND	1.375
REF	V_{CC}	REF	1.400
REF	V_{CC}	OPEN	1.425
REF	V_{CC}	V_{CC}	1.450

**Connect the three-level SUS input to a 2.7V or greater supply (3.3V or V_{CC}) for an input logic level high.*

troller ramps down to the 0V DAC code setting, it forces the DL_ low-side gate-driver high, and pulls the DH_ high-side gate-driver low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Thermal shutdown can be disabled through the "no-fault" test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The latched-fault protection features and overlap mode can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a "no-fault" test mode is provided to disable the fault protection (overvoltage protection, undervoltage protection, and thermal shutdown) and overlap mode. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 12V to 15V on $\overline{SHDN}$.

Multiphase Quick-PWM

5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V bias supply can be generated with an external linear regulator.

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G(LOW)} + Q_{G(HIGH)})$$

where I_{CC} is provided in the *Electrical Characteristics*, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V. V+ and V_{DD} can be tied together if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Free-Running, Constant On-Time PWM Controller with Input Feed Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator

with input voltage feed forward (Figure 5). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to the input voltage, and directly proportional to the output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot (TON)* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 180° out-of-phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output voltage set point.

On-Time One-Shot (TON)

The core of each phase contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFETs on-time. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{K(V_{FB} + 0.075V)}{V_{IN}}$$

where K is set by the TON pin-strap connection (Table 6) and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

The one-shot for the secondary phase varies the on-time in response to the input voltage and the difference between the main and secondary inductor currents. Two identical transconductance amplifiers integrate the difference between the master and slave current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network connected between CCI and FB.

The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_M (V_{CMP} - V_{CMN}) - G_M (V_{CSP} - V_{CSN})$$

$$V_{CCI} = V_{FB} + I_{CCI} Z_{CCI}$$

Table 6. Approximate K-Factor Errors

TON CONNECTION	FREQUENCY SETTING (kHz)	K-FACTOR (µs)	MAX K-FACTOR ERROR (%)
V_{CC}	100	10	±10
Float	200	5	±10
REF	300	3.3	±10
GND	550	1.8	±12.5

where Z_{CCI} is the impedance at the CCI output. The secondary on-time one-shot uses this integrated signal (V_{CCI}) to set the secondary high-side MOSFETs on-time. When the main and secondary current-sense signals ($V_{CM} = V_{CMP} - V_{CMN}$ and $V_{CS} = V_{CSP} - V_{CSM}$) become unbalanced, the transconductance amplifiers adjust the secondary on-time, which increases or decreases the secondary inductor current until the current-sense signals are properly balanced:

$$t_{ON(2ND)} = K \left(\frac{V_{CCI} + 0.075V}{V_{IN}} \right)$$

$$= K \left(\frac{V_{FB} + 0.075V}{V_{IN}} \right) + K \left(\frac{I_{CCI} Z_{CCI}}{V_{IN}} \right)$$

$$= (\text{Main On-Time}) + (\text{Secondary Current Balance Correction})$$

This algorithm results in a nearly constant switching frequency and balanced inductor currents, despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics*. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* can vary over a wider range. For example, the 300kHz setting typically runs about 3% slower with inputs much greater than 12V due to the very short on-times required.

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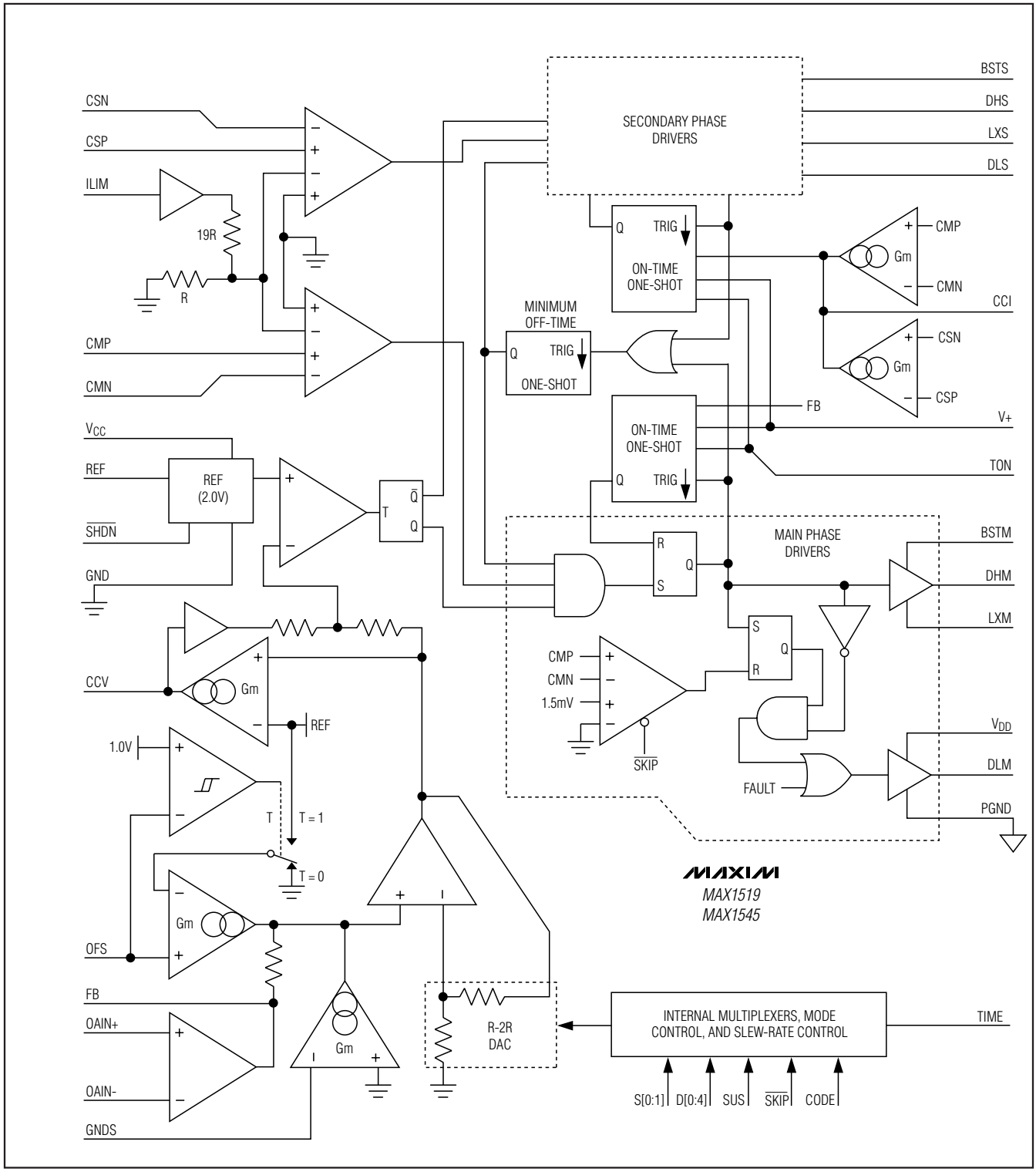

Figure 5. Dual-Phase Quick-PWM Functional Diagram

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time.

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON}\,(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time as determined above.

Current Balance

Without active current-balance circuitry, the current matching between phases depends on the MOSFET's on-resistance ($R_{DS(ON)}$), thermal ballasting, on-/off-time matching, and inductance matching. For example, variation in the low-side MOSFET on-resistance (ignoring thermal effects) results in a current mismatch that is proportional to the on-resistance difference:

$$I_{MAIN} - I_{2ND} = I_{MAIN}\left[1 - \left(\frac{R_{MAIN}}{R_{2ND}}\right)\right]$$

However, mismatches between on-times, off-times, and inductor values increase the worst-case current imbalance, making it impossible to passively guarantee accurate current balancing.

The multiphase Quick-PWM controller integrates the difference between the current-sense voltages and adjusts the on-time of the secondary phase to maintain current balance. The current balance now relies on the accuracy of the current-sense resistors instead of the inaccurate, thermally sensitive on-resistance of the low-side MOSFETs.

With active current balancing, the current mismatch is determined by the current-sense resistor values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LM} - I_{LS} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics*.

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different di/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier

The multiphase Quick-PWM controllers include an independent operational amplifier for adding gain to the voltage-positioning sense path. The voltage-positioning gain allows the use of low-value current-sense resistors in order to minimize power dissipation. This 3MHz gain-bandwidth amplifier was designed with low offset voltage (70µV, typ) to meet the IMVP output accuracy requirements.

The inverting (OAIN-) and noninverting (OAIN+) inputs are used to differentially sense the voltage across the voltage-positioning sense resistor. The op amp's output is internally connected to the regulator's feedback input (FB). The op amp should be configured as a noninverting, differential amplifier, as shown in Figure 10. The voltage-positioning slope is set by properly selecting the feedback resistor connected from FB to OAIN- (see the *Setting Voltage Positioning* section). For applications using a slave controller, additional differential input resistors (summing configuration) can be connected to the slave's voltage-positioning sense resistor. Summing together both the master and slave current-sense signals ensures that the voltage-positioning slope remains constant when the slave controller is disabled.

The controller also uses the amplifier for remote output sensing (FBS) by summing the remote-sense voltage into the positive terminal of the voltage-positioning amplifier (Figure 10).

In applications that do not require voltage-positioning gain, the amplifier can be disabled by connecting the OAIN- pin directly to V_{CC}. The disabled amplifier's output becomes high impedance, guaranteeing that the unused amplifier does not corrupt the FB input signal. The logic threshold to disable the op amp is approximately V_{CC} - 1V.

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Table 7. $\overline{SKIP}$ Settings*

$\overline{SKIP}$ CONNECTION	MODE	OPERATION
High (3.3V or V_{CC})	Two-phase forced-PWM	The controller operates with a constant switching frequency, providing low-noise forced-PWM operation. The controller disables the zero-crossing comparators, forcing the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform.
REF	Two-phase pulse skipping	The controller automatically switches over to PFM operation under light loads. The controller keeps both phases active and uses the automatic pulse-skipping control scheme—alternating between the primary and secondary phases with each cycle.
GND	One-phase pulse skipping	The controller automatically switches over to PFM operation under light loads. Only the main phase is active. The secondary phase is disabled—DHS and DLS are pulled low so LXS is high impedance.

**Settings for a dual 180° out-of-phase controller.*

Integrator Amplifier

A feedback amplifier forces the DC average of the feedback voltage to equal the VID DAC setting. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 5), allowing accurate DC output voltage regulation regardless of the output ripple voltage. The feedback amplifier has the ability to shift the output voltage. The differential input voltage range is at least ±80mV total, including DC offset and AC ripple. The integration time constant can be set easily with an external compensation capacitor at the CCV pin. Use a capacitor value of 47pF to 1000pF (47pF, typ).

Differential Remote Sense

The multiphase Quick-PWM controllers include differential remote-sense inputs to eliminate the effects of voltage drops down the PC board traces and through the processor's power pins. The remote output sense (FBS) is accomplished by summing the remote-sense voltage into the positive terminal of the voltage-positioning amplifier (Figure 10). The controller includes a dedicated input and internal amplifier for the remote ground sense. The GNDS amplifier adds an offset directly to the feedback voltage, adjusting the output voltage to counteract the voltage drop in the ground path. Together, the feedback sense resistor (R_{FBS}) and GNDS input sum the remote-sense voltages with the feedback signals that set the voltage-positioned output, enabling true differential remote sense of the processor voltage. Connect the feedback sense resistor (R_{FBS}) and ground-sense input (GNDS) directly to the processor's core supply remote-sense outputs as shown in the *Standard Applications Circuit*.

Offset Amplifier

The multiphase Quick-PWM controllers include a third amplifier used to add small offsets to the voltage-positioned load line. The offset amplifier is summed directly with the feedback voltage, making the offset gain independent of the DAC code. This amplifier has the ability to offset the output by ±100mV.

The offset is adjusted using resistive voltage-dividers at the OFS input. For inputs from 0 to 0.8V, the offset amplifier adds a negative offset to the output that is equal to 1/8 the voltage appearing at the selected OFS input ($V_{OUT} = V_{DAC} - 0.125 \times V_{OFS}$). For inputs from 1.2V to 2V, the offset amplifier adds a positive offset to the output that is equal to 1/8 the difference between the reference voltage and the voltage appearing at the selected OFS input ($V_{OUT} = V_{DAC} + 0.125 \times (V_{REF} - V_{OFS})$). With this scheme, the controller supports both positive and negative offsets with a single input. The piecewise linear transfer function is shown in the *Typical Operating Characteristics*. The regions of the transfer function below zero, above 2V, and between 0.8V and 1.2V are undefined. OFS inputs are disallowed in these regions, and the respective effects on the output are not specified.

The controller disables the offset amplifier during suspend mode (SUS = REF or high).

Forced-PWM Operation (Normal Mode)

During normal mode, when the CPU is actively running ($\overline{SKIP}$ = high, Table 7), the Quick-PWM controller operates with the low-noise forced-PWM control scheme. Forced-PWM operation disables the zero-crossing comparator, forcing the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform. This keeps the switching frequency fairly constant and allows the inductor current to

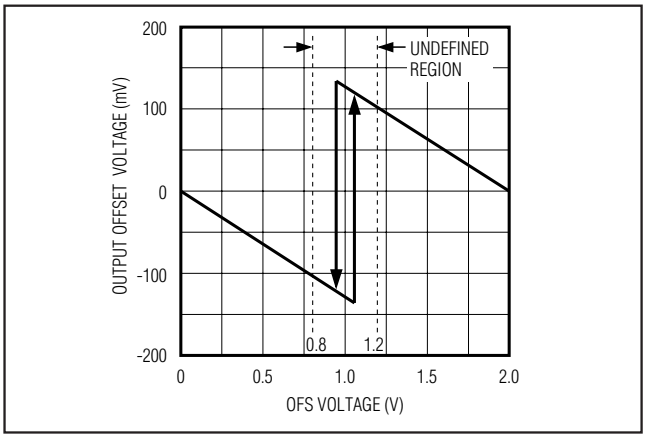

Figure 6. Offset Voltage

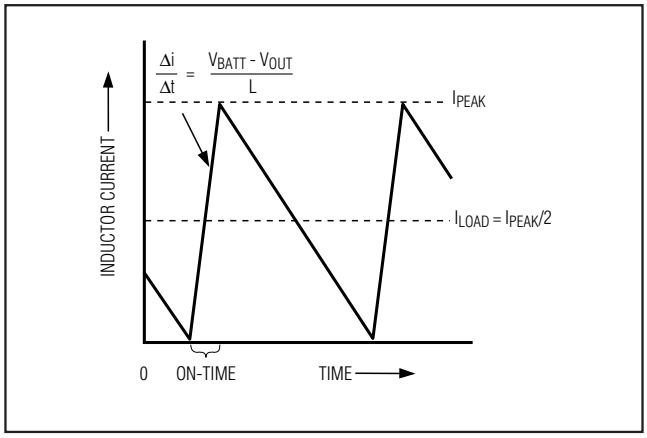

Figure 7. Pulse-Skipping/Discontinuous Crossover Point

reverse under light loads, providing fast, accurate negative output voltage transitions by quickly discharging the output capacitors.

Forced-PWM operation comes at a cost: the no-load 5V bias supply current remains between 10mA to 60mA per phase, depending on the external MOSFETs and switching frequency. To maintain high efficiency under light load conditions, the processor may switch the controller to a low-power pulse-skipping control scheme after entering suspend mode.

Low-Power Pulse Skipping

During pulse-skipping override mode ($\overline{SKIP}$ = REF or GND, Table 7), the multiphase Quick-PWM controllers use an automatic pulse-skipping control scheme. When $\overline{SKIP}$ is pulled low, the controller uses the automatic pulse-skipping control scheme, overriding forced-PWM operation, and blanks the upper VROK threshold.

$\overline{SKIP}$ is a three-level logic input—GND, REF, or high. This input is intended to be driven by a dedicated open-drain output with the pullup resistor connected either to REF (or a resistive divider from V_{CC}) or to a logic-level high bias supply (3.3V or greater).

When driven to GND, the multiphase Quick-PWM controller disables the secondary phase (DLS = PGND and DHS = LXS) and the primary phase uses the automatic pulse-skipping control scheme. When pulled up to REF, the controller keeps both phases active and uses the automatic pulse-skipping control scheme—alternating between the primary and secondary phases with each cycle.

Automatic Pulse-Skipping Switchover

In skip mode ($\overline{SKIP}$ = REF or GND), an inherent automatic switchover to PFM takes place at light loads (Figure 7). A comparator that truncates the low-side

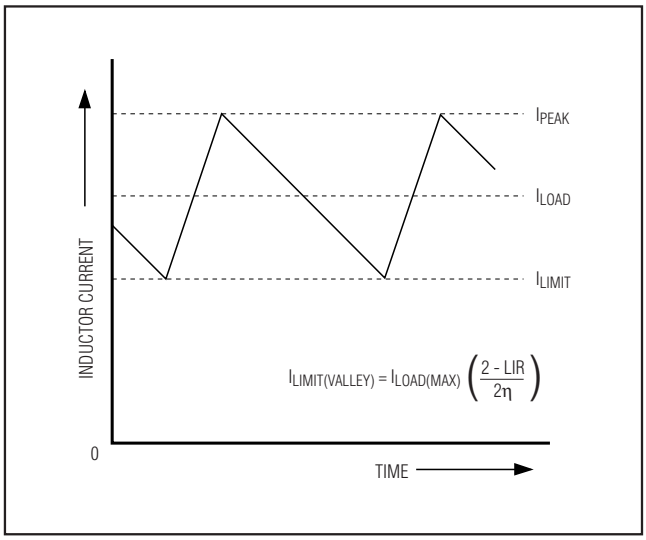

Figure 8. "Valley" Current-Limit Threshold Point

switch on-time at the inductor current's zero crossing affects this switchover. The zero-crossing comparator senses the inductor current across the current-sense resistors. Once V_{C_P} - V_{C_N} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics*), the comparator forces DL low (Figure 5). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 7). For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on

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the input voltage due to the typically low duty cycles. The total load current at the PFM/PWM crossover threshold ($I_{LOAD(SKIP)}$) is approximately:

$$I_{LOAD(SKIP)} = \eta_{TOTAL} \left(\frac{V_{OUT}K}{L} \right) \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$

where η_{TOTAL} is the number of active phases, and K is the on-time scale factor (Table 6).

The switching waveforms may appear noisy and asynchronous when light loading activates the pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Varying the inductor value makes trade-offs between PFM noise and light-load efficiency. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response, especially at low input voltage levels.

Current-Limit Circuit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses current-sense resistors between the current-sense inputs (C_P to C_N) as the current-sensing elements. If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle (Figure 8) until the inductor current of the selected phase drops below the valley current-limit threshold. When either phase trips the current limit, both phases are effectively current limited since the interleaved controller does not initiate a cycle with either phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when ILIM is adjusted. When a phase drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

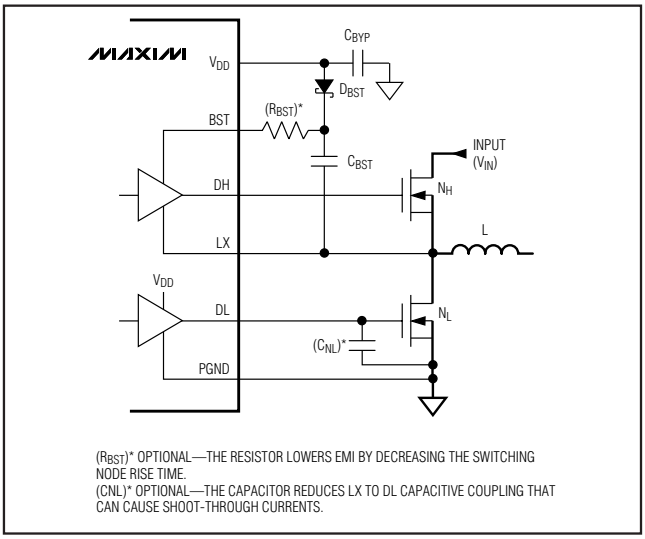

Figure 9. Optional Gate-Driver Circuitry

The current-limit threshold is adjusted with an external resistive voltage-divider at ILIM. The current-limit threshold voltage adjustment range is from 10mV to 75mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/20 the voltage seen at ILIM. The threshold defaults to 30mV when ILIM is connected to V_{CC}. The logic threshold for switchover to the 30mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (C_P, C_N).

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderately sized, high-side and larger, low-side power MOSFETs. This is consistent with the low-duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the Quick-PWM controller interprets the MOSFET gate as "off" while there is actually charge still left on the gate. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the device). The dead time at the other edge (DH turning off) is determined by a fixed 35ns internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.4Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive cou-

pling from the drain to the gate of the low-side MOSFETs when LX switches from ground to V_{IN}. Applications with high input voltages and long, inductive DL traces may require additional gate-to-source capacitance to ensure fast-rising LX edges do not pull up the low-side MOSFET's gate voltage, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the minimum threshold voltage:

$$V_{GS(TH)} < V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Typically, adding a 4700pF between DL and power ground (C_{NL} in Figure 9), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents may be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 9). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

Power-On Reset

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch, activating boot mode, and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching, and forces the DL gate driver high (to enforce output overvoltage protection). When V_{CC} rises above 4.25V, the DAC inputs are sampled and the output voltage begins to slew to the target voltage.

For automatic startup, the battery voltage should be present before V_{CC}. If the Quick-PWM controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. Toggle the $\overline{SHDN}$ pin to reset the fault latch.

Input Undervoltage Lockout

During startup, the V_{CC} UVLO circuitry forces the DL gate driver high and the DH gate driver low, inhibiting switching until an adequate supply voltage is reached. Once V_{CC} rises above 4.25V, valid transitions detected at the trigger input initiate a corresponding on-time pulse (see the *On-Time One-Shot* section). If the V_{CC} voltage drops below 4.25V, it is assumed that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller activates the shutdown sequence.

Multiphase Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$.

  For multiphase systems, each phase supports a fraction of the load, depending on the current balancing. When properly balanced, the load current is evenly distributed among each phase:

$$I_{LOAD(PHASE)} = \frac{I_{LOAD}}{\eta_{TOTAL}}$$

  where η_{TOTAL} is the total number of active phases.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient

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response vs. output noise. Low-inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \eta_{TOTAL}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where η_{TOTAL} is the total number of phases.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = \left(\frac{I_{LOAD(MAX)}}{\eta_{TOTAL}}\right)\left(1 + \frac{LIR}{2}\right)$$

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. For a dual-phase controller, the worst-case output sag voltage can be determined by:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2\left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - 2V_{OUT})K}{V_{IN}}\right) - 2t_{OFF(MIN)}\right] + \frac{\Delta I_{LOAD(MAX)}}{2C_{OUT}}\left[\left(\frac{V_{OUT}K}{V_{IN}}\right) + t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*) and K is from Table 6.

The amount of overshoot due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2\eta_{TOTAL} C_{OUT} V_{OUT}}$$

where η_{TOTAL} is the total number of active phases.

Setting the Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > \left(\frac{I_{LOAD(MAX)}}{\eta_{TOTAL}}\right)\left(1 - \frac{LIR}{2}\right)$$

where η_{TOTAL} is the total number of active phases, and $I_{LIMIT(LOW)}$ equals the minimum current-limit threshold voltage divided by the current-sense resistor (R_{SENSE}). For the 30mV default setting, the minimum current-limit threshold is 28mV.

Connect ILIM to V_{CC} for the default current-limit threshold (see the *Electrical Characteristics*). In adjustable mode, the current-limit threshold is precisely 1/20 the voltage seen at ILIM. For an adjustable threshold, connect a resistive divider from REF to GND with ILIM connected to the center tap. When adjusting the current limit, use 1% tolerance resistors with approximately 10µA of divider current to prevent a significant increase of errors in the current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In CPU V_{CORE} converters and other applications where the output is subject to large load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. When operating multiphase systems out-of-

phase, the peak inductor currents of each phase are staggered, resulting in lower output ripple voltage by reducing the total inductor ripple current. For 3- or 4-phase operation, the maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \frac{V_{RIPPLE}L}{(2V_{IN} - \eta_{TOTAL}V_{OUT})t_{ON} - \eta_{TOTAL}V_{OUT}t_{TRIG}}$$

where η_{TOTAL} is the total number of active phases, t_{ON} is the calculated on-time per phase, and t_{TRIG} is the trigger delay between the master's DH rising edge and the slave's DH rising edge. The trigger delay must be less than $1/(f_{SW} \times \eta_{TOTAL})$ for stable operation. The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of polymer types).

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section).

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \le \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{EFF}C_{OUT}}$$

and:

$$R_{EFF} = R_{ESR} + A_{VPS}R_{SENSE} + R_{PCB}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent-series resistance, R_{SENSE} is the current-sense resistance, A_{VPS} is the voltage-positioning gain, and R_{PCB} is the parasitic board resistance between the output capacitors and sense resistors.

For a standard 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum, Sanyo POSCAP, and Panasonic SP capacitors in widespread use at the time of publication have typical ESR zero frequencies below 50kHz. For example, the ESR needed to support a $30mV_{P-P}$ ripple in a 40A design is $30mV/(40A \times 0.3) = 2.5m\Omega$. Four 330µF/2.5V Panasonic SP (type XR) capacitors in parallel provide $2.5m\Omega$ (max) ESR. Their typical combined ESR results in a zero at 40kHz.

Ceramic capacitors have a high ESR zero frequency, but applications with significant voltage positioning can take advantage of their size and low ESR. Do not put high-value ceramic capacitors directly across the output without verifying that the circuit contains enough voltage positioning and series PC board resistance to ensure stability. When only using ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value can cause output overshoot when stepping from full-load to no-load conditions, unless a small inductor value is used (high switching frequency) to minimize the energy transferred from inductor to capacitor during load-step recovery. The efficiency penalty for operating at 550kHz is about 5% when compared to the 300kHz circuit, primarily due to the high-side MOSFET switching losses.

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and feedback loop instability. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

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Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The multiphase Quick-PWM controllers operate out-of-phase, while the Quick-PWM slave controllers provide selectable out-of-phase or in-phase on-time triggering. Out-of-phase operation reduces the RMS input current by dividing the input current between several staggered stages. For duty cycles less than $100\%/\eta_{OUTPH}$ per phase, the I_{RMS} requirements may be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{\eta_{OUTPH} V_{IN}}\right)\sqrt{\eta_{OUTPH} V_{OUT}(V_{IN} - \eta_{OUTPH} V_{OUT})}$$

where η_{OUTPH} is the total number of out-of-phase switching regulators. The worst-case RMS current requirement occurs when operating with $V_{IN} = 2\eta_{OUTPH}V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}/\eta_{OUTPH}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON™) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than 10°C temperature rise at the RMS input current for optimal circuit longevity.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two SO-8s, DPAK, or D^2PAK), and is reasonably priced. Ensure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur (see the *MOSFET Gate Driver* section).

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\ (N_H\ RESISTIVE) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

where η_{TOTAL} is the total number of phases.

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFETs can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\ (N_H\ SWITCHING) = (V_{IN(MAX)})^2\left(\frac{C_{RSS} f_{SW}}{I_{GATE}}\right)\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)$$

where C_{RSS} is the reverse transfer capacitance of N_H and I_{GATE} is the peak gate-drive source/sink current (1A, typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the $C \times V_{IN}^2 \times f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

OS-CON is a trademark of Sanyo.

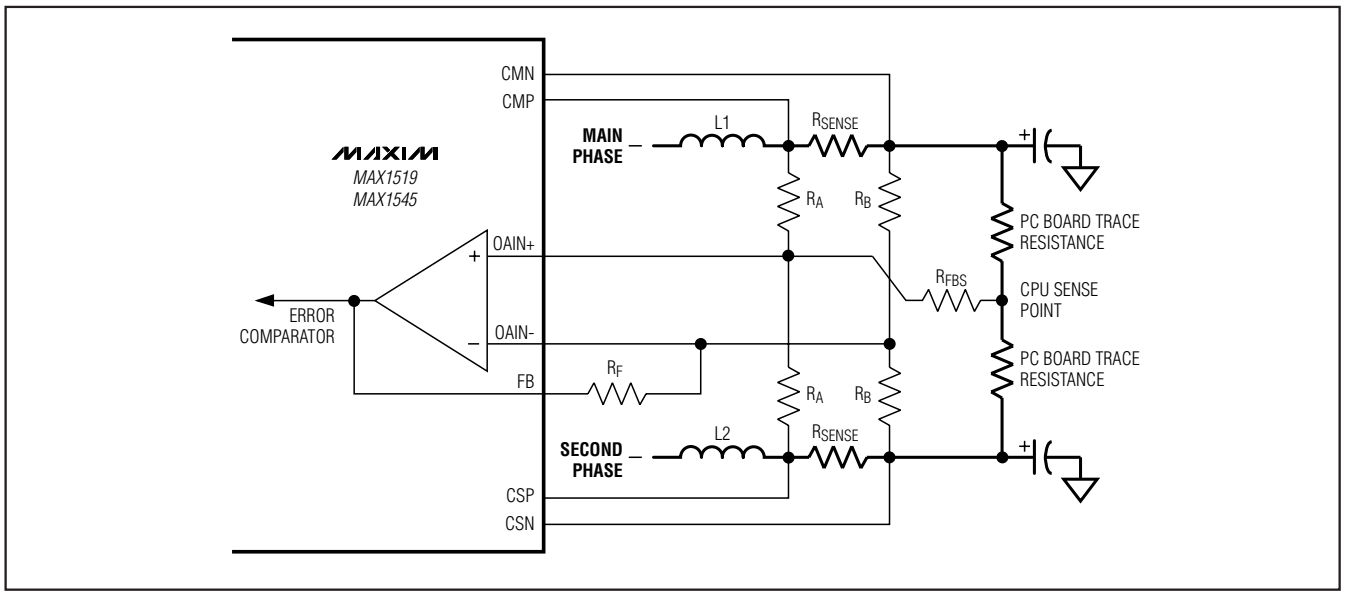

Figure 10. Voltage-Positioning Gain

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (N_L\ RESISTIVE) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{\eta_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst-case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "overdesign" the circuit to tolerate:

$$I_{LOAD} = \eta_{TOTAL_L}\left(I_{VALLEY(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}\right)$$

$$= \eta_{TOTAL} I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2}\right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 of the load current-per-phase. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) selected must be large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFET's gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W N-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

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Current-Balance Compensation (CCI)

The current-balance compensation capacitor (C_{CCI}) integrates the difference between the main and secondary current-sense voltages. The internal compensation resistor (R_{CCI} = 20kΩ) improves transient response by increasing the phase margin. This allows the dynamics of the current-balance loop to be optimized. Excessively large capacitor values increase the integration time constant, resulting in larger current differences between the phases during transients. Excessively small capacitor values allow the current loop to respond cycle-by-cycle but can result in small DC current variations between the phases. Likewise, excessively large resistor values can also cause DC current variations between the phases. Small resistor values reduce the phase margin, resulting in marginal stability in the current-balance loop. For most applications, a 470pF capacitor from CCI to the switching regulator's output works well.

Connecting the compensation network to the output (V_{OUT}) allows the controller to feed forward the output voltage signal, especially during transients. To reduce noise pickup in applications that have a widely distributed layout, it is sometimes helpful to connect the compensation network to the quiet analog ground rather than V_{OUT}.

Setting Voltage Positioning

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the processor's power dissipation. When the output is loaded, an op amp (Figure 5) increases the signal fed back to the Quick-PWM controller's feedback input. The adjustable amplification allows the use of standard, current-sense resistor values, and significantly reduces the power dissipated since smaller current-sense resistors can be used. The load-transient response of this control loop is extremely fast, yet well controlled, so the amount of voltage change can be accurately confined within the limits stipulated in the microprocessor power-supply guidelines.

The voltage-positioned circuit determines the load current from the voltage across the current-sense resistors ($R_{SENSE} = R_{CM} = R_{CS}$) connected between the inductors and output capacitors, as shown in Figure 10. The voltage drop can be determined by the following equation:

$$V_{VPS} = A_{VPS} I_{LOAD} R_{SENSE}$$

$$A_{VPS} = \frac{\eta_{SUM} R_F}{\eta_{TOTAL} R_B}$$

where η_{SUM} is the number of phases summed together for voltage-positioning feedback, and η_{TOTAL} is the total number of active phases. When the slave controller is disabled, the current-sense summation maintains the proper voltage-positioned slope. Select the positive input summing resistors so $R_{FBS} = R_F$ and $R_A = R_B$.

Minimum Input Voltage Requirements and Dropout Performance

The nonadjustable minimum off-time one-shot and the number of phases restrict the output voltage adjustable range for continuous-conduction operation. For best dropout performance, use the slower (200kHz) on-time settings. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the TON K-factor. This error is greater at higher frequencies (Table 6). Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \eta_{OUTPH}\left[\frac{V_{FB} - V_{VPS} + V_{DROP1}}{1 - \eta_{OUTPH}\left(\frac{h \times t_{OFF(MIN)}}{K}\right)}\right] + V_{DROP2} - V_{DROP1} + V_{VPS}$$

where η_{OUTPH} is the total number of out-of-phase switching regulators, V_{VPS} is the voltage-positioning droop, V_{DROP1} and V_{DROP2} are the parasitic voltage drops in the discharge and charge paths (see the *On-Time One-Shot* section), $t_{OFF(MIN)}$ is from the *Electrical Characteristics*, and K is taken from Table 6. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout design example:

V_{FB} = 1.4V

K_{MIN} = 3µs for f_{SW} = 300kHz

$t_{OFF(MIN)}$ = 400ns

V_{VPS} = 3mV/A × 30A = 90mV

V_{DROP1} = V_{DROP2} = 150mV (30A load)

h = 1.5 and η_{OUTPH} = 2

$$V_{IN(MIN)} = 2 \times \left[\frac{1.4V - 90mV + 150mV}{1 - 2 \times (0.4\mu s \times 1.5/3.0\mu s} \right] + 150mV - 150mV + 90mV = 4.96V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = 2 \times \left[\frac{1.4V - 90mV + 150mV}{1 - 2 \times (0.4\mu s \times 1.0/3.0\mu s} \right] + 150mV - 150mV + 90mV = 4.07V$$

Therefore, V_{IN} must be greater than 4.1V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 5V.

Applications Information

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 11). If possible, mount all of the power components on the topside of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
2) Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, REF and GNDS bypass capacitors, compensation (CC_) components, and the resistive dividers connected to ILIM and OFS.
3) Each slave controller should also have a separate analog ground. Return the appropriate noise-sensitive slave components to this plane. Since the reference in the master is sometimes connected to the slave, it may be necessary to couple the analog ground in the master to the analog ground in the slave to prevent ground offsets. A low-value (≤10Ω) resistor is sufficient to link the two grounds.
4) Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
5) Keep the high-current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
6) C_P, C_N, OAIN+, and OAIN- connections for current limiting and voltage positioning must be made using Kelvin-sense connections to guarantee the current-sense accuracy.
7) When trade-offs in trace lengths must be made, it is preferable to allow the inductor-charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
8) Route high-speed switching nodes away from sensitive analog areas (REF, CCV, CCI, FB, C_P, C_N, etc). Make all pin-strap control input connections ($\overline{SHDN}$, ILIM, $\overline{SKIP}$, SUS, S_, TON) to analog ground or V_{CC} rather than power ground or V_{DD}.

Layout Procedure

Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas:

1) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).

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2) Group the gate-drive components (BST diodes and capacitors, V_{DD} bypass capacitor) together near the controller IC.

3) Make the DC-to-DC controller ground connections as shown in the *Standard Application Circuits*. This diagram can be viewed as having four separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the PGND pin and V_{DD} bypass capacitor go; the master's analog ground plane, where sensitive analog components, the master's GND pin, and V_{CC} bypass capacitor go; and the slave's analog ground plane, where the slave's GND pin and V_{CC} bypass capacitor go. The master's GND plane must meet the PGND plane only at a single point directly beneath the IC. Similarly, the slave's GND plane must meet the PGND plane only at a single point directly beneath the IC. The respective master and slave ground planes should connect to the high-power output ground with a short metal trace from PGND to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.

4) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-to-DC converter circuit as close to the CPU as is practical.

Chip Information

TRANSISTOR COUNT: 11,015

PROCESS: BiCMOS

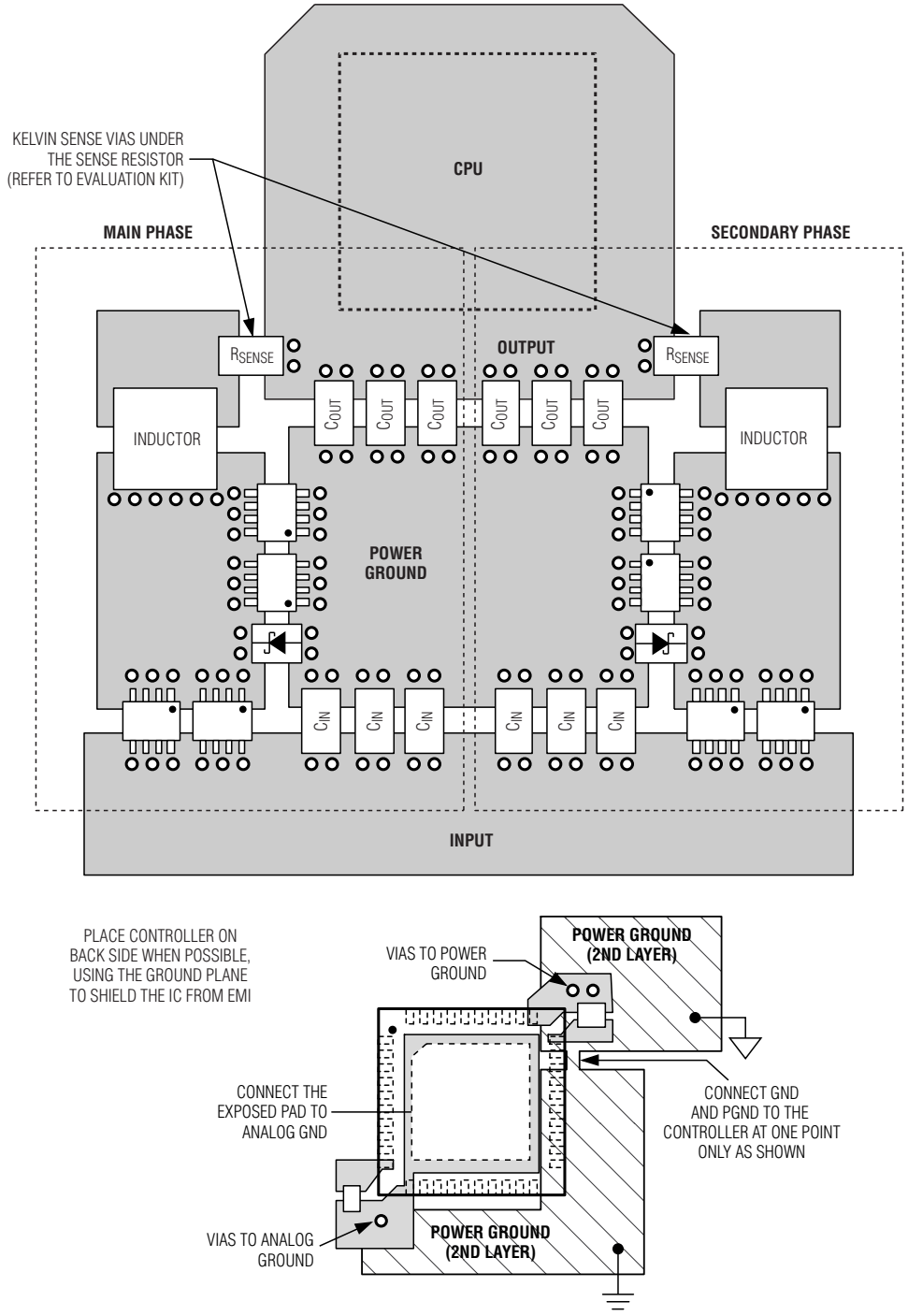

Figure 11. PC Board Layout Example

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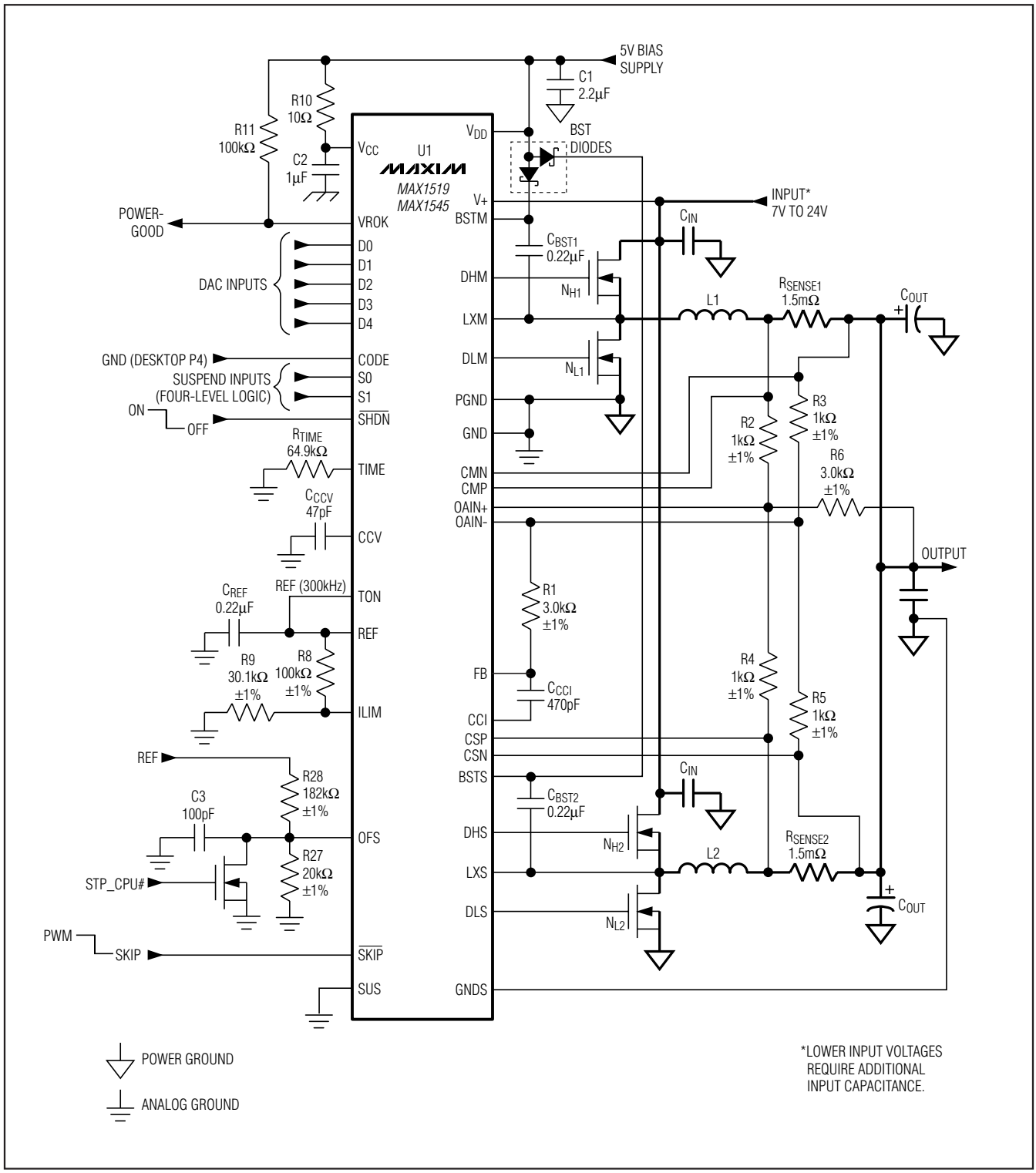


Figure 12a. Standard 4-Phase Desktop P4 Application Circuit (1st and 2nd Phases—MAX1519/MAX1545 Master)

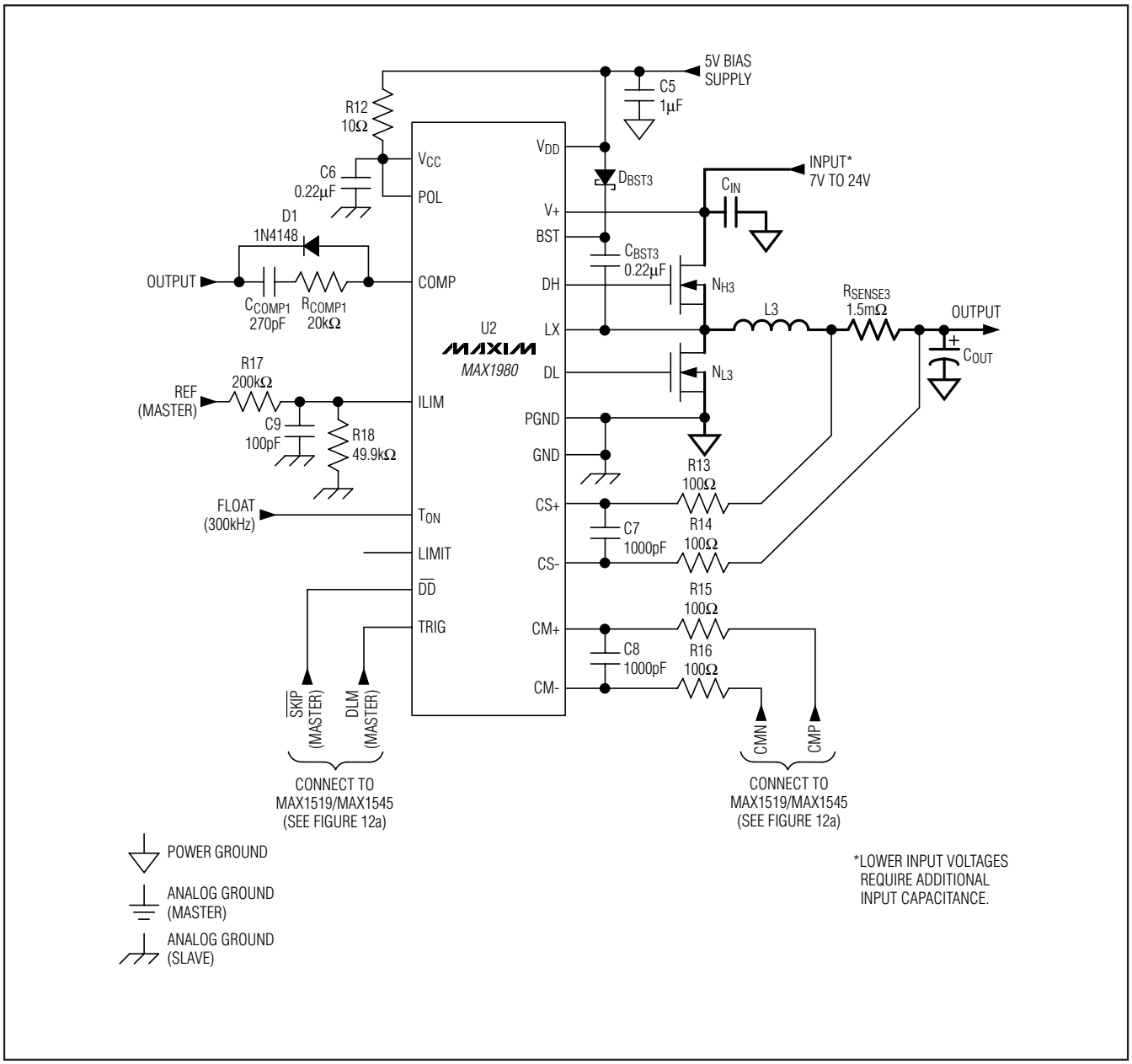


Figure 12b. Standard 4-Phase Desktop 4 Application Circuit (3rd Phase—MAX1980 Slave)

Dual-Phase, Quick-PWM Controllers for Programmable CPU Core Power Supplies

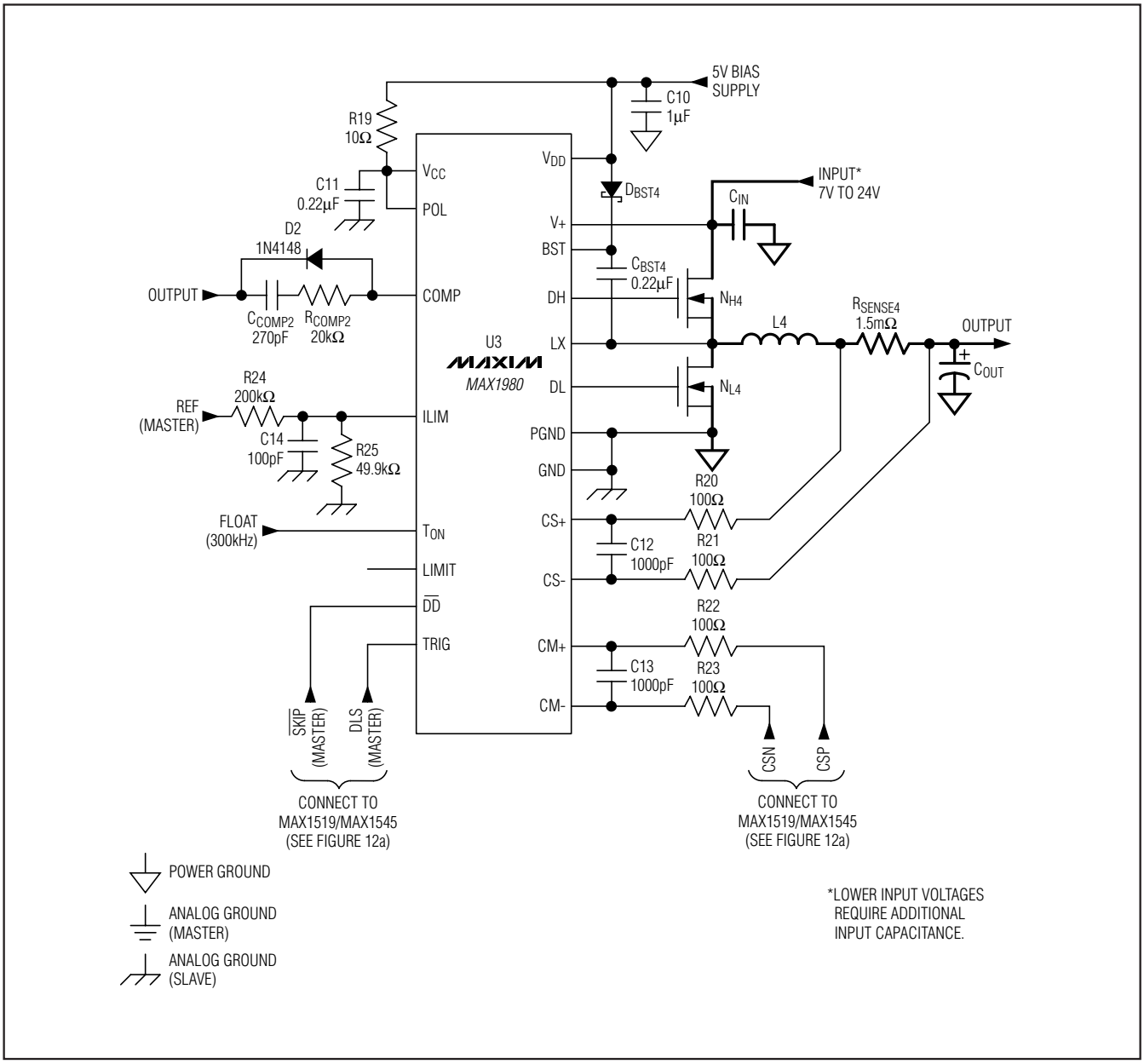
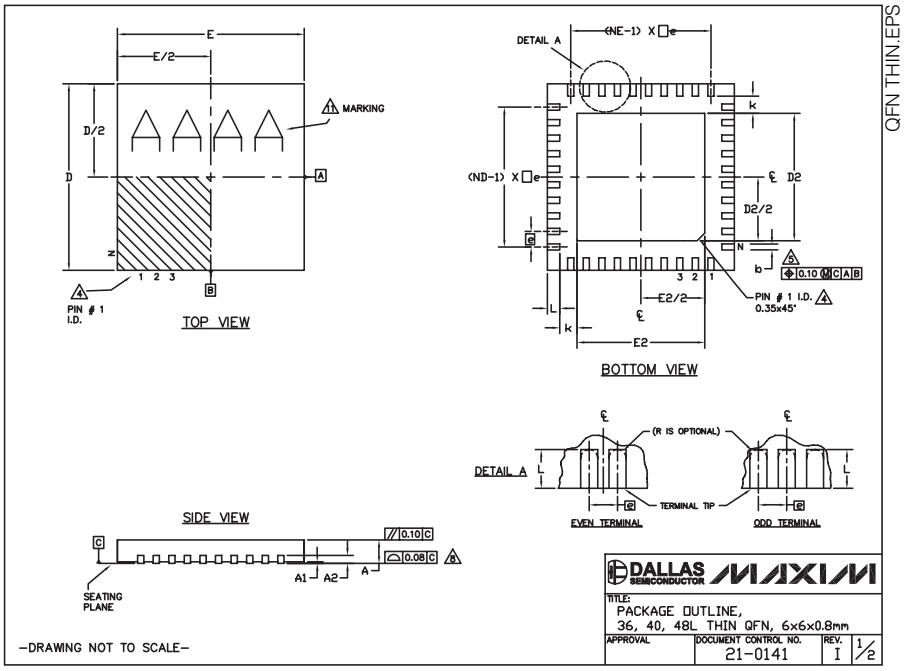


Figure 12c. Standard 4-Phase Desktop 4 Application Circuit (4th Phase—MAX1980 Slave)

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0141
REV. I
2/2