Ordering Information

PART NO.	TEMP. RANGE (^{O}C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL6141CBZA (See Note)	0 to 70	8 Lead SOIC	M8.15
ISL6151CBZA (See Note) **(No longer available or supported)**	0 to 70	8 Lead SOIC	M8.15
ISL6141IBZA (See Note)	-40 to 85	8 Lead SOIC	M8.15
ISL6151IBZA (See Note) **(No longer available or supported)**	-40 to 85	8 Lead SOIC	M8.15

*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

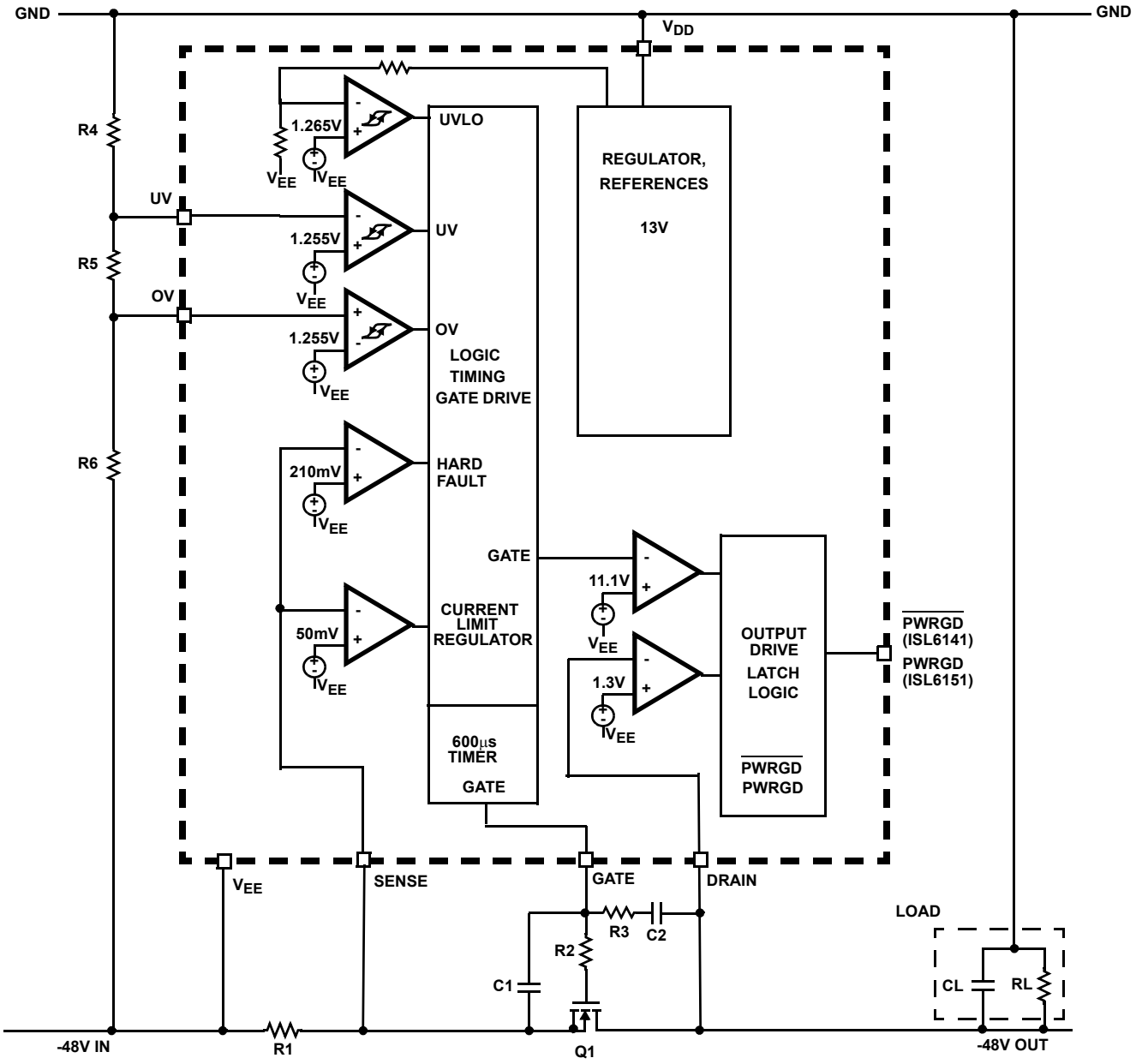

FIGURE 1. BLOCK DIAGRAM

Pin Descriptions

$\overline{\text{PWRGD}}$ (ISL6141; L Version) Pin 1

This digital output is an open-drain pull-down device. During start-up the DRAIN and GATE voltages are monitored with two separate comparators. The first comparator looks at the DRAIN pin voltage compared to the internal V_{PG} reference (V_{PG} is nominal 1.3V); this measures the voltage drop across the external FET and sense resistor. When the DRAIN to V_{EE} voltage drop is less than 1.3V, the first of two conditions required for the power to be considered good are met. In addition, the GATE voltage monitored by the second comparator must be within approximately 2.5V of its normal operating voltage (13.6V). When both criteria are met the $\overline{\text{PWRGD}}$ output will transition from high to low, enabling a power module in some applications. The output is latched in the low state until any of the signals that shut off the GATE occur (Over-Voltage, Under-Voltage, Under-Voltage Lock-Out, Over-Current Time-Out, or powering down). Any of these conditions will re-set the latch and the $\overline{\text{PWRGD}}$ output will transition from low to high indicating power is no longer good. In this case the output pull-down device shuts off, and the pin becomes high impedance. Typically an external pull-up of some kind is used to pull the pin high (many brick regulators have a pull-up function built in).

PWRGD (ISL6151; H Version) Pin 1 - This digital output is used to provide an active high signal to enable an external module. The Power Good comparators are the same as described above, but the active state of the output is reversed (reference Figure 33).

If the latch is reset (GATE turns off), the internal DMOS device (Q3) is turned off, and Q2 (NPN) turns on to clamp the output one diode drop above the DRAIN voltage to produce a logic low.

Once the latch is set (both DRAIN and GATE are normal), the DMOS device (Q3) turns on and sinks current to V_{EE} through a 6.2KΩ resistor. The base of Q2 is clamped to V_{EE} to turn it off. If the external pull-up current is high enough (>1mA, for example), the voltage drop across the resistor will be large enough to produce a logic high output (in this example, 1mA * 6.2kΩ = 6.2V) and enable the external module.

Note that for all H versions, although this is a digital pin functionally, the logic high level is determined by the external pull-up device, and the power supply to which it is connected; the IC will not clamp it below the V_{DD} voltage. Therefore, if the external device does not have its own clamp, or if it would be damaged by a high voltage, an external clamp might be necessary.

OV (Over-Voltage) Pin 2 - This analog input compares the voltage on the pin to an internal voltage reference of 1.255V (nominal). When the input goes above the reference (low to high transition) an Over-Voltage condition is detected and the GATE pin is immediately pulled low to shut off the external FET. The built in 25mV hysteresis will keep the GATE off until the OV pin drops below 1.230V, which is the nominal high to low threshold. A typical application will use an external resistor divider from V_{DD} to V_{EE} to set the OV level as desired. A three-resistor divider can be used to set both OV and UV trip points.

UV (Under-Voltage) Pin 3 - This analog input compares the voltage on the pin to an internal comparator with a built in hysteresis of 135mV. When the UV input goes below the nominal reference (high to low transition) voltage of 1.120V, the GATE pin is immediately pulled low to shut off the external FET. Since the comparator has a built in 135mV hysteresis the GATE will remain off until the UV pin rises above a 1.255V low to high threshold. A typical application will use an external resistor divider from V_{DD} to V_{EE} to set the UV level as desired. A three-resistor divider can be used to set both OV and UV trip points.

The UV pin is also used to reset the Over-Current latch. The pin must be cycled below 1.120V (nominal) and then above 1.255V (nominal) to clear the latch and initiate a normal power-up sequence.

V_{EE} Pin 4 - This is the most negative supply voltage, such as in a -48V system. Most of the other signals are referenced relative to this pin, even though it may be far away from what is considered a GND reference.

SENSE Pin 5 - This analog input monitors the voltage drop across the external sense resistor (between SENSE and V_{EE}) to determine if the current exceeds the programmed Over-Current trip point, equal to 50mV / Rsense. If the load current exceeds the Over-Current threshold, the circuit will regulate the current to maintain the nominal voltage drop (50mV) across the sensing resistor R1 (Rsense). If current is limited for more than 600µs, the Over-Current shutdown (also called electronic circuit breaker) will quickly turn off the FET and latch the GATE pin off.

A Hard Fault comparator is employed to detect and respond quickly to severe short circuits. The threshold of this comparator is set approximately four times higher (210mV) than the Over-Current trip point. When its threshold is exceeded the GATE is immediately (10µs typical) shut off, the timer is reset, and a single retry (soft start) is attempted before latching the GATE off (assuming the fault remains). During the retry, if the fault disappears prior to the Over-Current Time-Out period (600µs) the FET will remain on as normal. If the GATE is latched off, the user must either toggle the UV pin below then above its threshold, or reduce the supply voltage below the V_{DD} UVLO trip point and then above it. This will clear the latch and initiate a normal power-up sequence.

GATE Pin 6 - This analog output drives the gate of the external FET used as a pass transistor. The GATE pin is high (FET is on) when the following conditions are met:

- UVLO is above its trip point (~16.5V)
- Voltage on the UV pin is above its trip point (1.255V)
- Voltage on the OV pin is below its trip point (1.255V)
- No Over-Current conditions are present.

If any of the 4 conditions are violated, the GATE pin will be pulled low to shut off or regulate current through the FET. The GATE is latched off only when the 600µs Over-Current Time-Out period is exceeded.

The GATE is driven high by a weak (-50µA nominal) pull-up current source, in order to slowly turn on the FET. It is driven low by a 70mA nominal pull-down device for three of the above shut-off conditions. A larger (350mA nominal) pull-down current shuts off the FET very quickly in the event of a hard fault where the sense pin voltage exceeds approximately 210mV.

DRAIN Pin 7 - This is the analog input to one of two comparators that control the $\overline{\text{PWRGD}}$ (ISL6141) or PWRGD (ISL6151) outputs. It compares the voltage of the external FET DRAIN to a 1.3V internal reference (V_{PG}). The DRAIN voltage is criticized only until the $\overline{\text{PWRGD}}$ or PWRGD outputs are latched into their active low or high states. The latch is reset when any of the conditions that turn off the GATE occur (UVLO, OV, UV, OC Time-Out). Note that the comparator does NOT itself turn off the GATE.

V_{DD} Pin 8 - This is the most positive power supply pin. It can range from the Under-Voltage Lock-Out threshold (16.5V) to +80V (Relative to V_{EE}).

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{EE}) . . . . . -0.3V to 100V
DRAIN, $\overline{PWRGD}$, PWRGD Voltage . . . . . -0.3V to 100V
UV, OV Input Voltage . . . . . -0.3V to 60V
SENSE, GATE Voltage . . . . . -0.3V to 20V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 2000V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
8 Lead SOIC	90

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C

Operating Conditions

Temperature Range (Industrial) . . . . . -40^{o}C to 85^{o}C
Temperature Range (Commercial) . . . . . 0^{o}C to 70^{o}C
Supply Voltage Range (Typical) . . . . . 36V to 72V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. PWRGD is referenced to DRAIN; V_{PWRGD}-V_{DRAIN} = 0V.

Electrical Specifications

V_{DD} = +48V, V_{EE} = +0V Unless Otherwise Specified. All tests are over the full temperature range; either Commercial (0^{o}C to 70^{o}C) or Industrial (-40^{o}C to 85^{o}C). Typical specs are at 25^{o}C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	Units
DC PARAMETERS						
V_{DD} PIN						
Supply Operating Range	V_{DD}		20	-	80	V
Supply Current	I_{DD}	UV = 3V; OV = V_{EE}; SENSE = V_{EE}; V_{DD} = 80V		2.4	4.5	mA
UVLO High	V_{UVLOH}	V_{DD} Low to High transition	15	16.7	19	V
UVLO Low	V_{UVLOL}	V_{DD} High to Low transition	13	14.8	17	V
UVLO hysteresis				1.9		V
GATE PIN						
GATE Pin Pull-Up Current	I_{PU}	GATE Drive on, V_{GATE} = V_{EE}	-30	-50	-60	µA
GATE Pin Pull-Down Current	I_{PD1}	GATE Drive off, UV or OV false		70		mA
GATE Pin Pull-Down Current	I_{PD2}	GATE Drive off, Over-Current Time-Out		70		mA
GATE Pin Pull-Down Current	I_{PD3}	GATE Drive off; Hard Fault (Vsense > 210mV)		350		mA
External GATE Drive (V_{DD} = 20V, 80V)	ΔV_{GATE}	(V_{GATE} - V_{EE}), 20V <=V_{DD} <=80V	12	13.6	15	V
GATE High Threshold ($\overline{PWRGD}$/PWRGD active)	V_{GH}	ΔV_{GATE} - V_{GATE}		2.5		V
SENSE PIN						
Current Limit Trip Voltage	V_{CL}	V_{CL} = (V_{SENSE} - V_{EE})	40	50	60	mV
Hard Fault Trip Voltage	V_{HFT}	V_{HFTV} = (V_{SENSE} - V_{EE})		210		mV
SENSE Pin Current	I_{SENSE}	V_{SENSE} = 50mV		-1.3	-4.0	µA
UV PIN						
UV Pin High Threshold Voltage	V_{UVH}	UV Low to High Transition	1.240	1.255	1.270	V
UV Pin Low Threshold Voltage	V_{UVL}	UV High to Low Transition	1.105	1.120	1.145	V
UV Pin Hysteresis	V_{UVHY}			135		mV

Electrical Specifications V_{DD} = +48V, V_{EE} = +0V Unless Otherwise Specified. All tests are over the full temperature range; either Commercial (0°C to 70°C) or Industrial (-40°C to 85°C). Typical specs are at 25°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	Units
UV Pin Input Current	I_{INUV}	$V_{UV} = V_{EE}$		-0.05	-0.5	µA
OV pin						
OV Pin High Threshold Voltage	V_{OVH}	OV Low to High Transition	1.235	1.255	1.275	V
OV Pin Low Threshold Voltage	V_{OVL}	OV High to Low Transition	1.215	1.230	1.255	V
OV Pin Hysteresis	V_{OVHY}			25		mV
OV Pin Input Current	I_{INOV}	$V_{OV} = V_{EE}$		-0.05	-0.5	µA
DRAIN Pin						
Power Good Threshold ($\overline{PWRGD}$/PWRGD active)	V_{PG}	$V_{DRAIN} - V_{EE}$	0.80	1.30	2.00	V
DRAIN Input Bias Current	I_{DRAIN}	V_{DRAIN} = 48V		38	60	µA
ISL6141 ($\overline{PWRGD}$ Pin: L Version)						
$\overline{PWRGD}$ Output Low Voltage	V_{OL1} V_{OL5}	$(V_{DRAIN} - V_{EE}) < V_{PG}$; I_{OUT} = 1mA	-	0.30	1.0	V
		$(V_{DRAIN} - V_{EE}) < V_{PG}$; I_{OUT} = 5mA	-	1.50	3.0	V
Output Leakage	I_{OH}	V_{DRAIN} = 48V, $V_{\overline{PWRGD}}$ = 80V	-	0.05	10	µA
ISL6151 (PWRGD Pin: H Version)						
PWRGD Output Low Voltage (PWRGD-DRAIN)	V_{OL}	V_{DRAIN} = 5V, I_{OUT} = 1mA	-	0.85	1.0	V
PWRGD Output Impedance	R_{OUT}	$(V_{DRAIN} - V_{EE}) < V_{PG}$	3.5	6.2	9.0	kΩ
AC Timing						
OV High to GATE Low	t_{PHLOV}	Figures 2A, 3A	0.6	1.3	3.0	µs
OV Low to GATE High	t_{PLHOV}	Figures 2A, 3A	1.0	4.5	12.0	µs
UV Low to GATE Low	t_{PHLUV}	Figures 2A, 3B	0.6	0.90	3.0	µs
UV High to GATE High	t_{PLHUV}	Figures 2A, 3B	1.0	5.0	12.0	µs
SENSE High to GATE Low	$t_{PHLSENSE}$	Figures 2A, 6		0.35	3	µs
Current Limit to GATE Low (O.C. Time-out)	t_{PHLCB}	Figures 2B, 8		600		µs
Hard Fault to GATE Low (200mV comparator) Typical GATE shutdown based on application ckt. Guaranteed by design.	t_{PHLHF}	Figures 7, 23, 27 (zero Ω short to V_{DD})		10		µs
ISL6141 (L Version)						
DRAIN Low to $\overline{PWRGD}$ Low	t_{PHLDL}	Figures 2A, 4A (note 2)		3.0	5.0	µs
GATE High to $\overline{PWRGD}$ Low	t_{PHLGH}	Figures 2A, 5A (note 2)		1.0	3.0	µs
ISL6151 (H Version)						
DRAIN Low to (PWRGD-DRAIN) High	t_{PLHDL}	Figures 2A, 4B (note 2)		3.0	5.0	µs
GATE High to (PWRGD-DRAIN) High	t_{PLHGH}	Figures 2A, 5B (note 2)		0.4	3.0	µs

Test Circuit and Timing Diagrams

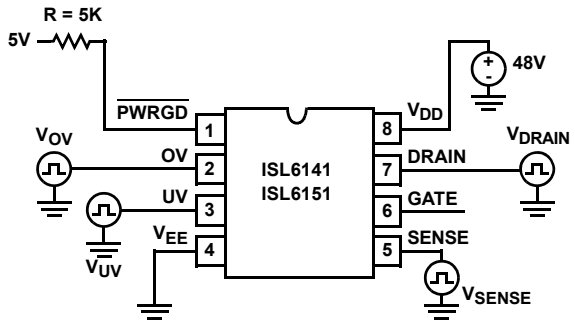

FIGURE 2A. TYPICAL TEST CIRCUIT

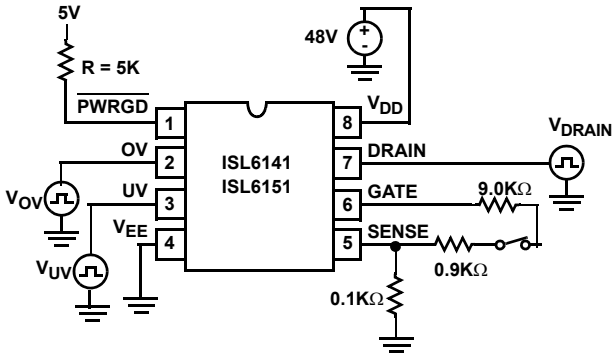

FIGURE 2B. TEST CIRCUIT FOR 600µs TIME-OUT

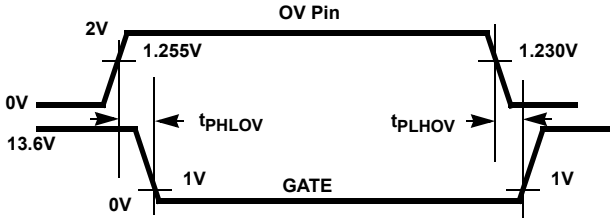

FIGURE 3A. OV TO GATE TIMING

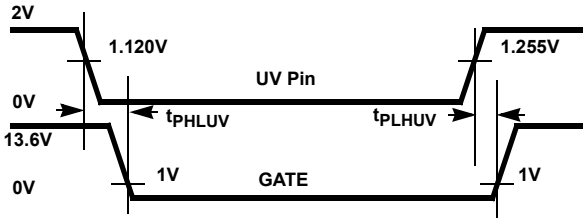

FIGURE 3B. UV TO GATE TIMING

FIGURE 3. OV AND UV TO GATE TIMING

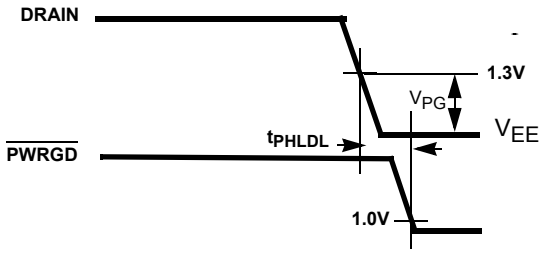

FIGURE 4A. DRAIN TO $\overline{\text{PWRGD}}$ TIMING (ISL6141)

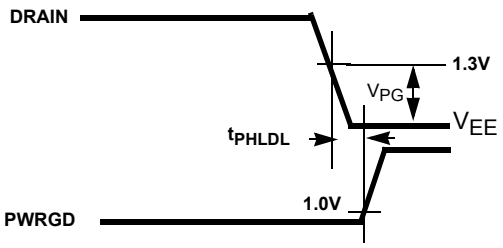

FIGURE 4B. DRAIN TO PWRGD TIMING (ISL6151)

FIGURE 4. DRAIN TO $\overline{\text{PWRGD}}$/PWRGD TIMING

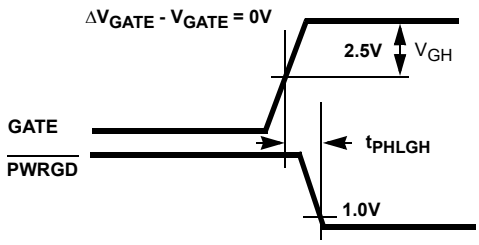

FIGURE 5A. GATE TO $\overline{\text{PWRGD}}$ (ISL6141)

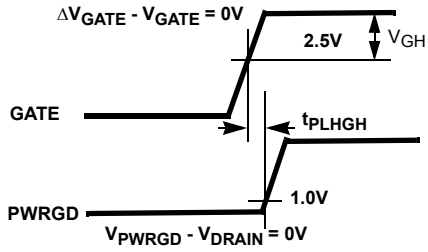

FIGURE 5B. GATE TO PWRGD (ISL6151)

FIGURE 5. GATE TO $\overline{\text{PWRGD}}$/PWRGD TIMING

Test Circuit and Timing Diagrams (Continued)

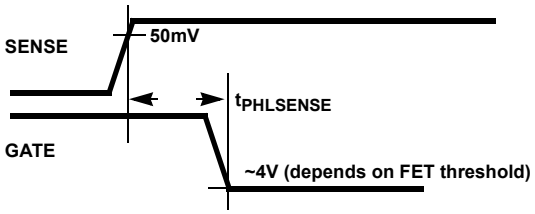

FIGURE 6. SENSE TO GATE TIMING

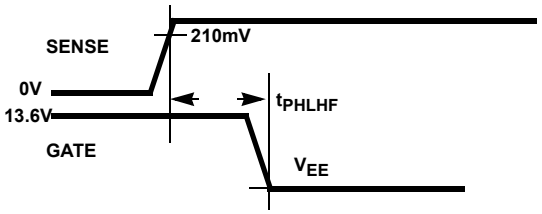

FIGURE 7. SENSE TO GATE (Hard Fault) TIMING

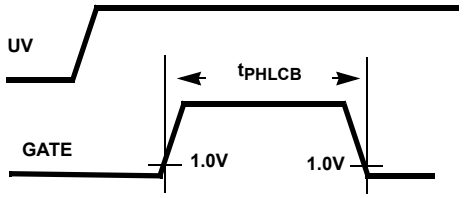

FIGURE 8. CURRENT LIMIT TO GATE TIMING

Typical Performance Curves

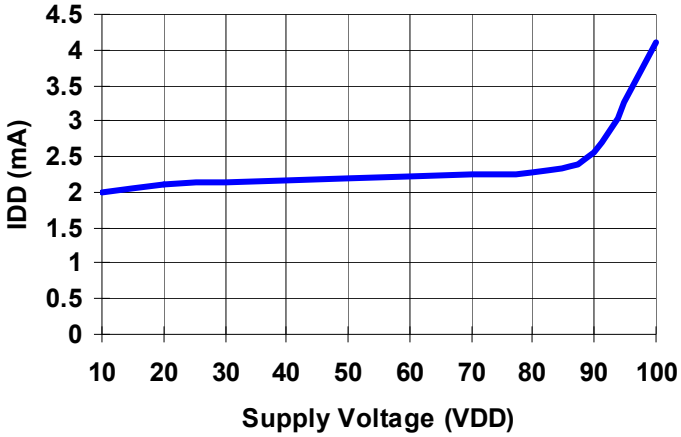

FIGURE 9. SUPPLY CURRENT VS. SUPPLY VOLTAGE (25°C)

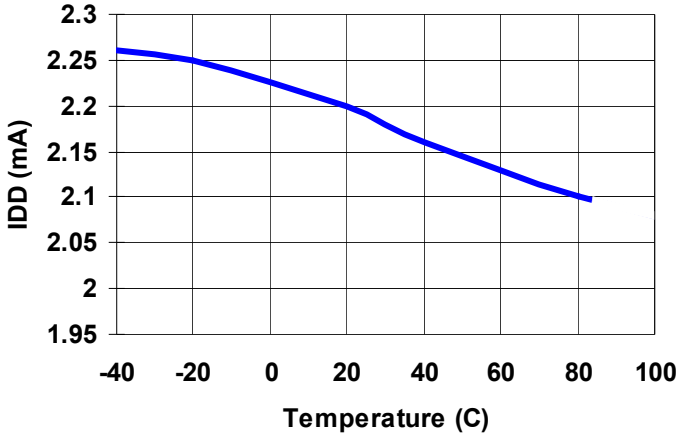

FIGURE 10. SUPPLY CURRENT VS. TEMPERATURE, V_{DD} = 48V

Typical Performance Curves (Continued)

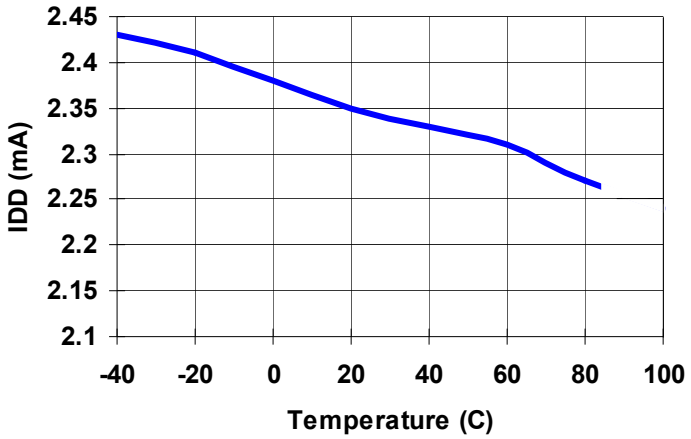

FIGURE 11. SUPPLY CURRENT VS TEMPERATURE, V_{DD} = 80V

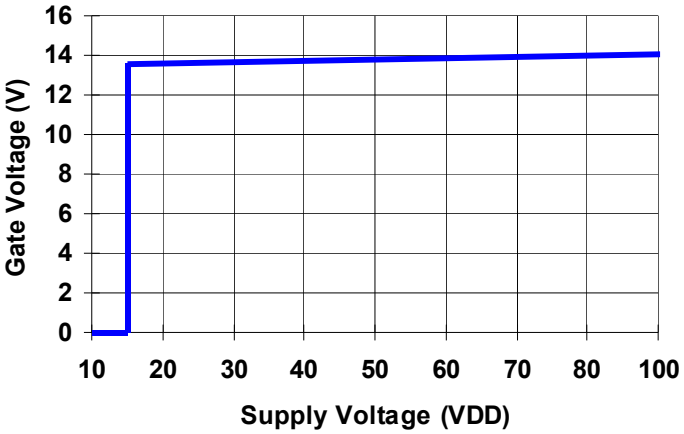

FIGURE 12. GATE VOLTAGE VS SUPPLY VOLTAGE (25°C)

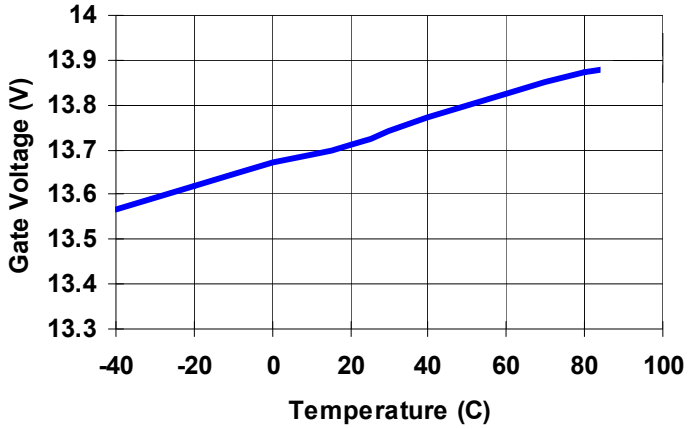

FIGURE 13. GATE VOLTAGE VS TEMPERATURE, V_{DD} = 48V

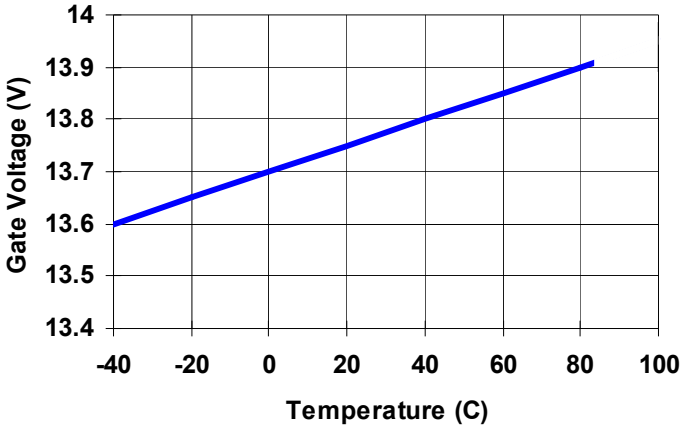

FIGURE 14. GATE VOLTAGE VS TEMPERATURE, V_{DD} = 80V

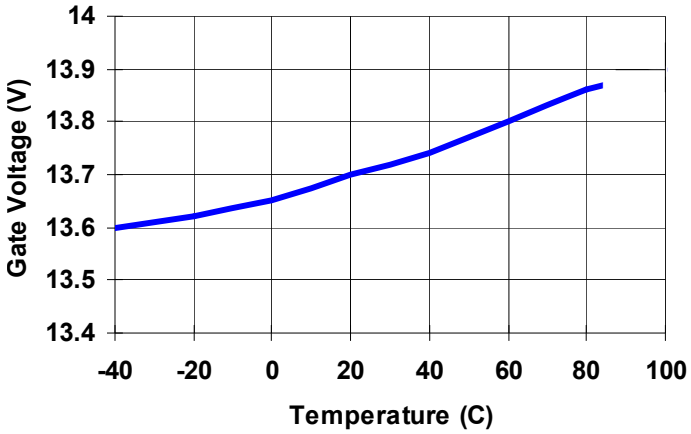

FIGURE 15. GATE VOLTAGE VS TEMPERATURE, V_{DD} = 20V

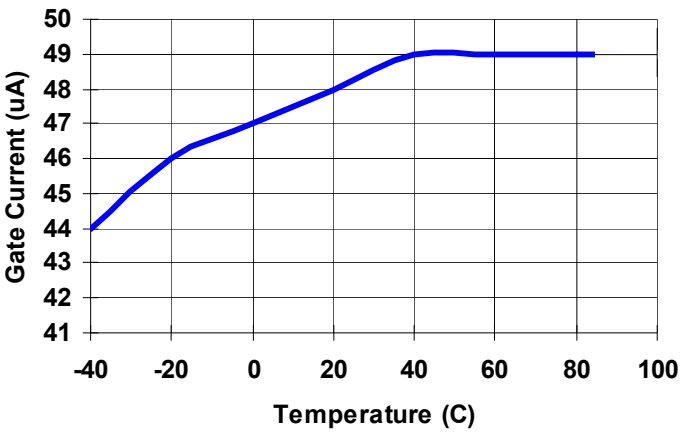

FIGURE 16. GATE PULL-UP CURRENT VS TEMPERATURE

Typical Performance Curves (Continued)

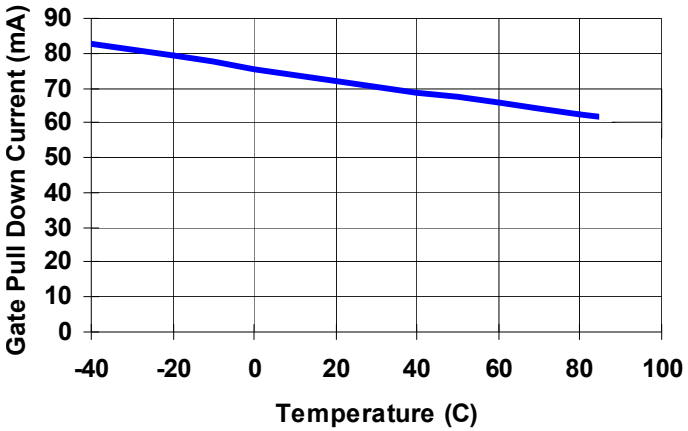

FIGURE 17. GATE PULL-DOWN CURRENT (UV/OV/TIME-OUT) VS TEMPERATURE

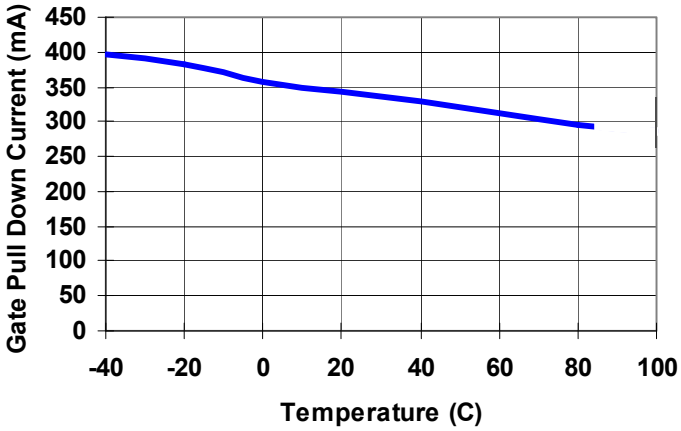

FIGURE 18. HARD FAULT GATE PULL-DOWN CURRENT (200mV COMPARATOR) VS TEMPERATURE

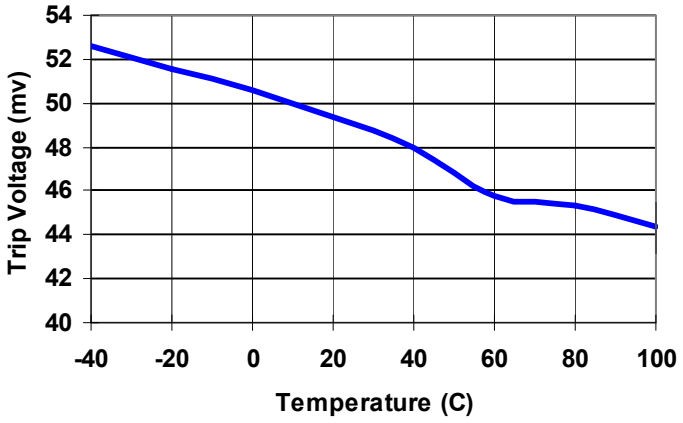

FIGURE 19. OVER-CURRENT TRIP VOLTAGE VS TEMPERATURE

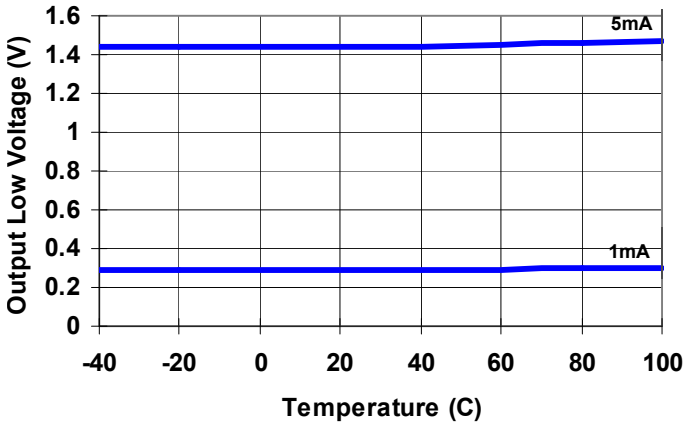

FIGURE 20. $\overline{\text{PWRGD}}$ (ISL6141) V_{OL} VS TEMPERATURE

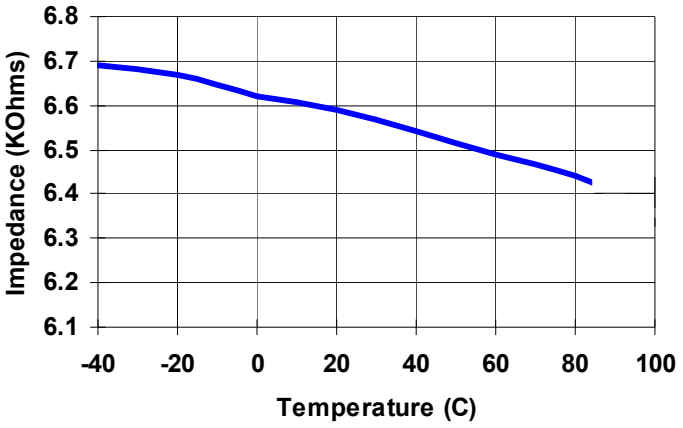

FIGURE 21. PWRGD (ISL6151) IMPEDANCE VS TEMPERATURE

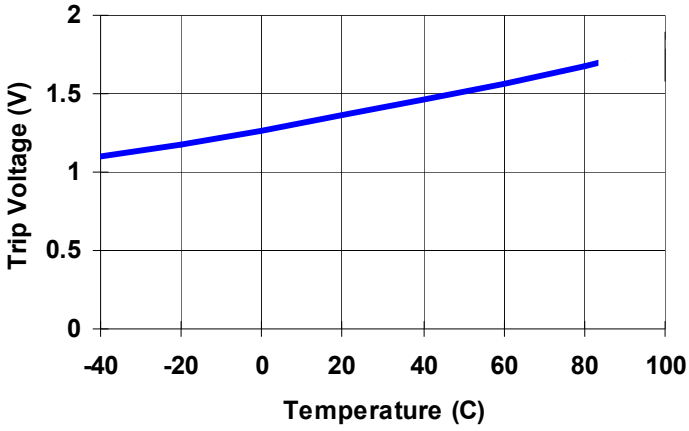

FIGURE 22. DRAIN to $\overline{\text{PWRGD}}$ / PWRGD TRIP VOLTAGE (V_{PG}) VS TEMPERATURE

Applications Information

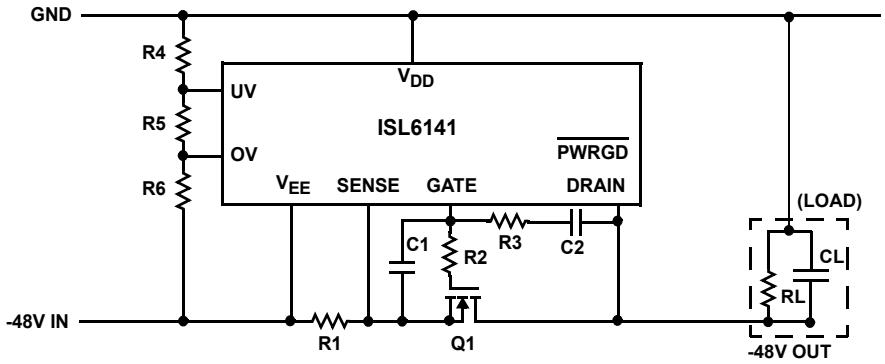

FIGURE 23. TYPICAL APPLICATION WITH MINIMUM COMPONENTS

Typical Values for a representative system; which assumes:

- 43V to 71V supply range; 48 nominal; UV = 43V; OV = 71V
- 1Amp of typical current draw; 2.5 Amp Over-Current
- 100µF of load capacitance (CL); equivalent RL of 48Ω (R = V/I = 48V/1A)

R1: 0.02Ω (1%)

R2: 10Ω (5%)

R3: 18kΩ (5%)

R4: 549kΩ (1%)

R5: 6.49kΩ (1%)

R6: 10kΩ (1%)

C1: 150nF (25V)

C2: 3.3nF (100V)

Q1: IRF530 (100V, 17A, 0.11Ω)

Quick Guide to Choosing Component Values

(See fig 23 for reference)

This section will describe the minimum components needed for a typical application, and will show how to select component values. (Note that “typical” values may only be good for this application; the user may have to select alternate component values to optimize performance for other applications). Each block will then have more detailed explanation of how the device works, and alternatives.

R4, R5, R6 - together set the Under-Voltage (UV) and Over-Voltage (OV) trip points. When the power supply ramps up and down, these trip points (and their hysteresis) will determine when the GATE is allowed to turn on and off (UV and OV do not control the $\overline{\text{PWRGD}}$ / PWRGD output). The input power supply is divided down such that when the voltage on the OV pin is below its threshold and the UV pin is above its threshold their comparators will be in the proper state signaling the supply is within its desired range, allowing the GATE to turn on. The equations below define the comparator thresholds for an increasing (in magnitude) supply voltage.

$$V_{UV} = \frac{\langle R_4 + R_5 + R_6 \rangle}{(R_5 + R_6)} \times 1.255 \quad \text{(EQ. 1)}$$

$$V_{OV} = \frac{\langle R_4 + R_5 + R_6 \rangle}{(R_6)} \times 1.255 \quad \text{(EQ. 2)}$$

The values of R4 = 549K, R5 = 6.49K, and R6 = 10K shown in figure 23 set the Under-Voltage turn-on threshold to 43V, and the Over-Voltage turn off threshold to 71V. The Under-Voltage (UV) comparator has a hysteresis of 135mV (4.6V of hysteresis on the supply) which correlates to a 38.4V turn off voltage. The Over-Voltage comparator has a 25mV hysteresis which translates to a turn on voltage (supply decreasing) of approximately 69.6V.

Q1 - is the FET that connects the input supply voltage to the output load, when properly enabled. It needs to be selected based on several criteria:

- Maximum voltage expected on the input supply (including transients) as well as transients on the output side.
- Maximum current and power dissipation expected during normal operation, usually at a level just below the current limit threshold.
- Power dissipation and/or safe-operating-area considerations during current limiting and single retry events.
- Other considerations include the GATE voltage threshold which affects the $r_{DS(ON)}$ (which in turn, affects the voltage drop across the FET during normal operation), and the maximum GATE voltage allowed (the ICs GATE output is clamped to ~14V).

R1 - Is the Over-Current sense resistor. If the input current is high enough, such that the voltage drop across R1 exceeds the SENSE comparator trip point (50mV nominal), the GATE pin will be pulled lower (to ~4V) and current will be regulated to 50mV/Rsense for approximately 600µs. The Over-Current threshold is defined in Equation 3 below. If the 600µs time-out period is exceeded the Over-Current latch will be set and the FET will be turned off to protect the load from excessive current. A typical value for R1 is 0.02Ω, which sets an Over-Current trip point of; I_{OC} = V/R = 0.05/0.02 = 2.5 Amps. To select the appropriate value for R1, the user must first determine at what level of current it should trip, take into account worst case variations for the trip point (50mV ±10mV = ±20%), and the tolerances of the resistor (typically 1% or 5%). Note that the Over-Current threshold should be set above the inrush current level plus the expected load current to avoid activating the current limit and time-out circuitry during start-up. If the power good output is used to enable an external module, the desired inrush current only needs to be considered. One rule of thumb is to set the Over-Current threshold 2-3 times higher than the normal operating current.

$$I_{OC} = \frac{50mv}{R_{sense}} \quad \text{(EQ. 3)}$$

Physical layout of R1 SENSE resistor is critical to avoid the possibility of false over current events. Since it is in the main input-to-output path, the traces should be wide enough to support both the normal current, and up to the over-current trip point. Ideally trace routing between the R1 resistor and the ISL6141/51 (pin 4 (V_{EE}) and pin 5 (SENSE) is direct and as short as possible with zero current in the sense lines. (See Figure 24).

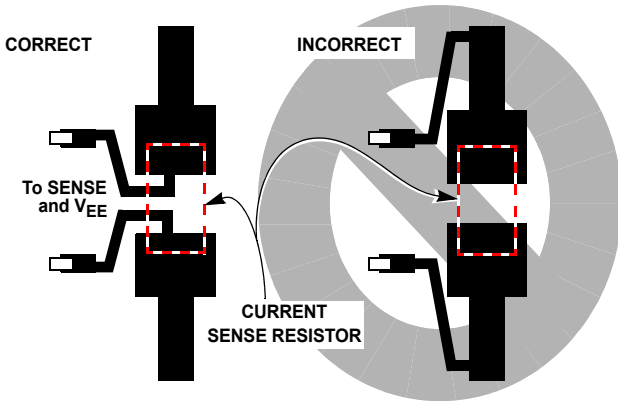

FIGURE 24. SENSE RESISTOR LAYOUT GUIDELINES

CL - is the sum of all load capacitances, including the load's input capacitance itself. Its value is usually determined by the needs of the load circuitry, and not the hot plug (although there can be interaction). For example, if the load is a regulator, then the capacitance may be chosen based on the input requirements of that circuit (holding regulation under current spikes or loading, filtering noise, etc.) The value chosen will affect the peak inrush current. Note that in the case of a regulator, there may be capacitors on the output of that circuit as well; these need to be added into the capacitance calculation during inrush (unless the regulator is delayed from operation by the PWRGD signal).

RL - is the equivalent resistive value of the load and determines the normal operation current delivered through the FET. It also affects some dynamic conditions (such as the discharge time of the load capacitors during a power-down). A typical value might be 48Ω (I = V/R = 48/48 = 1A).

R2, C1, R3, C2 - are related to the GATE driver, as it controls the inrush current.

R2 prevents high frequency oscillations; 10Ω is a typical value. **R2 = 10Ω**.

R3 and C2 act as a feedback network to control the inrush current as shown in equation 4 below, where CL is the load capacitance (including module input capacitance), and I_{PU} is the GATE pin charging current, nominally 50µA.

$$I_{inrush} = I_{PU} \times \frac{C_L}{C_2} \quad \text{(EQ. 4)}$$

Begin by choosing a value of acceptable inrush current for the system, and then solve for C2.

C1 and R3 prevent Q1 from turning on momentarily when power is first applied. Without them, C2 would pull the gate of Q1 up to a voltage roughly equal to V_{EE}*C2/Cgs(Q1) (where Cgs is the FET gate-source capacitance) before the ISL6141/2 could power up and actively pull the gate low. Place C1 in parallel with the gate capacitance of Q1; isolate them from C2 by R3.

C1= [(Vinmax - Vth)/Vth] * (C2+Cgd) - where Vth is the FET's minimum gate threshold, Vinmax is the maximum operating input voltage, and Cgd is the FET gate-drain capacitance.

R3 - its value is not critical, a typical value of 18kΩ is recommended but values down to 1KΩ can be used. Lower values of R3 will add delay to the gate turn-on for hot insertion and the single retry event following a hard fault.

Note that although this IC was designed for -48V systems, it can also be used as a low-side switch for positive 48V systems; the operation and components are usually similar. One possible difference is the kind of level shifting that may be needed to interface logic signals to the UV input (to reset the latch) or PWRGD output. For example, many of the IC functions are referenced to the IC substrate, connected to the V_{EE} pin. But this pin may be considered -48V or GND, depending upon the polarity of the system. And input or output logic (running at 5V or 3.3V or even lower) might be externally referenced to either V_{DD} or V_{EE} of the IC, instead of GND.

Inrush Current Control

The primary function of the ISL6141 hot plug controller is to control the inrush current. When a board is plugged into a live backplane, the input capacitors of the board's power supply circuit can produce large current transients as they charge up. This can cause glitches on the system power supply (which can affect other boards!), as well as possibly cause some permanent damage to the power supply.

The key to allowing boards to be inserted into a live backplane is to turn on the power to the board in a controlled manner, usually by limiting the current allowed to flow through a FET switch, until the input capacitors are fully charged. At that point, the FET is fully on, for the smallest voltage drop across it. Figure 25 below illustrates the typical inrush current response resulting from a hot insertion for the following conditions:

- V_{EE} = -48V, Rsense = 0.02Ω (2.5A current limit)
- C1 = 150nF, C2 = 3.3nF, R3 = 18kΩ
- I_{Inrush} = 50µA (100µF/3.3nF) = 1.5A
- C_L = 100uF, R_L = 150Ω (48V/150Ω = 320mA)

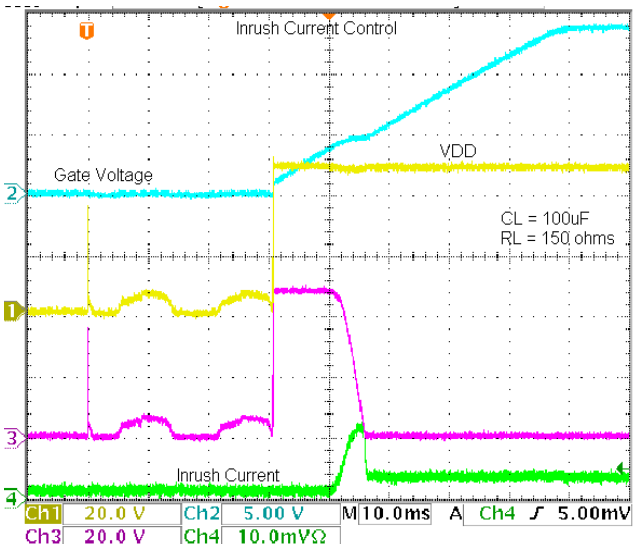

FIGURE 25. INRUSH CURRENT LIMITING FOR A HOT INSERTION

After the contact bounce subsides the UVLO and UV criteria are quickly met and the GATE begins to ramp up. As the GATE reaches approximately 4V with respect to the source, the FET begins to turn on allowing current to charge the load capacitor. As the drain to source voltage begins to drop, the feedback network of C2 and R3 hold the GATE constant, in this case limiting the current to approximately 1.3A. When the DRAIN voltage completes its ramp down the load current remains constant at 320mA as the GATE voltage increases to its final value.

Electronic Circuit Breaker/Current Limit

The ISL6141/51 features programmable current limiting with a fixed 600µs time-out period to protect against excessive supply or fault currents. The IntelliTrip™ electronic circuit breaker is capable of detecting both hard faults, and less severe Over-Current conditions.

The Over-Current trip point is determined by R1 (Eq. #3) also referred to as Rsense. When the voltage across this resistor exceeds 50mV, the current limit regulator will turn on, and the GATE will be pulled lower (to ~4V) to regulate current through the FET at 50mV/Rsense. If the fault persists and current limiting exceeds the 600µs time-out period, the FET will be turned off by discharging the GATE pin to V_{EE}. This will enable the Over-Current latch and the $\overline{PWRGD}$/PWRGD output will transition to the inactive state to indicate power is no longer good. To clear the latch and initiate a normal power-up sequence, the user must either power down the system (below the UVLO voltage), or toggle the UV pin below and above its threshold (usually with an external transistor). Figure 26 below shows the Over-Current shut down and current limiting response for a 10Ω short to ground on the output. With

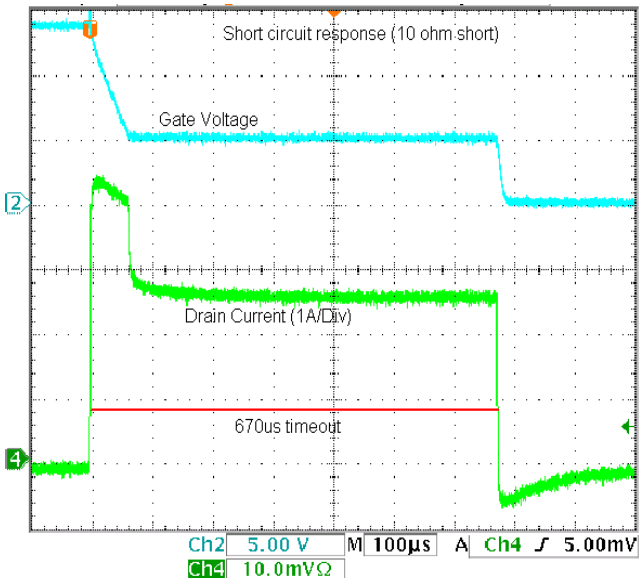

FIGURE 26. CURRENT LIMITING AND TIMEOUT

a 10Ω short and a -48V supply, the initial fault current is approximately 4.8A, producing a voltage drop across the 0.02Ω sense resistor of 95mV, roughly two times the Over-Current threshold of 50mV. This enables the 600µs timer and the GATE is quickly pulled low to limit the current to 2.5A (50mV/Rsense). The fault condition persists for the duration of the time-out period and the GATE is latched off in about 670µs. There is a short filter (3µs nominal) on the comparator, so current transients shorter than this will be ignored. Longer transients will initiate the GATE pull down, current limiting, and the timer. If the fault current goes away before the time-out period expires the device will exit the current limiting mode and resume normal operation.

In addition to the above current limit and 600µs time-out, there is a Hard Fault comparator to respond to short circuits with an immediate GATE shutdown (typically 10µs) and a single retry. The trip point of this comparator is set ~4 times (210mV) higher than the Over-Current threshold of 50mV. If the Hard Fault comparator trip point is exceeded, a hard pull down current (350mA) is enabled to quickly pull down the GATE and momentarily turn off the FET. The fast shutdown resets the 600µs timer and is followed by a soft start, single retry event. If the fault is still present after the GATE is slowly turned on, the current-limit regulator will trip (sense pin voltage > 50mV), turn on the timer, and limit the current to 50mV/Rsense for 600µs before latching the GATE pin low. Note: Since the 600µs timer starts when the SENSE pin exceeds the 50mV threshold, then depending on the speed of the current transient exceeding 200mV, it's possible that the current limit time-out and shutdown can occur before the Hard Fault comparator trips (and thus no retry). Figure 27 illustrates the Hard Fault response with a zero ohm short circuit at the output.

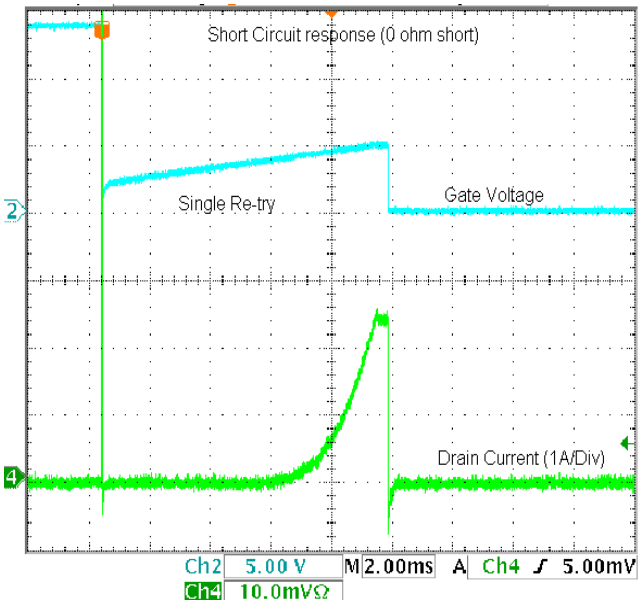

FIGURE 27. HARD FAULT SHUTDOWN AND RETRY

As in the Over-Current response discussed previously the supply is set at -48V and the current limit is set at 2.5A. After the initial gate shutdown (10µs) a soft start is initiated with the short circuit still present. As the GATE slowly turns on the current ramps up and exceeds the Over-Current threshold (50mV) enabling the timer and current limiting. The fault remains for the duration of the time-out period and the GATE pin is quickly pulled low and latched off requiring a UVLO or UV reset to resume normal operation (assuming the fault has gone away).

Applications: OV and UV

The UV and OV pins can be used to detect Over-Voltage and Under-Voltage conditions on the input supply and quickly shut down the external FET. Each pin is tied to an internal comparator with a nominal reference of 1.255V. A resistor divider between the V_{DD} (gnd) and V_{EE} is typically used to set the trip points on the UV and OV pins. If the voltage on the UV pin is above its threshold and the voltage on the OV pin is below its threshold, the supply is within its operating range and the GATE will be allowed to turn on, or remain on. If the UV pin voltage drops below its high to low threshold, or the OV pin voltage increases above its low to high threshold, the GATE pin will be pulled low, turning off the FET until the supply is back within tolerance.

The OV and UV inputs are high impedance, so the value of the external resistor divider is not critical with respect to input current. Therefore, the next consideration is total current; the resistors will always draw current, equal to the supply voltage divided by the total resistance of the divider (R4+R5+R6) so the values should be chosen high enough to get an acceptable current. However, to the extent that the noise on the power supply can be transmitted to the pins, the resistor values might be chosen to be lower. A filter capacitor from UV to V_{EE} or OV to V_{EE} is a possibility, if certain transients need to be filtered. (Note that even some transients which will momentarily shut off the GATE might recover fast enough such that the GATE or the output current does not even see the interruption).

Finally, take into account whether the resistor values are readily available, or need to be custom ordered. Tolerances of 1% are recommended for accuracy. Note that for a typical 48V system (with a 43V to 72V range), the 43V or 72V is being divided down to 1.255V, a significant scaling factor. For UV, the ratio is roughly 35 times; every 3mV change on the UV pin represents roughly 0.1V change of power supply voltage. Conversely, an error of 3mV (due to the resistors, for example) results in an error of 0.1V for the supply trip point. The OV ratio is around 60. So the accuracy of the resistors comes into play.

The hysteresis of the comparators is also multiplied by the scale factor of 35 for the UV pin (35 * 135mV = 4.7V of hysteresis at the power supply) and 60 for the OV pin (60 * 25mV = 1.5V of hysteresis at the power supply).

With the three resistors, the UV equation is based on the simple resistor divider:

$1.255 = V_{UV} * (R5 + R6)/(R4 + R5 + R6)$ or

$V_{UV} = 1.255 (R4 + R5 + R6)/(R5 + R6)$

Similarly, for OV:

$1.255 = V_{OV} * (R6)/(R4 + R5 + R6)$ or

$V_{OV} = 1.255 (R4 + R5 + R6)/(R6)$

Note that there are two equations, but 3 unknowns. Because of the scale factor, R4 has to be much bigger than the other two; chose its value first, to set the current (for example, 50V / 500kΩ draws 100µA), and then the other two will be in the 10kΩ range. Solve the two equations for two unknowns. Note that some iteration may be necessary to select values that

meet the requirement, and are also readily available standard values.

The three resistor divider (R4, R5, R6) is the recommended approach for most cases. But if acceptable values can't be found, then consider 2 separate resistor dividers (one for each pin, both from V_{DD} to V_{EE}). This also allows the user to adjust or trim either trip point independently. Some applications employ a short pin ground on the connector tied to R4 to ensure the hot plug device is fully powered up before the UV and OV pins (tied to the short pin ground) are biased. This ensures proper control of the GATE is maintained during power up. This is not a requirement for the ISL6141/51 however the circuit will perform properly if a short pin scheme is implemented (reference Figure 34).

Supply ramping

As previously mentioned the UV and OV pins can be used to detect under and Over-Voltage conditions on the input supply. Figures 28 and 29 illustrate the GATE shutdown response and the UV/OV hysteresis as a typical power supply is ramped from 0 to 80V, and then from 80V to 0V.

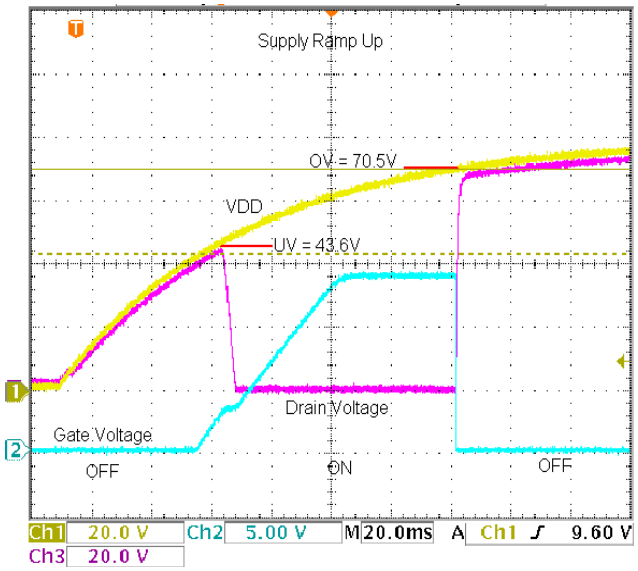

FIGURE 28. SUPPLY RAMP-UP

As the supply ramps up, the UV threshold is reached at 43.6V and the FET begins to turn on. Within 40ms the GATE is fully on and the device is operating normally. As the supply continues to ramp up the Over-Voltage threshold is exceeded at approximately 70.5V and the GATE is quickly shut down as expected. In figure 29 the GATE voltage begins in the off state as the supply voltage is above the OV set point. As the supply voltage decreases the GATE turns on at about 69V (roughly a 1.5 volt hysteresis). Some 800ms later (a characteristic of the supply used) the UV high to low threshold is met at approximately 38.5 volts (about 5.0V of hysteresis) and the GATE is shut off.

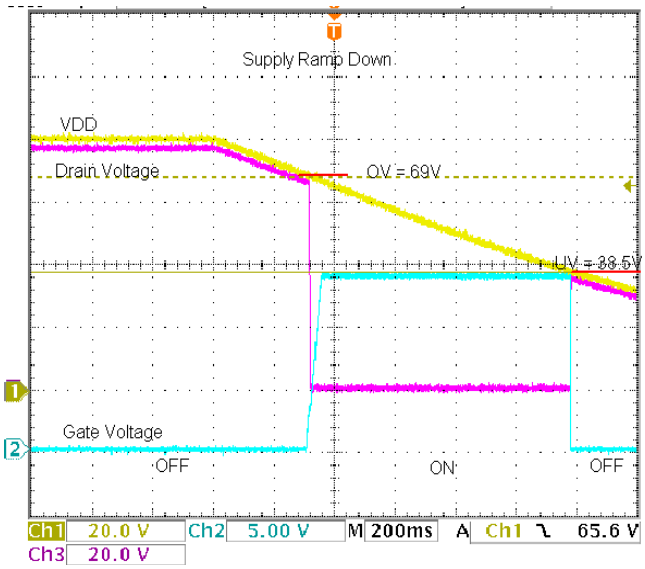

FIGURE 29. SUPPLY RAMP-DOWN

Applications: $\overline{PWRGD}$/PWRGD

The $\overline{PWRGD}$/PWRGD outputs are typically used to directly enable a power module, such as a DC/DC converter. The $\overline{PWRGD}$ (ISL6141) is used for modules with active low enable (L version), and PWRGD (ISL6151) for those with active high enable (H version). The modules usually have a pull-up device built-in, as well as an internal clamp. If not, an external pull-up resistor may be needed. If the pin is not used, it can be left open.

For both versions at initial start-up, when the DRAIN to V_{EE} voltage differential is less than 1.3V and the GATE voltage is within 2.5V (V_{GH}) of its normal operating voltage (13.6V), power is considered good and the $\overline{PWRGD}$/PWRGD pins will go active. At this point the output is latched and the DRAIN is no longer criticized. The latch is reset by any of the signals that shut off the GATE (Over-Voltage, Under-Voltage; Under-Voltage-Lock-Out; Over-Current Time-Out or powering down). In this case the $\overline{PWRGD}$/PWRGD output will go inactive, indicating power is no longer good.

ISL6141 (L version; Figure 30): Under normal conditions (DRAIN voltage - V_{EE} < V_{PG}, and ΔV_{GATE} - V_{GATE} < V_{GH}) the Q2 DMOS will turn on, pulling $\overline{PWRGD}$ low, enabling the module.

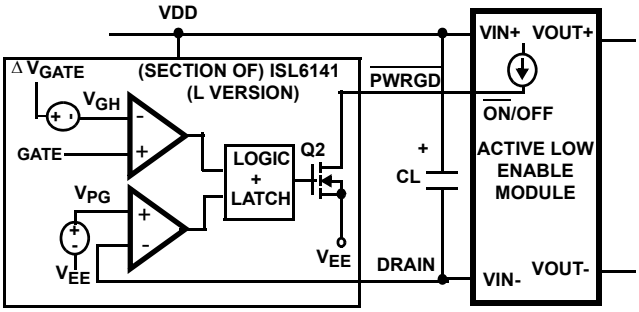

FIGURE 30. ACTIVE LOW ENABLE MODULE

When any of the 4 conditions occur that turn off the GATE (OV, UV, UVLO, Over-Current Time-Out) the PWRGD latch is reset and the Q2 DMOS device will shut off (high impedance). The pin will quickly be pulled high by the external module (or an optional pull-up resistor or equivalent) which in turn will disable it. If a pull-up resistor is used, it can be connected to any supply voltage that doesn't exceed the IC pin maximum ratings on the high end, but is high enough to give acceptable logic levels to whatever signal it is driving. An external clamp may be used to limit the voltage range.

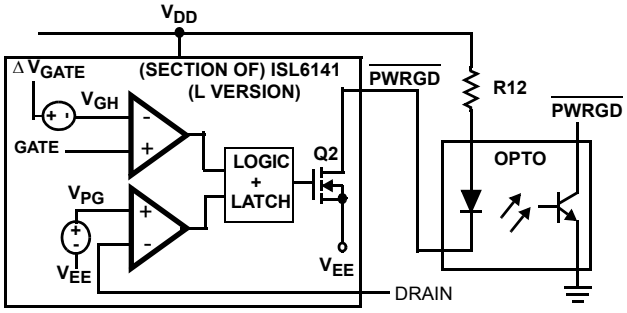

FIGURE 31. ACTIVE LOW ENABLE OPTO-ISOLATOR

The $\overline{PWRGD}$ can also drive an opto-coupler (such as a 4N25), as shown in Figure 31 or LED (Figure 32). In both cases, they are on (active) when power is good. Resistors R12 or R13 are chosen, based on the supply voltage, and the amount of current needed by the loads.

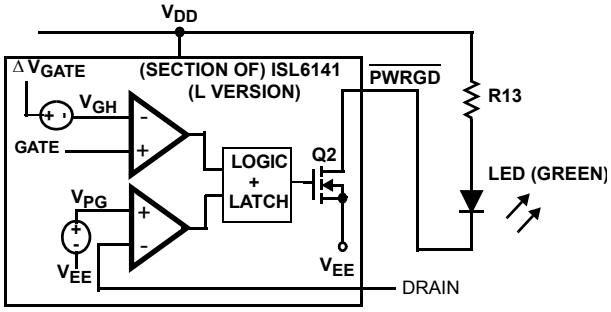

FIGURE 32. ACTIVE LOW ENABLE WITH LED

ISL6151 (H version; Figure 33): Under normal conditions (DRAIN voltage - V_{EE} < V_{PG}, and ΔV_{GATE} - V_{GATE} < V_{GH}), the Q3 DMOS will be on, shorting the bottom of the internal resistor to V_{EE}, and turning Q2 off. If the pull-up current from the external module is high enough, the voltage drop across the 6.2kΩ resistor will look like a logic high (relative to DRAIN). Note that the module is only referenced to DRAIN, not V_{EE} (but under normal conditions, the FET is on, and the DRAIN and V_{EE} are almost the same voltage).

When any of the 4 conditions occur that turn off the GATE, the Q3 DMOS turns off, and the resistor and Q2 clamp the PWRGD pin to one diode drop (~0.7V) above the DRAIN pin. This should be able to pull low against the module pull-up current, and disable the module.

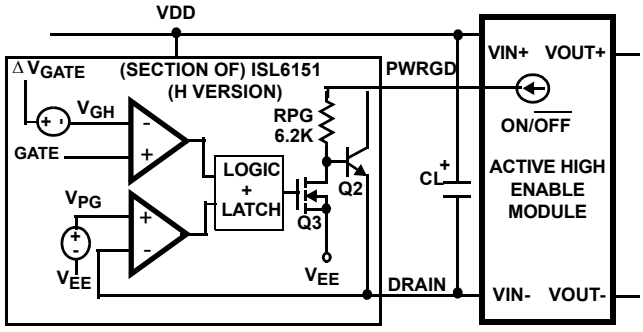

FIGURE 33. ACTIVE HIGH ENABLE MODULE

Applications: GATE pin

To help protect the external FET, the output of the GATE pin is internally clamped; up to an 80V supply and will not be any higher than 15V. Under normal operation when the supply voltage is above 20V, the GATE voltage will be regulated to a nominal 13.6V above V_{EE}.

Applications: "Brick" Regulators

One of the typical loads used are DC/DC regulators, some commonly known as "brick" regulators, (partly due to their shape, and because it can be considered a "building block" of a system). For a given input voltage range, there are usually whole families of different output voltages and current ranges. There are also various standardized sizes and pinouts, starting with the original "full" brick, and since getting smaller (half-bricks and quarter-bricks are now common).

Other common features may include: all components (except some filter capacitors) are self-contained in a molded plastic package; external pins for connections; and often an ENABLE input pin to turn it on or off. A hot plug IC, such as the ISL6141 is often used to gate power to a brick, as well as turn it on.

Many bricks have both logic polarities available (Enable Hi or Lo input); select the ISL6141 (L version) and ISL6151 (H version) to match. There is little difference between them, although the L version output is usually simpler to interface.

The Enable input often has a pull-up resistor or current source, or equivalent built in; care must be taken in the ISL6151 (H version) output that the given current will create a high enough input voltage (remember that current through the RPG 6.2kΩ resistor generates the high voltage level; see Figure 33).

The input capacitance of the brick is chosen to match its system requirements, such as filtering noise, and maintaining regulation under varying loads. Note that this input capacitance appears as the load capacitance of the ISL6141/51.

The brick's output capacitance is also determined by the system, including load regulation considerations. However, it can affect the ISL6141/51, depending upon how it is enabled. For example, if the PWRGD signal is not used to enable the brick, the following could occur. Sometime during the inrush current time, as the main power supply starts charging the brick input capacitors, the brick itself will start working, and start charging its output capacitors and load; that current has to be added to the inrush current. In some cases, the sum could exceed the Over-Current shutdown, which would shut down the whole system! Therefore, whenever practical, it is advantageous to use the PWRGD output to keep the brick off at least until the input caps are charged up, and then start-up the brick to charge its output caps.

Typical brick regulators include models such as Lucent JW050A1-E or Vicor VI-J30-CY. These are nominal -48V input, and 5V outputs, with some isolation between the input and output.

Applications: Optional Components

In addition to the typical application, and the variations already mentioned, there are a few other possible components that might be used in specific cases. See Figure 34 for some possibilities.

If the input power supply exceeds the 100V absolute maximum rating, even for a short transient, that could cause permanent damage to the IC, as well as other components on the board. If this cannot be guaranteed, a voltage suppressor (such as the SMAT70A, D1) is recommended. When placed from V_{DD} to V_{EE} on the board, it will clamp the voltage.

If transients on the input power supply occur when the supply is near either the OV or UV trip points, the GATE could turn on or off momentarily. One possible solution is to add a filter cap C4 to the V_{DD} pin, through isolation resistor R10. A large value of R10 is better for the filtering, but be aware of the voltage drop across it. For example, a 1kΩ resistor, with 2.4mA of I_{DD} would have 2.4V across it and dissipate 2.4mW. Since the UV and OV comparators are referenced with respect to the V_{EE} supply, they should not be affected. But the GATE clamp voltage could be offset by the voltage across the extra resistor.

The switch SW1 is shown as a simple push button. It can be replaced by an active switch, such as an NPN or NFET; the principle is the same; pull the UV node below its trip point, and then release it (toggle low). To connect an NFET, for example, the DRAIN goes to UV; the source to V_{EE}, and the GATE is the input; if it goes high (relative to V_{EE}), it turns the NFET on, and UV is pulled low. Just make sure the NFET resistance is low compared to the resistor divider, so that it has no problem pulling down against it.

R8 is a pull-up resistor for $\overline{\text{PWRGD}}$, if there is no other component acting as a pull-up device. The value of R8 is determined by how much current is needed when the pin is pulled low (also affected by the V_{DD} voltage); and it should be pulled low enough for a good logic low level. An LED can also be placed in series with R8, if desired. In that case, the criteria is the LED brightness versus current.

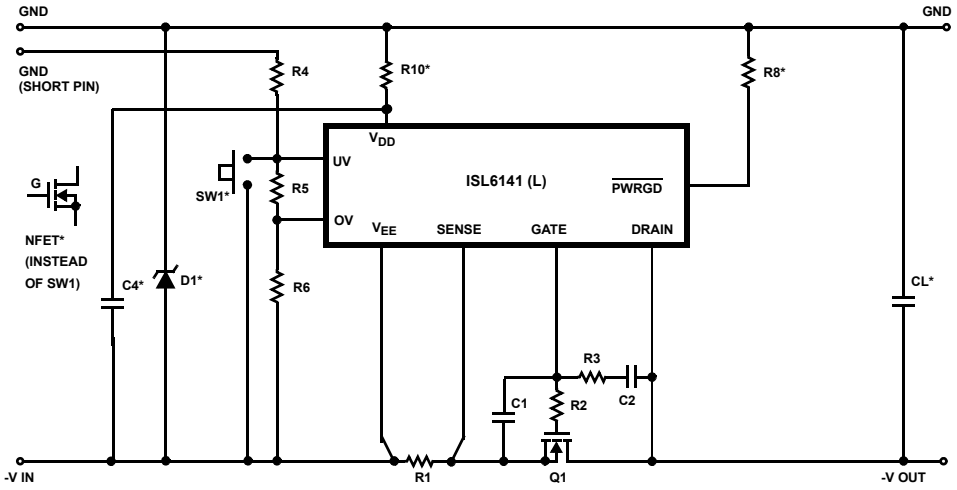

FIGURE 34. ISL6141/51 OPTIONAL COMPONENTS (SHOWN WITH *)

Applications: Layout Considerations

For the minimum application, there are only 6 resistors, 2 capacitors, one IC and one FET. A sample layout is shown in Figure 35. It assumes the IC is 8-SOIC; the FET is in a D2PAK (or similar SMD-220 package).

Although GND planes are common with multi-level PCBs, for a -48V system, the -48V rails (both input and output) act more like a GND than the top 0V rail (mainly because the IC signals are mostly referenced to the lower rail). So if separate planes for each voltage are not an option, consider prioritizing the bottom rails first.

Note that with the placement shown, most of the signal lines are short, and there should not be minimal interaction between them.

Although decoupling capacitors across the IC supply pins are often recommended in general, this application may not need one, nor even tolerate one. For one thing, a decoupling cap would add to (or be swamped out by) any other input capacitance; it also needs to be charged up when power is applied. But more importantly, there are no high speed (or any) input signals to the IC that need to be conditioned. If still desired, consider the isolation resistor R10, as shown in Figure 34.

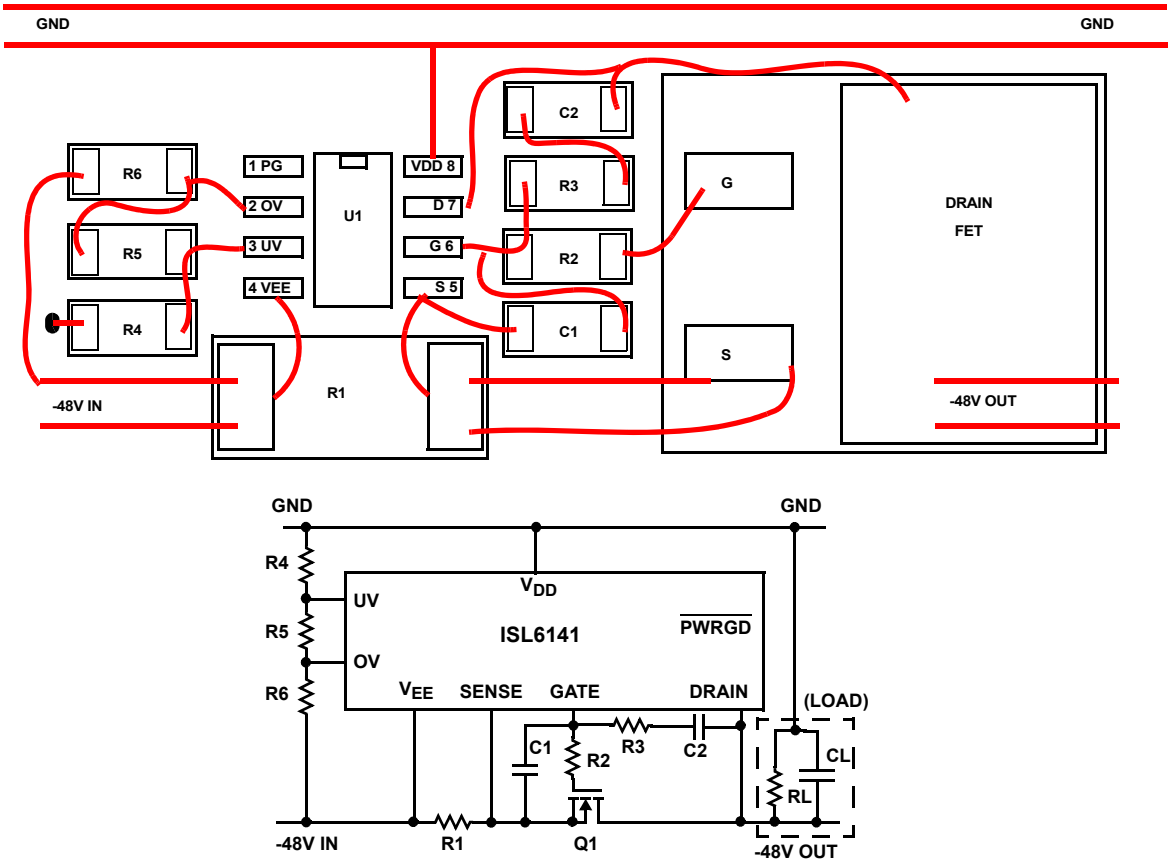

FIGURE 35. ISL6141/51 SAMPLE LAYOUT (NOT TO SCALE)

NOTES:

1. Layout scale is approximate; routing lines are just for illustration purposes; they do not necessarily conform to normal PCB design rules. High current buses are wider, shown with parallel lines.
2. Approximate size of the above layout is 1.6 x 0.6 inches; almost half of the area is just the FET (D2PAK or similar SMD-220 package).
3. R1 sense resistor is size 2512; all other R's and C's shown are 0805; they can all potentially use smaller footprints, if desired.
4. The RL and CL are not shown on the layout.
5. R4 uses a via to connect to GND on the bottom of the board; all other routing can be on top level. (It's even possible to eliminate the via, for an all top-level route).
6. $\overline{\text{PWRGD}}$ signal is not used here.

BOM (Bill Of Materials)

R1 = 0.02Ω (5%)
R2 = 10Ω (5%)
R3 = 18kΩ (5%)
R4 = 549kΩ (1%)
R5 = 6.49kΩ (1%)
R6 = 10kΩ (1%)
C1 = 150nF (25V)
C2 = 3.3nF (100V)
Q1 = IRF530 (100V, 17A, 0.11Ω)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Novmeber 9, 2015	FN9079.2	Updated the Ordering Information on page 2. Added Revision History and About Intersil sections. Updated POD (Package Outline Drawing) M18.15 to the latest revision. -Revision 0 to Revision 1 changes - Remove “u” symbol from drawing (overlaps the “a” on Side View). -Revision 1 to Revision 2 changes - Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern -Revision 2 to Revision 3 changes - Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 changes - Changed Note 1 “1982” to “1994”.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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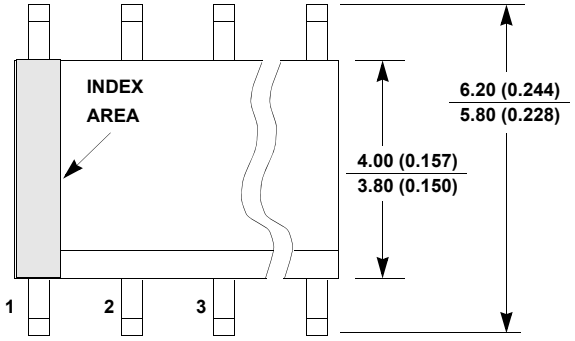
Package Outline Drawing

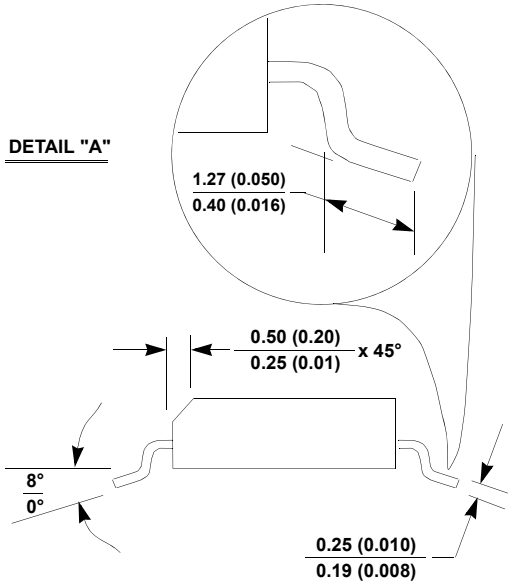
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

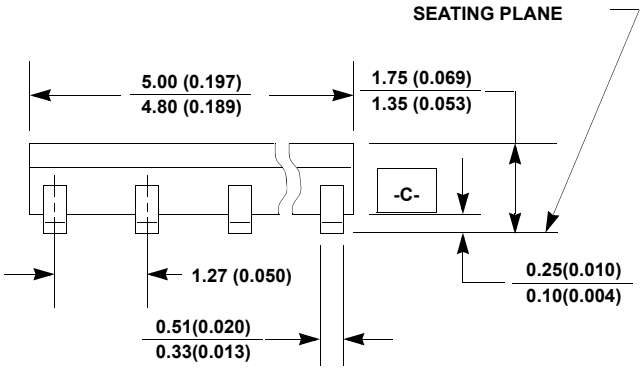
Rev 4, 1/12



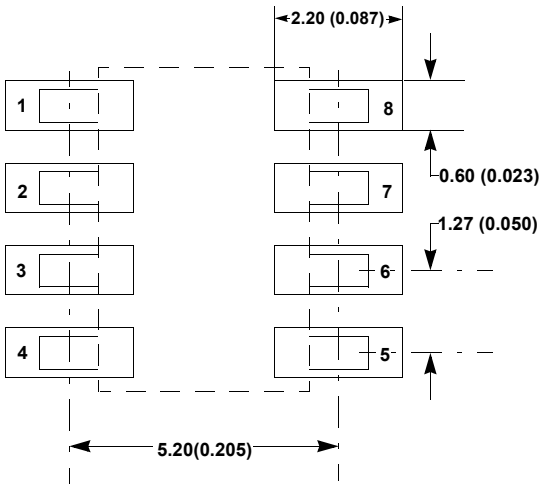
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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