Pin Configuration

9DB833

Pin Name	Pin	Pin	Pin Name
SRC_DIV#	1	48	VDDA
VDDR	2	47	GNDA
GND	3	46	IREF
SRC_IN	4	45	LOCK
SRC_IN#	5	44	**OE7#**
OE0#	6	43	**OE4#**
OE3#	7	42	DIF_7
DIF_0	8	41	DIF_7#
DIF_0#	9	40	**PD#**
GND	10	39	VDD
VDD	11	38	DIF_6
DIF_1	12	37	DIF_6#
DIF_1#	13	36	**OE6#**
OE1#	14	35	**OE5#**
OE2#	15	34	DIF_5
DIF_2	16	33	DIF_5#
DIF_2#	17	32	GND
GND	18	31	VDD
VDD	19	30	DIF_4
DIF_3	20	29	DIF_4#
DIF_3#	21	28	**SMB_ADR_tri**
BYP#_HIBW_LOBW	22	27	**VDD**
SMBCLK	23	26	**GND**
SMBDAT	24	25	GND

Notes:

Highlighted Pins are the differences between 9DB803 and 9DB833.

Pin 22 and Pin 28 are latched on power up. Please make sure that the power supply to the pullup/pulldown resistors ramps at the same time as the main supply to the chip.

Operating Mode Readback Table

BYP#_LOBW_HIBW	MODE	Byte0, bit 3	Byte 0 bit 1
Low	Bypass	0	0
Mid	PLL 100M Hi BW	1	0
High	PLL 100M Low BW	0	1

Power Connections

Pin Number		Description
VDD	GND	
2	3	SRC_IN/SRC_IN#
11,19,31,39	10,18, 25,32	DIF(7:0)
27	26	DIGITAL VDD/GND
48	47	Analog VDD/GND for PLL in IREF

For best results, treat pin 2 as analog VDD.

SMBus Address Selection and Readback

SMB_ADR_tri	Address
Low	DA/DB
Mid	DC/DD
High	D8/D9

Tri-level Input Logic Levels

State of Pin	Voltage
Low	<0.8V
Mid	1.2<Vin<1.8V
High	Vin > 2.0V

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	SRC_DIV#	IN	Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC
2	VDDR	PWR	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
3	GND	GND	Ground pin.
4	SRC_IN	IN	HCSL SRC TRUE input
5	SRC_IN#	IN	HCSL SRC COMPLEMENTARY input
6	OE0#	IN	Active low input for enabling output 0. 1 = disable output, 0 = enable output.
7	OE3#	IN	Active low input for enabling output 3. 1 = disable output, 0 = enable output.
8	DIF_0	OUT	HCSL true clock output.
9	DIF_0#	OUT	HCSL complementary clock output.
10	GND	GND	Ground pin.
11	VDD	PWR	Power supply, nominally 3.3V.
12	DIF_1	OUT	HCSL true clock output.
13	DIF_1#	OUT	HCSL complementary clock output.
14	OE1#	IN	Active low input for enabling output 1. 1 = disable output, 0 = enable output.
15	OE2#	IN	Active low input for enabling output 2. 1 = disable output, 0 = enable output.
16	DIF_2	OUT	HCSL true clock output.
17	DIF_2#	OUT	HCSL complementary clock output.
18	GND	GND	Ground pin.
19	VDD	PWR	Power supply, nominally 3.3V.
20	DIF_3	OUT	HCSL true clock output.
21	DIF_3#	OUT	HCSL complementary clock output.
22	BYP#_HIBW_LOBW	IN	Tri-level input to select bypass mode, Hi BW PLL, or Lo BW PLL mode
23	SMBCLK	IN	Clock pin of SMBUS circuitry
24	SMBDAT	I/O	Data pin of SMBUS circuitry

Pin Descriptions (cont.)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	GND	GND	Ground pin.
26	GND	GND	Ground pin.
27	VDD	PWR	Power supply, nominally 3.3V.
28	SMB_ADR_tri	IN	SMBus address select bit. This is a tri-level input that decodes 1 of 3 SMBus Addresses.
29	DIF_4#	OUT	HCSL complementary clock output.
30	DIF_4	OUT	HCSL true clock output.
31	VDD	PWR	Power supply, nominally 3.3V.
32	GND	GND	Ground pin.
33	DIF_5#	OUT	HCSL complementary clock output.
34	DIF_5	OUT	HCSL true clock output.
35	OE5#	IN	Active low input for enabling output 5. 1 = disable output, 0 = enable output.
36	OE6#	IN	Active low input for enabling output 6. 1 = disable output, 0 = enable output.
37	DIF_6#	OUT	HCSL complementary clock output.
38	DIF_6	OUT	HCSL true clock output.
39	VDD	PWR	Power supply, nominally 3.3V.
40	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO's (if any) and the XTAL oscillator are stopped.
41	DIF_7#	OUT	HCSL complementary clock output.
42	DIF_7	OUT	HCSL true clock output.
43	OE4#	IN	Active low input for enabling output 4 1 = disable output, 0 = enable output.
44	OE7#	IN	Active low input for enabling output 7. 1 = disable output, 0 = enable output.
45	LOCK	OUT	3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.
46	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
47	GNDA	GND	Ground pin for the PLL core.
48	VDDA	PWR	Power supply for PLL core.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DB833. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA/R				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.
[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–DIF_IN Clock Input Parameters

T_{AMB}=T_{COM} or T_{IND} unless otherwise indicated, supply voltages per normal operation conditions; see Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150	375	900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.6		8	V/ns	1,2
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.
[2] Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Current Consumption

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, PLL Mode, C_L = Full load;		164	200	mA	1
Powerdown Current	$I_{DD3.3PD}$	All diff pairs driven		53	60	mA	1
	$I_{DD3.3PDZ}$	All differential pairs tri-stated		3	6	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commercial range	0		70	°C	1
	T_{IND}	Industrial range	-40		85	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5	-0.02	5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	5		166	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	50	100	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30	31.5	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	2	3	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		13	300	us	1,3
Tfall	t_F	Fall time of control inputs			5	ns	1,2
Trise	t_R	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			440	kHz	1,5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Electrical Characteristics–DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM}$ or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1.5	2.8	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		8	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	797	850	mV	1
Voltage Low	VLow		-150	14	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		813	1150	mV	1
Min Voltage	Vmin		-300	-1			1
Vswing	Vswing	Scope averaging off (Differential)	300	1596.9		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	378	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		16	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. IREF = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode (T_{IND})	1.5	2.8	4.1	MHz	1
		-3dB point in High BW Mode (T_{COM})	2	2.8	4	MHz	1
		-3dB point in Low BW Mode	0.7	1.1	1.4	MHz	1
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain		1.5	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	49.2	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-2	-0.4	2	%	1,4
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50% (T_{IND})	3500	4263	4900	ps	1
		Bypass Mode, V_T = 50% (T_{COM})	3500	4115	4500	ps	1,5
	t_{pdPLL}	PLL Mode V_T = 50%	-250	-45	250	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%		40.0	50/60	ps	1,5
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		21	50	ps	1,3
		Additive Jitter in Bypass Mode		3	10	ps	1,3

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[3] Measured from differential waveform

[4] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[5] First number is commercial temp, second number is industrial temp.

Electrical Characteristics–PCIe Phase Jitter Parameters

TA = T_{COM} or $T_{IND;}$ Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1		26	40	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1	1.2	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2	1.8	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	0.6	1	ps (rms)	1,2
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1}$	PCIe Gen 1		2.6	5	N/A	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.06	0.2	N/A	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)			0.3	N/A	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)			0.1	N/A	ps (rms)	1,2

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

Clock Periods Differential Outputs Tracking Spread Spectrum

Measurement Window	1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol	**Lg-**	**-SSC**	**-ppm error**	**0ppm**	**+ ppm error**	**+SSC**	**Lg+**		
Definition	**Absolute Period**	**Short-term Average**	**Long-Term Average**	**Period**	**Long-Term Average**	**Short-term Average**	**Period**		
	Minimum Absolute Period	**Minimum Absolute Period**	**Minimum Absolute Period**	**Nominal**	**Maximum**	**Maximum**	**Maximum**	**Units**	**Notes**
DIF 100	9.949	9.999	10.024	10.025	10.026	10.051	10.101	ns	1,2,3

Output Termination and Layout Information			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

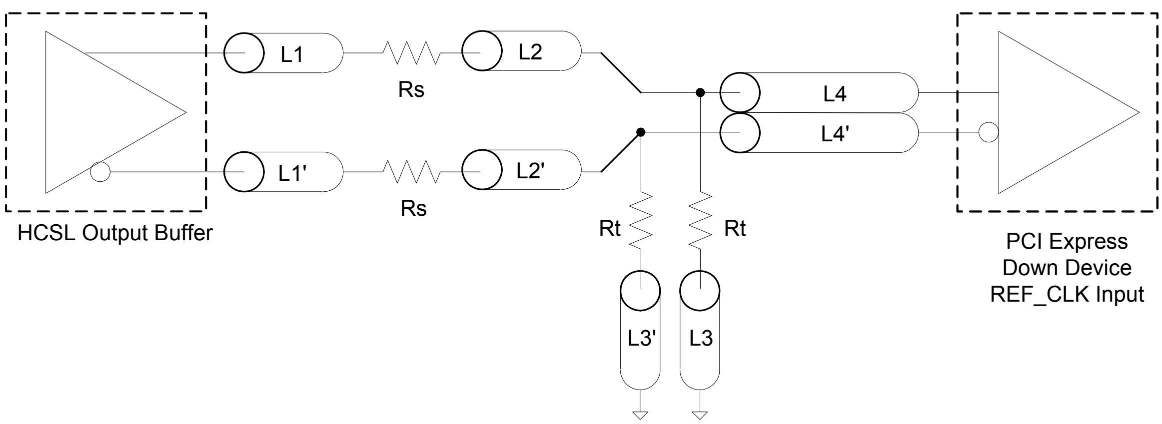
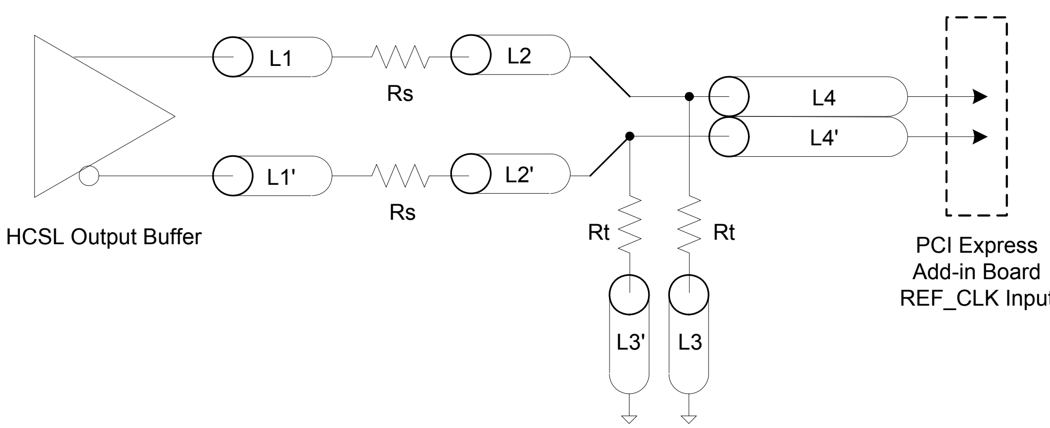


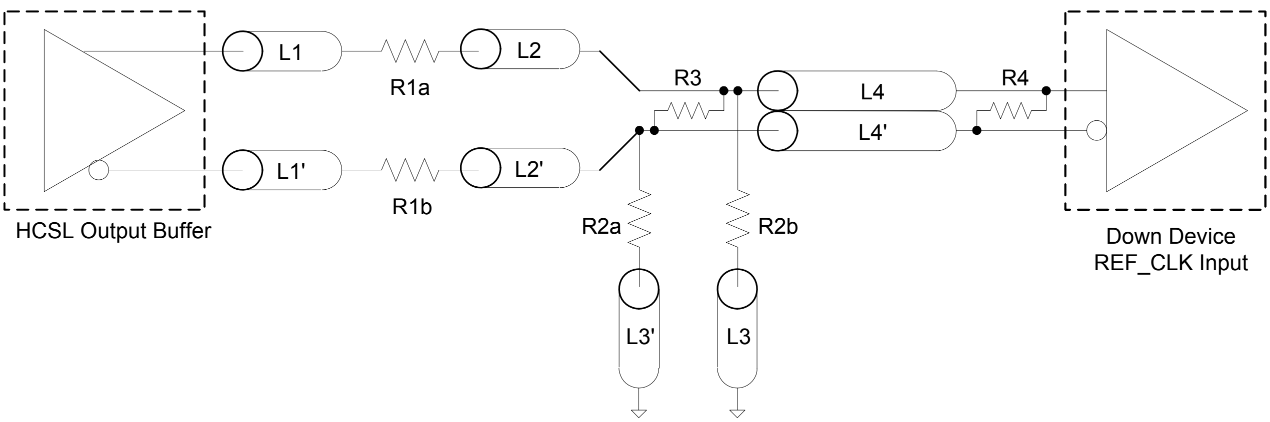
Figure 2: Differential Routing to PCI Express Controller



Termination for LVDS and other Common Differential Signals (figure 3)							
Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

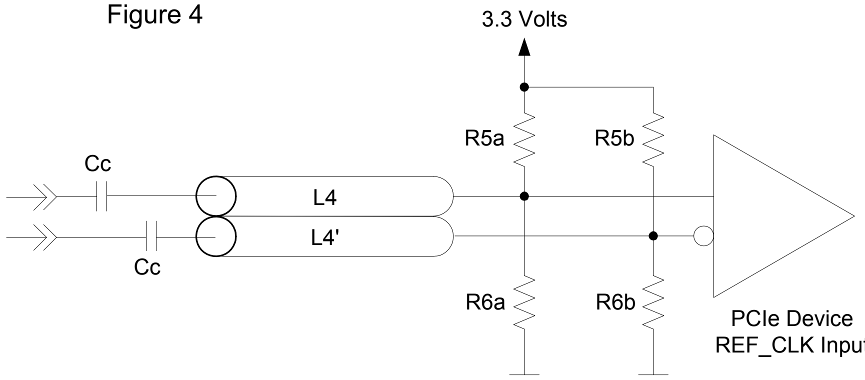
R1a = R1b = R1
R2a = R2b = R2

Figure 3



Termination for Cable AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 µF	
Vcm	0.350 volts	

Figure 4



General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address*
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

* Assuming SMB_ADR_tri is at mid-level

Read Address	Write Address
$DD_{(H)}$	$DC_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address*
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address*
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (Selectable)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	PD_Mode	PD# drive mode	RW	driven	Hi-Z	1
Bit 6	-	OE_Mode	OE#_Stop drive mode	RW	driven	Hi-Z	0
Bit 5	-		Reserved				0
Bit 4	-		Reserved				X
Bit 3	-	MODE1	BYPASS#/PLL1	RW	See Operating Mode Readback Table		Latched
Bit 2	-		Reserved				1
Bit 1	-	MODE0	BYPASS#/PLL0	RW	See Operating Mode Readback Table		Latched
Bit 0	-	SRC_DIV#	SRC Divide by 2 Select	RW	x/2	x/1	1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42,41	DIF_7	Output Enable	RW	Disable	Enable	1
Bit 6	38,37	DIF_6	Output Enable	RW	Disable	Enable	1
Bit 5	34,33	DIF_5	Output Enable	RW	Disable	Enable	1
Bit 4	30,29	DIF_4	Output Enable	RW	Disable	Enable	1
Bit 3	20,21	DIF_3	Output Enable	RW	Disable	Enable	1
Bit 2	16,17	DIF_2	Output Enable	RW	Disable	Enable	1
Bit 1	12,13	DIF_1	Output Enable	RW	Disable	Enable	1
Bit 0	8,9	DIF_0	Output Enable	RW	Disable	Enable	1

NOTE: The SMBus Output Enable Bit must be '1' AND the respective OE pin must be active for the output to run.

SMBus Table: OE Pin Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42,41	DIF_7	DIF_7 Stoppable with OE7#	RW	Free-run	Stoppable	0
Bit 6	38,37	DIF_6	DIF_6 Stoppable with OE6#	RW	Free-run	Stoppable	0
Bit 5	34,33	DIF_5	DIF_5 Stoppable with OE5#	RW	Free-run	Stoppable	0
Bit 4	30,29	DIF_4	DIF_4 Stoppable with OE4#	RW	Free-run	Stoppable	0
Bit 3	20,21	DIF_3	DIF_3 Stoppable with OE3#	RW	Free-run	Stoppable	0
Bit 2	16,17	DIF_2	DIF_2 Stoppable with OE2#	RW	Free-run	Stoppable	0
Bit 1	12,13	DIF_1	DIF_1 Stoppable with OE1#	RW	Free-run	Stoppable	0
Bit 0	8,9	DIF_0	DIF_0 Stoppable with OE0#	RW	Free-run	Stoppable	0

NOTE: If you wish the default to be "Stoppable" see the 9DB834.

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				X
Bit 6			Reserved				X
Bit 5			Reserved				X
Bit 4			Reserved				X
Bit 3			Reserved				X
Bit 2			Reserved				X
Bit 1			Reserved				X
Bit 0			Reserved				X

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	DID7	Device ID 7 (MSB)	RW	Device ID is 83 Hex for 9DB833		1
Bit 6	-	DID6	Device ID 6	RW			0
Bit 5	-	DID5	Device ID 5	RW			0
Bit 4	-	DID4	Device ID 4	RW			0
Bit 3	-	DID3	Device ID 3	RW			0
Bit 2	-	DID2	Device ID 2	RW			0
Bit 1	-	DID1	Device ID 1	RW			1
Bit 0	-	DID0	Device ID 0	RW			1

SMBus Table: Byte Count Register

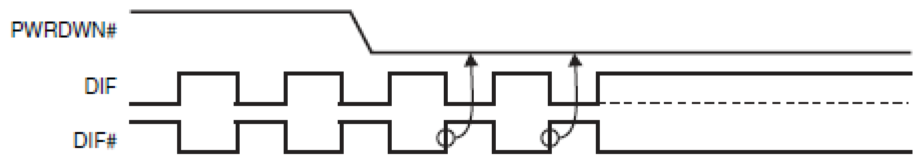
Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

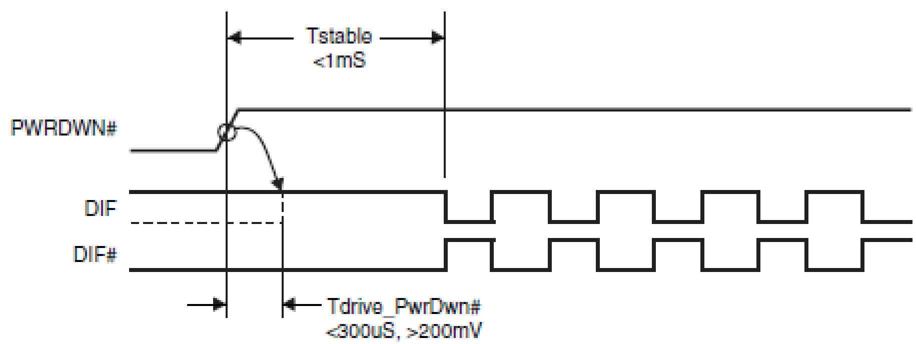
PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with 2 x I_{REF} and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.



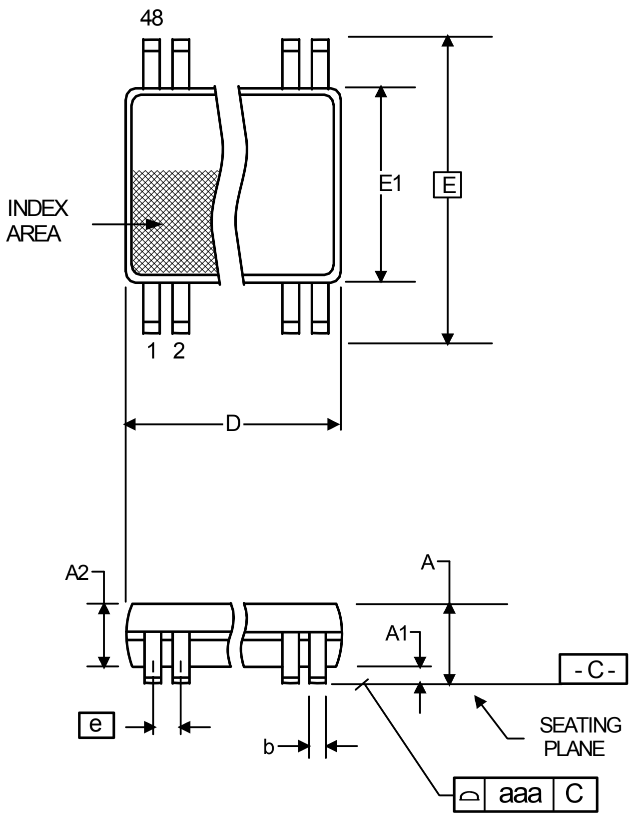
PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300µs of PD# de-assertion.



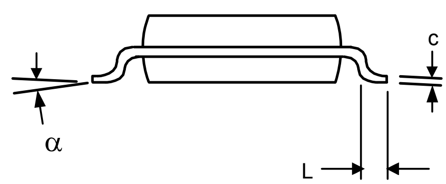
Package Outline Drawings (48-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95



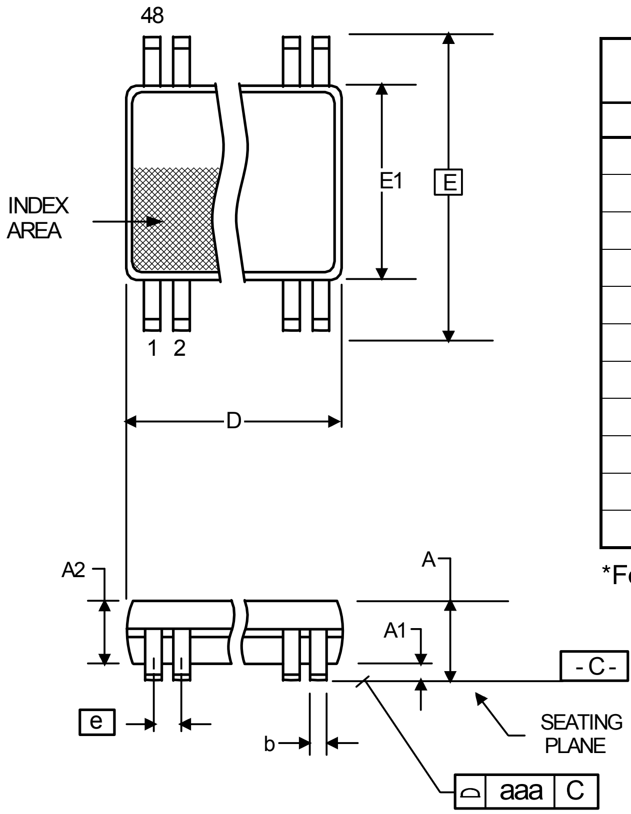
	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.0035	0.008
D	12.40	12.60	0.488	0.496
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	0.236	0.244
e	0.50 Basic		0.020 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.



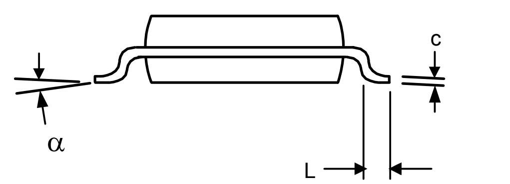
Package Outline Drawings (48-pin SSOP)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	15.75	16.00	.620	.630
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DB833AFLF	Tubes	48-pin SSOP	0 to +70°C
9DB833AFLFT	Tape and Reel	48-pin SSOP	0 to +70°C
9DB833AGLF	Tubes	48-pin TSSOP	0 to +70°C
9DB833AGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C
9DB833AFILF	Tubes	48-pin SSOP	-40 to +85°C
9DB833AFILFT	Tape and Reel	48-pin SSOP	-40 to +85°C
9DB833AGILF	Tubes	48-pin TSSOP	-40 to +85°C
9DB833AGILFT	Tape and Reel	48-pin TSSOP	-40 to +85°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Issue Date	Description	Page #
6/30/2010	Released to final	
5/9/2011	1. Update pin 2 pin-name and pin description from VDD to VDDR. This highlights that optimal performance is obtained by treating VDDR as in analog pin. This is a document update only, there is no silicon change.	Various
5/24/2011	1. Corrected pin description of Pins 27/28 2. Corrected orderable part number for 9DB833AGILFT	
3/13/2012	1. Added additional line to PLL Bandwidth "-3dB point in High BW Mode" conditions for industrial mode (min1.5, typ 2.7, max 4.1 MHz) 2. Added additional line to Skew, Input to Output "Bypass Mode" conditions for industrial mode (min 2500, max 4900 ps)	6
7/5/2012	1. Changed references of PCIe Gen3 to PCIe Gen1,2,3 2. Corrected Power Connections Table - pinout was/is correct.	1, 2
9/18/2012	Updated Byte 2, bits 1, 2, 5 and 6 per char review. Outputs can be programmed with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE pins.	12
8/25/2015	1. Added note to Byte 2 referring to 9DB434 if FFhex is the desired default.	12
6/7/2016	1. Updated typical values in electrical tables. 2. Updated clock input electrical table to latest format. 3. Updated SMbus operating frequency to 440KHz. 4. Corrected typo in Byte 0, bit 6 defaults to 0.	Various
5/25/2018	1. Updated the minimum input slew rate from 1 V/ns to 0.6V/ns.	6

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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