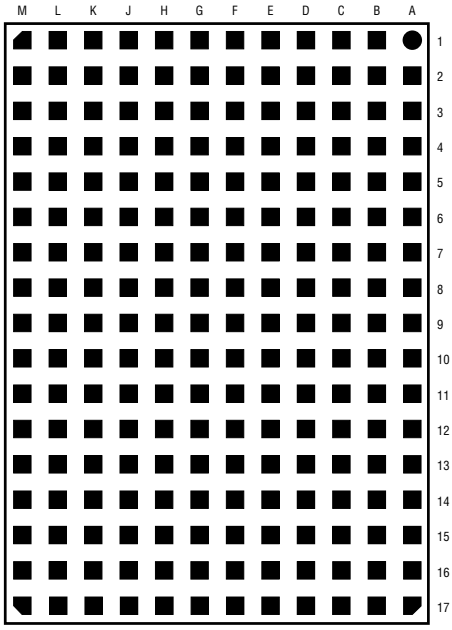
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC1}, V_{CC2}) ..... –0.3V to 5.5V
Supply Voltage (V_{CC3}, LTM9004-AA, LTM9004-AB) ..... –0.3V to 5.5V
Supply Voltage (V_{CC3}, LTM9004-AC, LTM9004-AD) ..... –0.3V to 3.5V
Supply Voltage (V_{DD}, OV_{DD}) ..... –0.3V to 4.0V
Digital Output Ground Voltage (OGND) ..... –0.3V to 1V
LO Input Power 10dBm
RF Input Power 20dBm
RF Input DC Voltage ..... ±0.1V
LO Input DC Voltage ..... ±0.1V
x_ADJ Input Voltage ..... –0.3V to V_{CC1}, V_{CC2}
SENSE Input Voltage ..... –0.3V to V_{DD}
Digital Input Voltage (MIXENABLE) ..... –0.3V to (V_{CC1} + 0.3V)
Digital Input Voltage (AMP1ENABLE) ..... –0.3V to (V_{CC2} + 0.3V)
Digital Input Voltage (AMP2ENABLE) ..... –0.3V to (V_{CC3} + 0.3V)
Digital Input Voltage (except MIXENABLE and AMPxENABLE) ..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range
  LTM9004C ..... 0°C to 70°C
  LTM9004I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
204-LEAD (22mm × 15mm × 2.91mm)
T_{JMAX} = 125°C, θ_{JA} = 18.2°C/W, θ_{JCtop} = 9.9°C/W, $\theta_{JCbottom}$ = 6.9°C/W, θ_{JB} = 7.1°C/W, VALUES DETERMINED PER JEDEC 51-9, 51-12, WEIGHT = 1.9g

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the RF and LO inputs of the LTM9004.

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9004CV-AA#PBF	LTM9004CV-AA#PBF	LTM9004V AA	204-Lead (15mm × 22mm × 2.91mm) LGA	0°C to 70°C
LTM9004IV-AA#PBF	LTM9004IV-AA#PBF	LTM9004V AA	204-Lead (15mm × 22mm × 2.91mm) LGA	–40°C to 85°C
LTM9004CV-AB#PBF	LTM9004CV-AB#PBF	LTM9004V AB	204-Lead (15mm × 22mm × 2.91mm) LGA	0°C to 70°C
LTM9004IV-AB#PBF	LTM9004IV-AB#PBF	LTM9004V AB	204-Lead (15mm × 22mm × 2.91mm) LGA	–40°C to 85°C
LTM9004CV-AC#PBF	LTM9004CV-AC#PBF	LTM9004V AC	204-Lead (15mm × 22mm × 2.91mm) LGA	0°C to 70°C
LTM9004IV-AC#PBF	LTM9004IV-AC#PBF	LTM9004V AC	204-Lead (15mm × 22mm × 2.91mm) LGA	–40°C to 85°C
LTM9004CV-AD#PBF	LTM9004CV-AD#PBF	LTM9004V AD	204-Lead (15mm × 22mm × 2.91mm) LGA	0°C to 70°C
LTM9004IV-AD#PBF	LTM9004IV-AD#PBF	LTM9004V AD	204-Lead (15mm × 22mm × 2.91mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V, V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB), P_{LO} = 0dBm. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	RF Input Frequency Range	No External Matching (High Band) With External Matching (Low Band, Mid Band)			1.5 to 2.7 0.7 to 1.5		GHz GHz
	LO Input Frequency Range	No External Matching (High Band) With External Matching (Low Band, Mid Band)			1.5 to 2.7 0.7 to 1.5		GHz GHz
	Baseband Frequency Range	LTM9004-AA LTM9004-AB LTM9004-AC LTM9004-AD			DC to 1.92 DC to 4.42 DC to 9.42 DC to 20		MHz MHz MHz MHz
	RF Input Return Loss	Z_0 = 50Ω, 1.5GHz to 2.7GHz, Internally Matched			>10		dB
	LO Input Return Loss	Z_0 = 50Ω, 1.5GHz to 2.7GHz, Internally Matched			>10		dB
	RF Input Power for –1dBFS	RF = 1950MHz			–7.3		dBm
	LO Input Power				–13 to 5		dBm
	I/Q Gain Mismatch				0.2		dB
	I/Q Phase Mismatch				1.5		Deg
	LO to RF Leakage	RF = 900MHz RF = 1900MHz			–60.8 –64.6		dBm dBm
	RF to LO Isolation	RF = 900MHz RF = 1900MHz			59.7 57.1		dB dB
	Maximum DC Offset Voltage, No RF	(Note 5)			35		mV
	DC Offset Variation	–40°C to 85°C			210		µV/°C
	Gain Flatness	DC to 1.92MHz (LTM9004-AA) DC to 4.42MHz (LTM9004-AB) DC to 9.42MHz (LTM9004-AC) DC to 20MHz (LTM9004-AD)			0.2 0.2 0.2 0.3		dB dB dB dB
	Group Delay Flatness	DC to 1.92MHz (LTM9004-AA) DC to 4.42MHz (LTM9004-AB) DC to 9.42MHz (LTM9004-AC) DC to 20MHz (LTM9004-AD)			15 15 15 5		nsec nsec nsec nsec
	Rejection	LTM9004-AA 5MHz 10MHz			 5.3 33.5		 dB dB
		LTM9004-AB 7.5MHz 12.5MHz			 1 11		 dB dB
		LTM9004-AC 12.5MHz 17.5MHz			 0.5 1		 dB dB
		LTM9004-AD 30MHz 40MHz			 1.5 5.5		 dB dB
f_{LPF}	Lowpass Filter Cutoff Frequency	1dB Point (LTM9004-AA) 1dB Point (LTM9004-AB) 1dB Point (LTM9004-AC) 1dB Point (LTM9004-AD)			4 6.3 15 28		MHz MHz MHz MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V, V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB), P_{LO} = 0dBm.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IIP3	Input 3rd-Order Intercept, 1 Tone				22		dBm
IIP2	Input 2nd-Order Intercept, 1 Tone				58		dBm
SNR	Signal-to-Noise Ratio at –1dBFS	1.92MHz (LTM9004-AA) 4.42MHz (LTM9004-AB) 9.42MHz (LTM9004-AC) 20MHz (LTM9004-AD)	● ● ● ●	70.6 69.7 70.3 66.3	76.1 75.2 72 68.9		dB/1.92MHz dB/4.42MHz dB/9.42MHz dB/20MHz
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic at –1dBFS	LTM9004-AA RF = 1950.5MHz, LO =1950MHz	●	50	63.5		dB
		LTM9004-AB RF = 1951MHz, LO =1950MHz	●	50	65		dB
		LTM9004-AC RF = 1952.5MHz, LO =1950MHz	●	52.5	66		dB
		LTM9004-AD RF = 1955MHz, LO =1950MHz	●	55	64		dB
SFDR	Spurious Free Dynamic Range 4th or Higher at –1dBFS	LTM9004-AA RF = 1950.5MHz, LO =1950MHz	●	65	88		dB
		LTM9004-AB RF = 1951MHz, LO =1950MHz	●	70	91		dB
		LTM9004-AC RF = 1952.5MHz, LO =1950MHz	●	70	89		dB
		LTM9004-AD RF = 1955MHz, LO =1950MHz	●	70	89		dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio at –1dBFS	LTM9004-AA RF = 1950.5MHz, LO =1950MHz	●	51.5	58.5		dB
		LTM9004-AB RF = 1951MHz, LO =1950MHz	●	51.5	60		dB
		LTM9004-AC RF = 1952.5MHz, LO =1950MHz	●	53	61		dB
		LTM9004-AD RF = 1955MHz, LO =1950MHz	●	53	60		dB
HD2	2nd Order Harmonic Distortion Ratio at –1dBFS	LTM9004-AA RF = 1950.5MHz, LO =1950MHz			64		dB
		LTM9004-AB RF = 1951MHz, LO =1950MHz			66		dB
		LTM9004-AC RF = 1952.5MHz, LO =1950MHz			66		dB
		LTM9004-AD RF = 1955MHz, LO =1950MHz			64		dB
HD3	3rd Order Harmonic Distortion Ratio at –1dBFS	LTM9004-AA RF = 1950.5MHz, LO =1950MHz			69		dB
		LTM9004-AB RF = 1951MHz, LO =1950MHz			66		dB
		LTM9004-AC RF = 1952.5MHz, LO =1950MHz			67		dB
		LTM9004-AD RF = 1955MHz, LO =1950MHz			67		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V. V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution (No Missing Codes)		●	14			Bits
	Integral Linearity Error (Note 4)	Differential Analog Input			±1.5		LSB
	Differential Linearity Error	Differential Analog Input			±1		LSB

DIGITAL INPUTS AND OUTPUTS

the ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V. V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Mixer Logic Input (MIXENABLE)							
V_{IH}	High Level Input Voltage	V_{CC1} = 5V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC1} = 5V	●			1	V
I_{IN}	Input Current	V_{IN} = V_{CC1}			120		µA
	Turn On Time				120		ns
	Turn Off Time				750		ns
First Amplifier Logic Input (AMP1ENABLE)							
V_{IH}	High Level Input Voltage	V_{CC2} = 5V	●	2.55	2		V
V_{IL}	Low Level Input Voltage	V_{CC2} = 5V	●		1.8	1.25	V
R_{IN}	Input Pull-Up Resistance	V_{CC2} = 5V, $V_{AMP1ENABLE}$ = 0V to 0.5V		25		70	kΩ
	Turn On Time				200		ns
	Turn Off Time				50		ns
Second Amplifier Logic Input (AMP2ENABLE, LTM9004-AA, LTM9004-AB)							
V_{IH}	High Level Input Voltage	V_{CC3} = 5V	●	V_{CC3} – 0.6			V
V_{IL}	Low Level Input Voltage	V_{CC3} = 5V	●			V_{CC3} – 2.1	V
R_{IN}	Input Pull-Up Resistance	V_{CC3} = 5V, $V_{AMP2ENABLE}$ = 2.9V to 0V		40	66	90	kΩ
	Turn On Time				4		µs
	Turn Off Time				350		ns
Second Amplifier Logic Input (AMP2ENABLE, LTM9004-AC, LTM9004-AD)							
V_{IH}	High Level Input Voltage	V_{CC3} = 3V	●	2.55	2.25		V
V_{IL}	Low Level Input Voltage	V_{CC3} = 3V	●		0.7	0.4	V
R_{IN}	Input Pull-Up Resistance	V_{CC3} = 3V, $V_{AMP2ENABLE}$ = 0V to 0.5V		60	100	140	kΩ
	Turn On Time				200		ns
	Turn Off Time				50		ns
ADC Logic Inputs (CLK, $\overline{OE}$, ADCSHDN, MODE, MUX)							
V_{IH}	High Level Input Voltage	V_{DD} = 3V	●	2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 3V	●			0.8	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 6)			3		pF
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–3		3	µA
I_{MODE}	MODE Input Leakage	0V < MODE < V_{DD}	●	–3		3	µA

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V. V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Outputs							
OV_{DD} = 3V							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = 3V (Note 6)			3		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = 3V			50		mA
V_{OH}	High Level Output Voltage	I_O = –10µA I_O = –200µA	 ●	 2.7	2.995 2.99		V V
V_{OL}	Low Level Output Voltage	I_O = 10µA I_O = 1.6mA	 ●		0.005 0.09	 0.4	V V
OV_{DD} = 2.5V							
V_{OH}	High Level Output Voltage	I_O = –200µA			2.49		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –200µA			1.79		V
V_{OL}	Low Level Output Voltage	I_O = 1.6mA			0.09		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V. V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB) (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC1}	Mixer Supply Voltage		●	4.5		5.25	V
V_{CC2}	First Amplifier Supply Voltage		●	4.5		5.25	V
V_{CC3}	Second Amplifier Supply Voltage	LTM9004-AA, LTM9004-AB LTM9004-AC, LTM9004-AD	● ●	4.5 2.7	 3	5.25 3.5	V V
V_{DD}	ADC Analog Supply Voltage		●	2.7	3	3.6	V
OV_{DD}	ADC Digital Output Supply Voltage		●	0.5	3	3.6	V
I_{CC1}	Mixer Supply Current		●		129	180	mA
$I_{CC1(SHDN)}$	Mixer Shutdown Current	MIXENABLE = 0V, AMPxENABLE = HIGH, ADCSHDN = 0V, $\overline{OE}$ = 0V	●		10	11	mA
I_{CC2}	First Amplifier Supply Current		●		52	63	mA
$I_{CC2(SHDN)}$	First Amplifier Shutdown Current	MIXENABLE = 5V, AMP1ENABLE = 0V, AMP2ENABLE = HIGH, ADCSHDN = 0V, $\overline{OE}$ = 0V	●		7.5	9	mA
I_{CC3}	Second Amplifier Supply Current	LTM9004-AA, LTM9004-AB	●		21	24	mA
$I_{CC3(SHDN)}$	Second Amplifier Shutdown Current	LTM9004-AA, LTM9004-AB, MIXENABLE = AMP1ENABLE = 5V, AMP2ENABLE = 0V, ADCSHDN = 0V, $\overline{OE}$ = 0V	●		0.8	4	mA
I_{CC3}	Second Amplifier Supply Current	LTM9004-AC, LTM9004-AD	●		36	44	mA
$I_{CC3(SHDN)}$	Second Amplifier Shutdown Current	LTM9004-AC, LTM9004-AD, MIXENABLE = AMP1ENABLE = 5V, AMP2ENABLE = 0V, ADCSHDN = 0V, $\overline{OE}$ = 0V	●		0.6	4	mA
I_{DD}	ADC Supply Current		●		273	306	mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V. V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB) (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$P_{D(SLEEP)}$	Sleep Power	MIXENABLE = AMPxENABLE = 0V, ADCSHDN = 3V, $\overline{OE}$ = 3V, No CLK			7		mW
$P_{D(NAP)}$	Nap Mode Power	MIXENABLE = AMPxENABLE = 0V, ADCSHDN = 3V, $\overline{OE}$ = 0V, No CLK			33		mW
$P_{D(TOTAL)}$	Total Power Dissipation	LTM9004-AA, LTM9004_AB, MIXENABLE = AMP1ENABLE = AMP2ENABLE = 5V, ADCSHDN = 0V, f_{SAMPLE} = MAX			1.83		W
		LTM9004-AC, LTM9004-AD MIXENABLE = AMP1ENABLE = 5V, AMP2ENABLE = 3V, ADCSHDN = 0V, f_{SAMPLE} = MAX			1.83		W

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Unless otherwise noted, V_{CC1} = V_{CC2} = 5V, V_{DD} = OV_{DD} = 3V. V_{CC3} = 3V (LTM9004-AC, LTM9004-AD), V_{CC3} = 5V (LTM9004-AA, LTM9004-AB)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency		●	1		125	MHz
t_L	CLK Low Time	Duty Cycle Stabilizer Off (Note 6) Duty Cycle Stabilizer Off (Note 6)	● ●	3.8 3	4 4	500 500	ns ns
t_H	CLK High Time	Duty Cycle Stabilizer Off (Note 6) Duty Cycle Stabilizer Off (Note 6)	● ●	3.8 3	4 4	500 500	ns ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Time Jitter				0.2		ps_{RMS}
t_{AP}	Sample-and-Hold Aperture Delay				0		ns
t_D	CLK to DATA delay	C_L = 5pF (Note 6)	●	1.4	2.7	5.4	ns
	DATA to CLKOUT Skew	(t_D - t_C) (Note 6)	●	–0.6	0	0.6	ns
t_C	MUX to DATA Delay	C_L = 5pF (Note 6)	●	1.4	2.7	5.4	ns
	DATA Access Time After $\overline{OE}$↓	C_L = 5pF (Note 6)	●		4.3	10	ns
	BUS Relinquish Time	(Note 6)	●		3.3	8.5	ns
	Pipeline Latency				5		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: f_{SAMPLE} = 125MHz, CLKI = CLKQ unless otherwise noted.

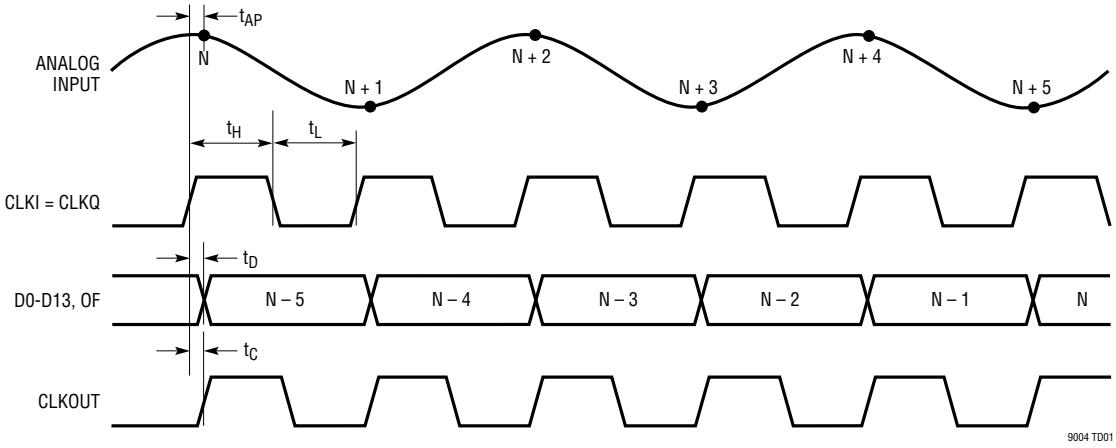
Note 4: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 5: DC offset voltage is defined as the DC voltage corresponding to the output code with LO signal applied, but no RF signal.

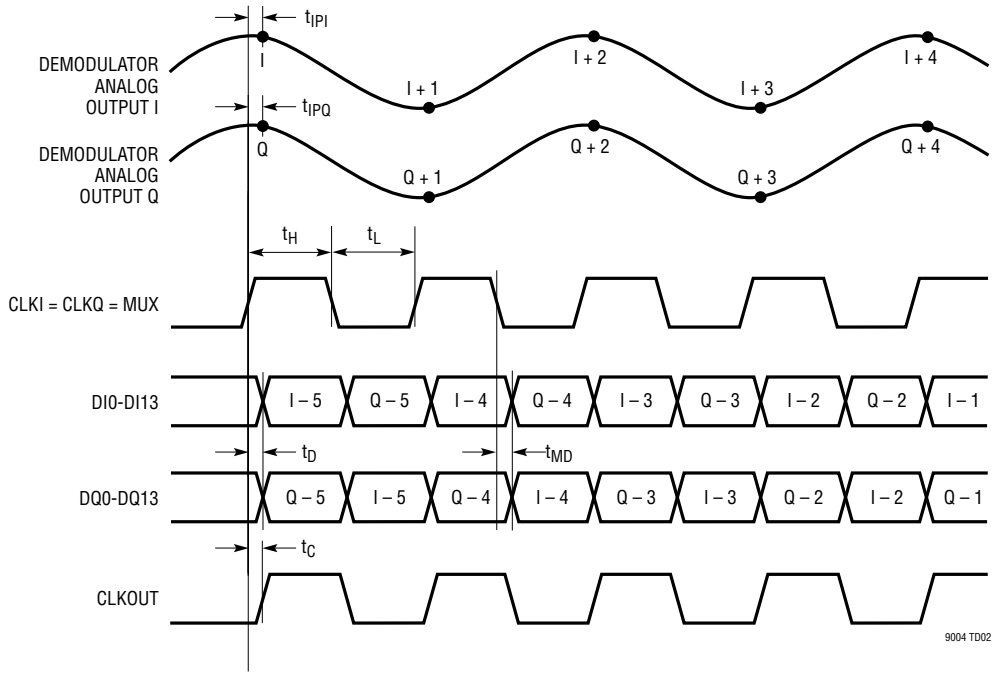
Note 6: Guaranteed by design, not subject to test.

TIMING DIAGRAMS

Dual Digital Output Bus Timing

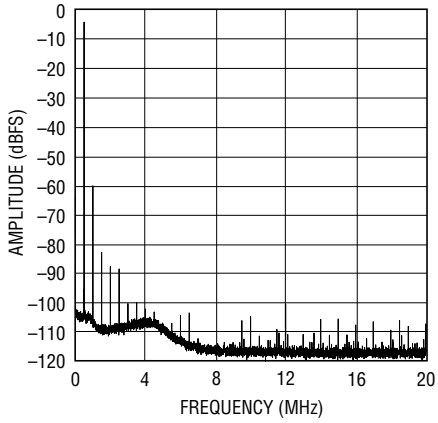


Multiplexed Digital Output Bus Timing

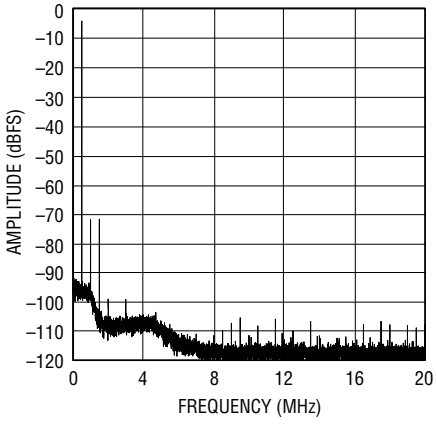


TYPICAL PERFORMANCE CHARACTERISTICS

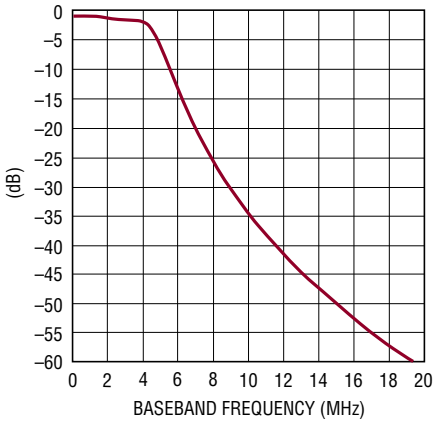
LTM9004-AA: 64k Point FFT
f_{IN} = 700.5MHz, –1dBFS
SENSE = V_{DD}



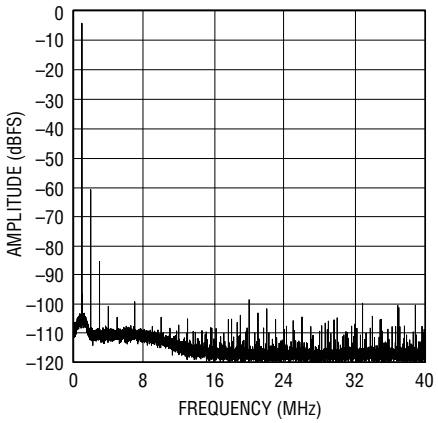
LTM9004-AA: 64k Point FFT
f_{IN} = 1950.5MHz, –1dBFS
SENSE = V_{DD}



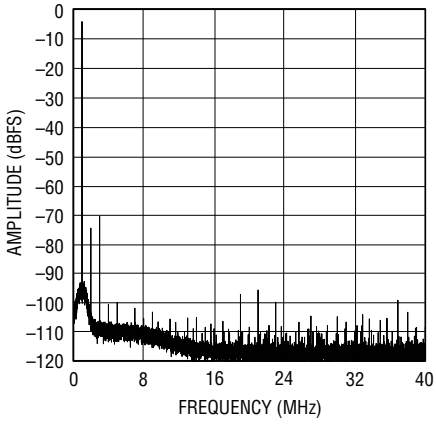
LTM9004-AA, Baseband Frequency Response



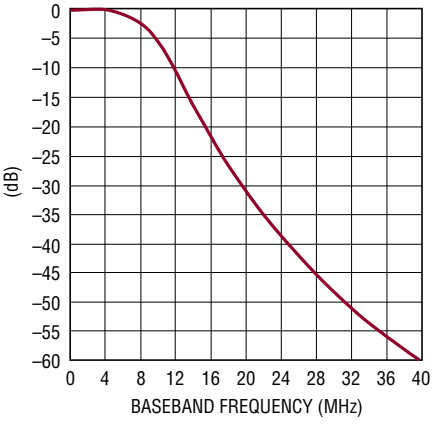
LTM9004-AB: 64k Point FFT
f_{IN} = 701.0MHz, –1dBFS
SENSE = V_{DD}



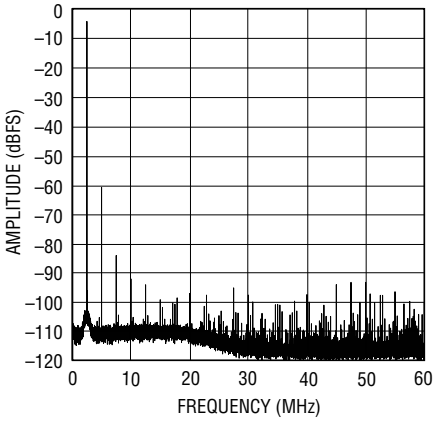
LTM9004-AB: 64k Point FFT
f_{IN} = 1951.0MHz, –1dBFS
SENSE = V_{DD}



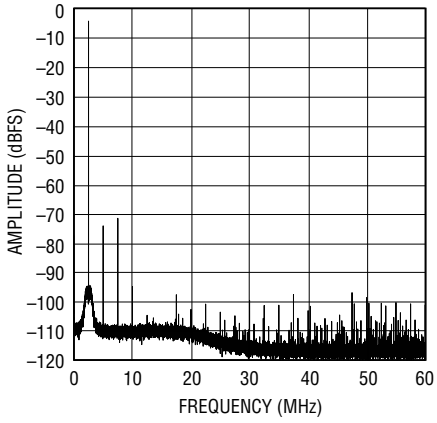
LTM9004-AB, Baseband Frequency Response



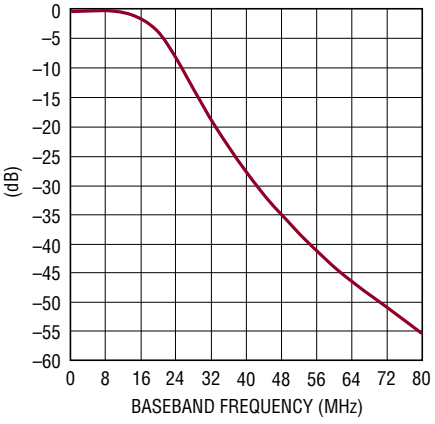
LTM9004-AC: 64k Point FFT
f_{IN} = 702.5MHz, –1dBFS
SENSE = V_{DD}



LTM9004-AC: 64k Point FFT
f_{IN} = 1952.5MHz, –1dBFS
SENSE = V_{DD}

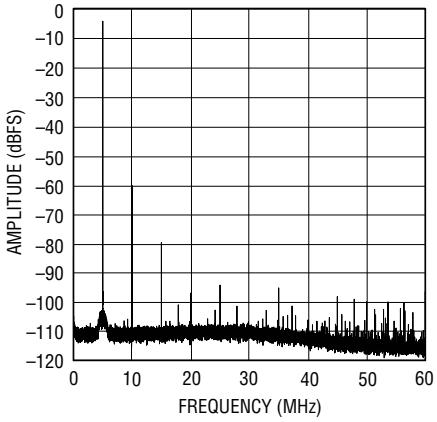


LTM9004-AC, Baseband Frequency Response

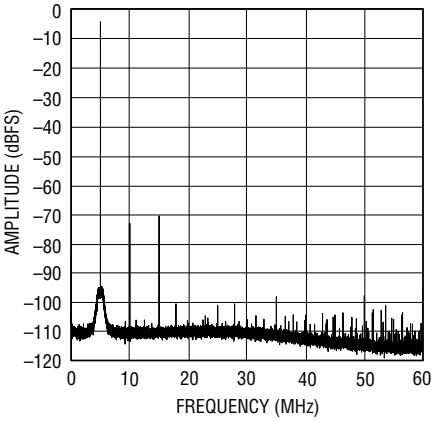


TYPICAL PERFORMANCE CHARACTERISTICS

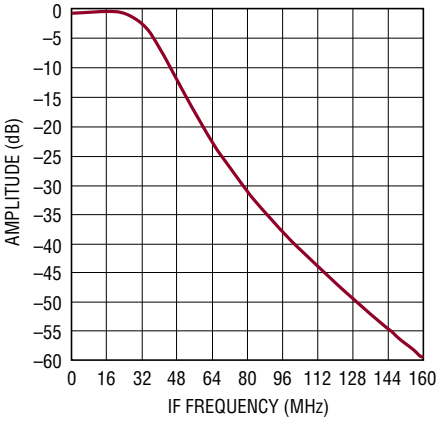
LTM9004-AD: 64k Point FFT
f_{IN} = 705.0MHz, –1dBFS
SENSE = V_{DD}



LTM9004-AD: 64k Point FFT
f_{IN} = 1955.0MHz, –1dBFS
SENSE = V_{DD}



LTM9004-AD, Baseband Frequency Response



PIN FUNCTIONS

Supply Pins

V_{CC1} (Pins G5, H2), V_{CC2} (Pins C5, C8, K5, K8): Analog 5V Supply for Mixer and First Amplifiers. The specified operating range is 4.5V to 5.25V. The voltage on this pin provides power for the mixer and amplifier stages only and is internally bypassed to GND.

V_{CC3} (Pins C9, C12, K9, K12): Analog Supply for Second Amplifiers. The specified operating range is 4.5V to 5.5V for LTM9004-AA and LTM9004-AB. The specified operating range is 2.7V to 3.5V for LTM9004-AC and LTM9004-AD. V_{CC3} is internally bypassed to GND.

V_{DD} (Pins D14, F13, G13, J14): Analog 3V Supply for the ADC. The specified operating range is 2.7V to 3.6V. V_{DD} is internally bypassed to GND.

OV_{DD} (Pins D17, J17): Positive Supply for the Digital Output Drivers. The specified operating range is 0.5V to 3.6V. OV_{DD} is internally bypassed to OGND.

GND (See Table for Pin Locations): Analog Ground.

OGND (Pins C17, K17): Digital Output Driver Ground.

Analog Inputs

RF (Pin E2): RF Input Pin. This is a single-ended 50Ω terminated input. No external matching network is required for the high frequency band. An external series capacitor (and/or shunt capacitor) may be required for impedance transformation to 50Ω in the low frequency band from 700MHz to 1.5GHz (see Figure 4). If the RF source is not DC blocked, a series blocking capacitor should be used. Otherwise, damage to the IC may result.

LO (Pin H3): Local Oscillator Input Pin. This is a single-ended 50Ω terminated input. No external matching network is required in the high frequency band. An external shunt capacitor (and/or series capacitor) may be required for impedance transformation to 50Ω for the low frequency band from 700MHz to 1.5GHz (see Figure 6). If the LO source is not DC blocked, a series blocking capacitor must be used. Otherwise, damage to the IC may result.

CLKQ (Pin G14): Q-Channel ADC Clock Input. The input sample starts on the positive edge. Tie CLKQ and CLKI together.

CLKI (Pin F14): I-Channel ADC Clock Input. The input sample starts on the positive edge. Tie CLKQ and CLKI together.

I^+_ADJ (Pin B1): DC Offset Adjust Pin for I-Channel, + Line. Source or sink current through this pin to trim DC offset.

I^-_ADJ (Pin C1): DC Offset Adjust Pin for I-Channel, – Line. Source or sink current through this pin to trim DC offset.

Q^+_ADJ (Pin K1): DC Offset Adjust Pin for Q-Channel, + Line. Source or sink current through this pin to trim DC offset.

Q^-_ADJ (Pin L1): DC Offset Adjust Pin for Q-Channel, – Line. Source or sink current through this pin to trim DC offset.

Control Pins

MIXENABLE (Pin E4): Mixer Enable Pin. If MIXENABLE = high (the input voltage is higher than 2.0V), the mixer is enabled. If MIXENABLE = low (the input voltage is less than 1.0V), it is disabled. If the enable function is not needed, then this pin should be tied to V_{CC1}.

AMP1ENABLE (Pins D5, L5): First Amplifier Enable Pin. AMP1ENABLE = high or floating results in normal (active) operating mode for the first amplifier in each channel. AMP1ENABLE = low (a minimum of 2.1V below V_{CC2}), results in the first amplifiers being disabled. If the enable function is not needed, then this pin should be tied to V_{CC2}.

AMP2ENABLE (Pins C10, L10): Second Amplifier Enable Pin. AMP2ENABLE = high or floating results in normal (active) operating mode for the second amplifier in each channel. AMP2ENABLE = low (a minimum of 0.45V below V_{CC3}), results in the second amplifiers being disabled. If the enable function is not needed, then this pin should be tied to V_{CC3}.

ADCSHDNQ (Pin J12): Q-Channel ADC Shutdown Mode Selection Pin. Connecting ADCSHDNQ to GND and $\overline{OEQ}$ to GND results in normal operation with the outputs enabled. Connecting ADCSHDNQ to GND and $\overline{OEQ}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting ADCSHDNQ to V_{DD} and $\overline{OEQ}$ to GND results in nap mode with the outputs at high impedance. Connecting ADCSHDNQ to V_{DD} and $\overline{OEQ}$ to V_{DD} results in sleep mode with the outputs at high impedance.

ADCSHDNI (Pin D12): I-Channel ADC Shutdown Mode Selection Pin. Connecting ADCSHDNI to GND and $\overline{OEI}$ to GND results in normal operation with the outputs enabled. Connecting ADCSHDNI to GND and $\overline{OEI}$ to V_{DD} results in normal operation with the outputs at high impedance.

PIN FUNCTIONS

Connecting ADCSHDNI to V_{DD} and $\overline{OEI}$ to GND results in nap mode with the outputs at high impedance. Connecting ADCSHDNI to V_{DD} and $\overline{OEI}$ to V_{DD} results in sleep mode with the outputs at high impedance.

SENSEQ (Pin H13), SENSEI (Pin E13): ADC Reference Programming Pin. Tie to V_{DD} for normal operation. An external reference can be used, see ADC Reference section.

MODE (Pin J13): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Note that MODE controls both channels. Connecting MODE to GND selects straight binary output format and turns the clock duty cycle stabilizer off. 1/3 V_{DD} selects straight binary output format and turns the clock duty cycle stabilizer on. 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

MUX (Pin D13): Digital Output Multiplexer Control. If MUX = high, Q-channel comes out on DQ0 to DQ13; I-channel comes out on DI0 to DI13. If MUX = low, the output busses are swapped and Q-channel comes out on DI0 to DI13; I-channel comes out on DQ0 to DQ13. To multiplex both channels onto a single output bus, connect MUX, CLKQ and CLKI together.

$\overline{OEQ}$ (Pin K13): Q-Channel Output Enable Pin. Refer to ADCSHDNQ pin function.

$\overline{OEI}$ (Pin C13): I-Channel Output Enable Pin. Refer to ADCSHDNI pin function.

Digital Outputs

CLKOUT (Pin E12): ADC Data Ready Clock Output. Latch data on the falling edge of CLKOUT. CLKOUT is derived from CLKQ. Tie CLKQ to CLKI for simultaneous operation.

DI0 - DI13 (See Table for Pin Locations): I-Channel (In-Phase) ADC Digital Outputs. DI13 is the MSB.

DQ0 - DQ13 (See Table for Pin Locations): Q-Channel (Quadrature) ADC Digital Outputs. DQ13 is the MSB.

OF (Pin H12): Overflow/Underflow Output. High when an overflow or underflow has occurred on either I-channel or Q-channel.

Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M
1	GND	I^+_ADJ	I^-_ADJ	GND	GND	GND	GND	GND	GND	Q^+_ADJ	Q^-_ADJ	GND
2	GND	GND	GND	GND	RF	GND	GND	V_{CC1}	GND	GND	GND	GND
3	GND	GND	GND	GND	GND	GND	GND	LO	GND	GND	GND	GND
4	GND	GND	GND	GND	MIX_EN	GND	GND	GND	GND	GND	GND	GND
5	GND	GND	V_{CC2}	AMP1A_EN	GND	GND	V_{CC1}	GND	GND	V_{CC2}	AMP1B_EN	GND
6	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
7	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
8	GND	GND	V_{CC2}	GND	GND	GND	GND	GND	GND	V_{CC2}	GND	GND
9	GND	GND	V_{CC3}	GND	GND	GND	GND	GND	GND	V_{CC3}	GND	GND
10	GND	GND	AMP2A_EN	GND	GND	GND	GND	GND	GND	GND	AMP2B_EN	GND
11	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
12	GND	GND	V_{CC3}	SHDNI	CLKOUT	GND	GND	OF	SHDNQ	V_{CC3}	GND	GND
13	DI3	DI0	$\overline{OEI}$	MUX	SENSEI	V_{DD}	V_{DD}	SENSEQ	MODE	$\overline{OEQ}$	DQ13	DQ10
14	DI8	DI4	DI1	V_{DD}	GND	CLKI	CLKQ	GND	V_{DD}	DQ12	DQ8	DQ6
15	DI7	DI6	DI2	GND	GND	GND	GND	GND	GND	DQ11	DQ4	DQ5
16	GND	DI9	DI5	DI10	DI11	GND	GND	DQ1	DQ3	DQ9	DQ7	GND
17	GND	GND	OGND	OV_{DD}	DI12	DI13	DQ0	DQ2	OV_{DD}	OGND	GND	GND

Top View of LGA Package (Looking Through Component)

BLOCK DIAGRAM

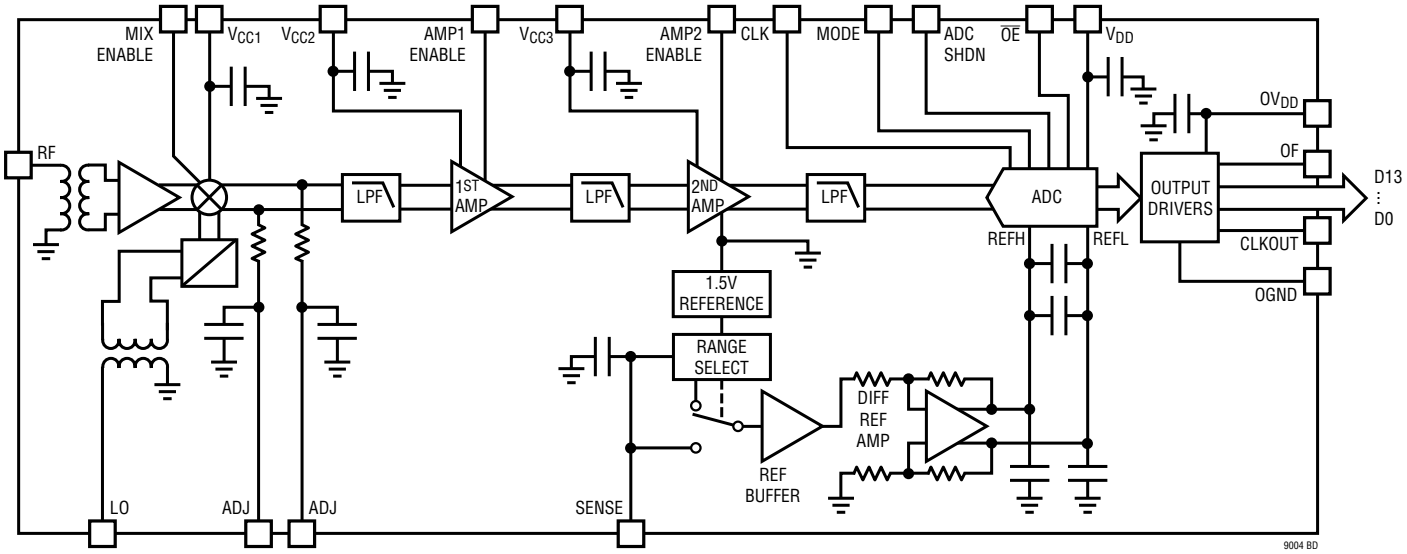


Figure 1. Functional Block Diagram (Only One Channel is Shown)

OPERATION

DESCRIPTION

The LTM9004 is a direct conversion receiver targeting high linearity receiver applications, such as wireless infrastructure with RF input frequencies up to 2.7GHz. It is an integrated µModule receiver utilizing system in a package (SiP) technology to combine a dual, high speed 14-bit A/D converter, lowpass filters, two low noise differential amplifiers per channel with fixed gain, and an I/Q demodulator with DC offset adjustment.

The direct conversion receiver architecture offers several advantages over the traditional superheterodyne. It eases the requirements for RF front-end bandpass filtering, as it is not susceptible to signals at the image frequency. The RF bandpass filters need only attenuate strong out-of-band signals to prevent them from overloading the front end. Also, direct conversion eliminates the need for IF amplifiers and bandpass filters. Instead, the RF input signal is directly converted to baseband.

Direct conversion does, however, come with its own set of implementation issues. Since the receive LO signal is at the same frequency as the RF signal, it can easily radiate from the receive antenna and violate regulatory standards.

Unwanted baseband signals can also be generated by 2nd order nonlinearity of the receiver. A tone at any frequency entering the receiver will give rise to a DC offset in the baseband circuits. The 2nd order nonlinearity of the receiver also allows a modulated signal, even the desired signal, to generate a pseudo-random block of energy centered about DC.

For this reason, the LTM9004 provides for DC offset correction immediately following the I/Q demodulator stage. Once generated, straightforward elimination of DC offset becomes very problematic. Necessary gain in the baseband amplifiers increases the offset because their frequency response extends to DC.

The following sections describe in further detail the operation of each section. The µModule technology allows the LTM9004 to be customized and this is described in the first section. The outline of the remaining sections follows the basic functional elements as shown in Figure 2.

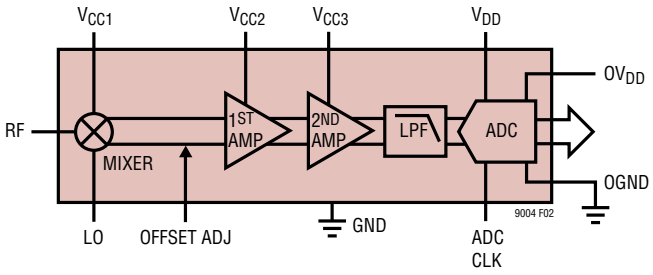


Figure 2. Basic Functional Elements (Only Half Shown)

SEMI-CUSTOM OPTIONS

The µModule construction affords a new level of flexibility in application-specific standard products. Standard ADC, amplifier and RF components can be integrated regardless of their process technology and matched with passive components to a particular application. The LTM9004-AA, as the first example, is configured with a dual 14-bit ADC sampling at rates up to 125Msps. The amplifiers provide a total voltage gain of 14dB (including the gain of the mixer). The lowpass filter limits the bandwidth to 1.92MHz. The RF and LO inputs of the I/Q demodulator have integrated transformers and present 50Ω single-ended inputs. An external DAC can be used for DC offset cancellation.

However, other options are possible through Linear Technology's semi-custom development program. Linear Technology has in place a program to deliver other sample rate, resolution, gain and filter configurations for nearly any specified application. These semi-custom designs are based on existing components with an appropriately modified passive network. The final subsystem is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested and optimized solution in the same package. For more details on the semi-custom receiver subsystem program, contact Linear Technology.

MIXER OPERATION

The RF signal is applied to the inputs of the RF transconductance amplifiers and is then demodulated into I/Q baseband signals using quadrature LO signals which are internally generated from an external LO source by precision 90° phase shifters.

OPERATION

Broadband transformers are integrated at both the RF and LO inputs to enable single-ended RF and LO interfaces. In the high frequency band (1.5GHz to 2.7GHz), both RF and LO ports are internally matched to 50Ω. No external matching components are needed. For the lower frequency bands (700MHz to 1.5GHz), a simple network with series and/or shunt capacitors can be used as the impedance matching network.

I-CHANNEL AND Q-CHANNEL PHASE RELATIONSHIP

The phase relationship between the I-channel output signal and the Q-channel output signal is fixed. When the LO input frequency is larger (or smaller) than the RF input frequency, the Q-channel outputs (DQ0 to DQ13) lag (or lead) the I-channel outputs (DI0 to DI13) by 90°.

DC OFFSET ADJUSTMENT

Each channel includes provision for adjustment of the DC offset voltage presented at the input of the A/D converter. There are two adjust terminals for each channel, so that the common mode and differential mode DC offset may be independently trimmed. These terminals are designed to accept a source or sink current of up to 0.3mA. If the currents through the two terminals are not equal, then a differential DC offset will be created. If they are equal, then the resulting DC offset will be common mode only. As an example, sinking 0.1mA from one terminal and 0.11mA from the other terminal will yield a differential DC offset of approximately 5.9mV or 48LSB. A maximum DC offset of approximately 178mV or 1457LSB can be imposed by applying a 5V differential voltage to the adjust terminals.

AMPLIFIER OPERATION

Each channel of the LTM9004 consists of two stages of DC-coupled, low noise and low distortion fully differential op amps/ADC drivers. Each stage implements a 2-pole active lowpass filter using a high speed, high performance operational amplifier and precision passive components. The cascade of two stages is designed to provide maximum gain and phase flatness, along with adjacent channel and blocker rejection. The lowpass response can be configured for different cutoff frequencies within the range of the amplifiers. LTM9004-AA, for example, implements a lowpass filter designed for 1.92MHz.

ADC INPUT NETWORK

The passive network between the second amplifier output stages and the ADC input stages provides a 1st order topology configured for lowpass response.

CONVERTER OPERATION

The analog-to-digital converter (ADC) shown in Figure 1 is a dual CMOS pipelined multistep converter. The converter has six pipelined ADC stages; a sampled analog input will result in a digitized value six cycles later (see the Timing Diagrams section). The CLK inputs are single ended. The ADC has two phases of operation, determined by the state of the CLK input pins.

Each pipelined stage contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and visa versa.

When CLK is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors. At the instant that CLK transitions from low to high, the sampled input is held. While CLK is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of CLK. When CLK goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When CLK goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third, fourth and fifth stages, resulting in a fifth stage residue that is sent to the sixth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

APPLICATIONS INFORMATION

RF INPUT

Figure 3 shows the mixer's RF input which consists of an integrated transformer and high linearity transconductance amplifiers. The primary side of the transformer is connected to the RF input pin. The secondary side of the transformer is connected to the differential inputs of the transconductance amplifiers. Under no circumstances should an external DC voltage be applied to the RF input pin. DC current flowing into the primary side of the transformer may cause damage to the integrated transformer. A series blocking capacitor should be used to AC-couple the RF input port to the RF signal source.

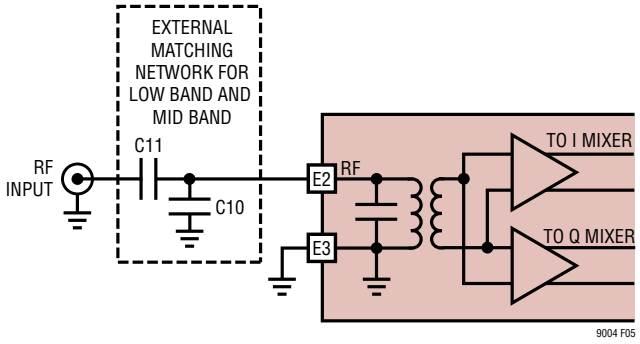


Figure 3. RF Input Interface

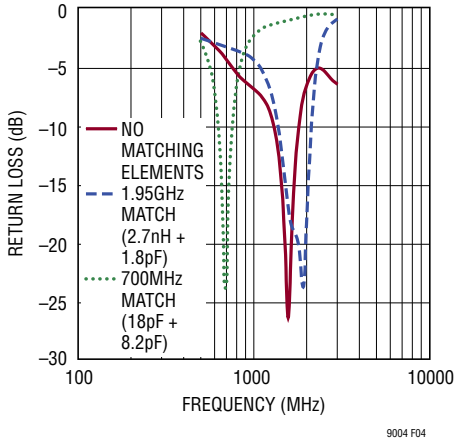


Figure 4. RF Port Return Loss vs Frequency

The RF input port is internally matched over a wide frequency range from 1.5GHz to 2.7GHz with input return loss typically better than 10dB. No external matching network is needed for this frequency range. When the part is operated at lower frequencies, however, the input return loss can be improved with the matching network shown in Figure 3. Shunt capacitor C10 and series capacitor C11 can be selected for optimum input impedance matching at the desired frequency as illustrated in Figure 4. For lower frequency band operation, the external matching component C11 can serve as a series DC blocking capacitor.

The RF input impedance and S11 parameters (without external matching components) are listed in Table 1.

Table 1. RF Input Impedance

FREQUENCY (MHz)	MAGNITUDE	PHASE (°)	R (Ω)	X (Ω)
500	0.78	–139.7	16.1	–10.7
600	0.69	–166.6	10.1	–3.8
700	0.60	163.7	14.0	3.8
800	0.52	132.6	25.8	6.9
900	0.48	102.7	41.9	3.4
1000	0.45	77.4	58.8	–4.3
1100	0.42	56.6	74.9	–11.4
1200	0.38	40.1	86.4	–12.4
1300	0.31	25.7	87.6	–7.1
1400	0.22	10.9	76.8	–1.4
1500	0.10	–14.5	60.9	0.3
1600	0.06	–132.9	45.9	–0.2
1700	0.19	–170.7	34.6	–0.4
1800	0.30	–177.7	26.8	0.2
1900	0.40	–172.1	21.8	1.1
2000	0.47	–169.4	18.7	1.9
2100	0.51	–168.6	16.7	2.2
2200	0.54	–169.3	15.4	2.3
2300	0.55	–172.0	14.7	1.7
2400	0.55	–176.0	14.4	0.9
2500	0.54	–178.7	14.9	–0.3
2600	0.52	–172.3	15.9	–1.6
2700	0.50	–164.3	17.6	–3.0
2800	0.49	–155.0	19.9	–4.3
2900	0.48	–144.7	22.9	–5.4
3000	0.48	–134.8	26.4	–6.0

LO Input Port

The mixer's LO input interface is shown in Figure 5. The input consists of an integrated transformer and a precision quadrature phase shifter which generates 0° and

APPLICATIONS INFORMATION

90° phase-shifted LO signals for the LO buffer amplifiers driving the I/Q mixers. The primary side of the transformer is connected to the LO input pin. The secondary side of the transformer is connected to the differential inputs of the LO quadrature generator. Under no circumstances should an external DC voltage be applied to the input pin. DC current flowing into the primary side of the transformer may damage the transformer. A series blocking capacitor should be used to AC-couple the LO input port to the LO signal source.

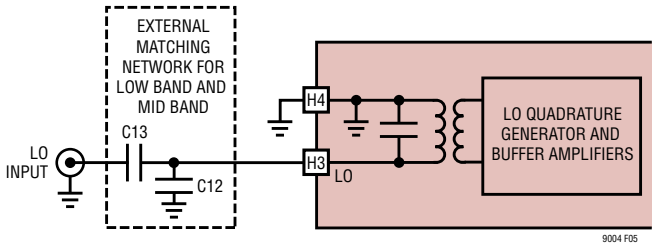


Figure 5. LO Input Interface

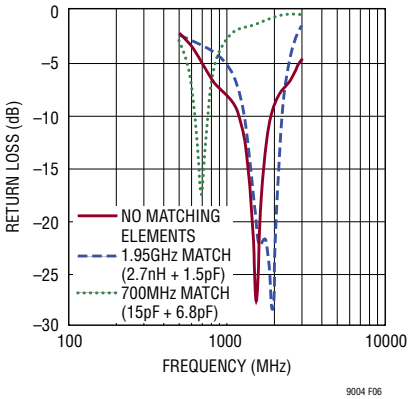


Figure 6. LO Return Loss vs Frequency

The LO input port is internally matched over a wide frequency range from 1.5GHz to 2.7GHz with input return loss typically better than 10dB. No external matching network is needed for this frequency range. When the part is operated at a lower frequency, the input return loss can be improved with the matching network shown in Figure 8. Shunt capacitor C12 and series capacitor C13 can be selected for optimum input impedance matching at the desired frequency as illustrated in Figure 6. For lower frequency operation, external matching component C13 can serve as the series DC blocking capacitor.

The LO input impedance and S11 parameters (without external matching components) are listed in Table 2.

Table 2. LO Input Impedance

FREQUENCY (MHz)	MAGNITUDE	PHASE (°)	R (Ω)	X (Ω)
500	0.77	–143.2	14.8	–10.0
600	0.66	–172.6	10.6	–2.0
700	0.55	154.5	17.8	5.1
800	0.46	119.8	33.1	5.5
900	0.41	88.8	50.8	–0.3
1000	0.39	63.9	67.5	–7.4
1100	0.35	44.9	80.2	–10.1
1200	0.30	31.5	83.4	–7.2
1300	0.23	22.7	76.9	–3.1
1400	0.14	20.7	65.2	–0.9
1500	0.05	47.3	53.6	–0.1
1600	0.08	139.3	44.1	0.3
1700	0.17	152.3	36.9	0.9
1800	0.25	154.7	31.7	1.6
1900	0.31	157.5	27.9	2.0
2000	0.35	160.5	25.1	2.2
2100	0.38	164.9	23.1	2.0
2200	0.41	170.3	21.4	1.4
2300	0.42	177.7	20.2	0.4
2400	0.44	–173.8	19.6	–1.0
2500	0.46	–164.6	19.7	–2.6
2600	0.48	–155.7	20.2	–4.1
2700	0.51	–147.1	21.2	–5.6
2800	0.54	–139.2	22.8	–6.8
2900	0.56	–131.5	25.2	–7.6
3000	0.58	–124.9	27.9	–7.9

ADC Reference

The internal voltage reference can be configured for two pin-selectable ADC input ranges. Tying the SENSE pin to V_{DD} selects the default range; tying the SENSE pin to 1.5V selects a 3dB lower range. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. The SENSE pin is internally bypassed to ground with a 1µF ceramic capacitor.

APPLICATIONS INFORMATION

Enable Interface

The enable voltage necessary to turn on the mixer is 2V. To disable or turn off the mixer, this voltage should be below 1V. If this pin is not connected, the mixer is disabled. However, it is not recommended that the pin be left floating for normal operation.

The AMP1ENABLE and AMP2ENABLE pins are CMOS logic inputs with internal pull-up resistors. If the pin is driven low, the amplifier powers down with Hi-Z outputs. If the pin is left unconnected or driven high, the part is in normal active operation. Some care should be taken to control leakage currents at this pin to prevent inadvertently putting it into shutdown. The turn-on and turn-off time between the shutdown and active states are typically less than 1µs.

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting ADCSHDNx to GND results in normal operation. Connecting ADCSHDNx to V_{DD} and $\overline{OE}$x to V_{DD} results in sleep mode, which powers down all circuitry including the reference and the ADC typically dissipates 1mW. When exiting sleep mode, it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting ADCSHDNx to V_{DD} and $\overline{OE}$x to GND results in nap mode and the ADC typically dissipates 30mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap modes, all digital outputs are disabled and enter the Hi-Z state.

Channels I and Q have independent ADCSHDN pins (ADCSHDNI, ADCSHDNQ.) I-Channel is controlled by ADCSHDNI and $\overline{OEI}$, and Q-Channel is controlled by ADCSHDNQ and $\overline{OEQ}$. The nap, sleep and output enable modes of the two channels are completely independent, so it is possible to have one channel operating while the other channel is in nap or sleep mode.

Note that ADCSHDN has the opposite polarity as MIXENABLE, AMP1ENABLE and AMP2ENABLE. Normal operation is achieved with a logic low level on the SHDN pins and a high level disables the respective functions.

It is not recommended to enable or shut down individual components separately. These pins are separated for test purposes.

Driving the ADC Clock Inputs

The CLK inputs can be driven directly with a CMOS or TTL level signal. A sinusoidal clock can also be used along with a low-jitter squaring circuit before the CLK pin (Figure 7).

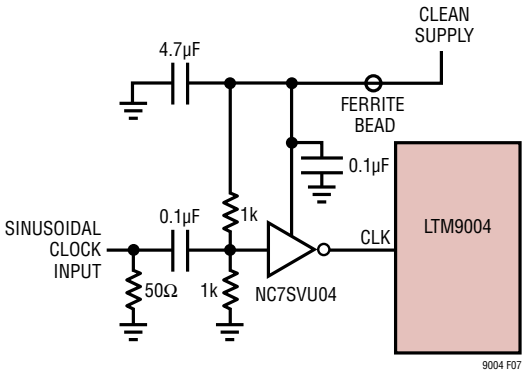


Figure 7. Sinusoidal Single-Ended CLK Driver

The noise performance of the ADC can depend on the clock signal quality as much as on the analog input. Any noise present on the CLK signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter. In applications where jitter is critical, such as when digitizing high input frequencies, use as large an amplitude as possible. Also, if the ADC is clocked with a sinusoidal signal, filter the CLK signal to reduce wideband noise and distortion products generated by the source.

It is recommended that CLKI and CLKQ are shorted together and driven by the same clock source. If a small time delay is desired between when the two channels sample the analog inputs, CLKI and CLKQ can be driven by two different signals. If this time delay exceeds 1ns, the performance of the part may degrade. CLKI and CLKQ should not be driven by asynchronous signals.

APPLICATIONS INFORMATION

Figure 8 and Figure 9 show alternatives for converting a differential clock to the single-ended CLK input. The use of a transformer provides no incremental contribution to phase noise. The LVDS or PECL to CMOS translators provide little degradation below 70MHz, but at 140MHz will degrade the SNR compared to the transformer solution. The nature of the received signals also has a large bearing on how much SNR degradation will be experienced. For high crest factor signals such as WCDMA or OFDM, where the nominal power level must be at least 6dB to 8dB below full scale, the use of these translators will have a lesser impact.

The transformer in the example may be terminated with the appropriate termination for the signaling in use. The use of a transformer with a 1:4 impedance ratio may be desirable in cases where lower voltage differential signals are considered. The center tap may be bypassed to ground through a capacitor close to the ADC if the differential signals originate on a different plane. The use of a capacitor at the input may result in peaking, and depending on transmission line length may require a 10Ω to 20Ω series resistor to act as both a lowpass filter for high frequency noise that may be induced into the clock line by neighboring digital signals, as well as a damping mechanism for reflections.

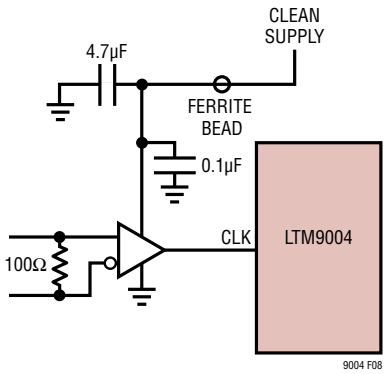


Figure 8. CLK Driver Using an LVDS or PECL to CMOS Converter

Maximum and Minimum Conversion Rates

The maximum conversion rate for the ADC is 125Msps. The lower limit of the sample rate is determined by the droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM9004 is 1Msps.

Clock Duty Cycle Stabilizer

An optional clock duty cycle stabilizer circuit ensures high performance even if the input clock has a non 50% duty cycle. Using the clock duty cycle stabilizer is recommended for most applications. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

This circuit uses the rising edge of the CLK pin to sample the analog input. The falling edge of CLK is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 40% to 60% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require a hundred clock cycles for the PLL to lock onto the input clock.

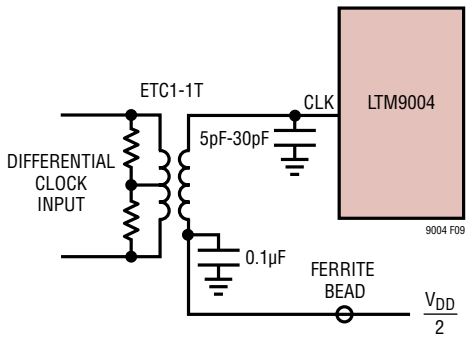


Figure 9. LVDS or PECL CLK Drive Using a Transformer

APPLICATIONS INFORMATION

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50% (±5%) duty cycle.

DIGITAL OUTPUTS

Table 3 shows the relationship between the analog input voltage, the digital data bits, and the overflow bit. Note that OF is high when an overflow or underflow has occurred on either channel I or channel Q.

Table 3. Output Codes vs Input Voltage

INPUT	OF	D13 – D0 (OFFSET BINARY)	D13 – D0 (2'S COMPLEMENT)
Overvoltage	1	11 1111 1111 1111	01 1111 1111 1111
Maximum	0	11 1111 1111 1111	01 1111 1111 1111
	0	11 1111 1111 1110	01 1111 1111 1110
	0	10 0000 0000 0001	00 0000 0000 0001
	0	10 0000 0000 0000	00 0000 0000 0000
	0	01 1111 1111 1111	11 1111 1111 1111
	0	01 1111 1111 1110	11 1111 1111 1110
	0	00 0000 0000 0001	10 0000 0000 0001
Minimum	0	00 0000 0000 0000	10 0000 0000 0000
Undervoltage	1	00 0000 0000 0000	10 0000 0000 0000

Digital Output Modes

Figure 10 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to low voltages. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

As with all high speed/high resolution converters the digital output loading can affect the performance. The digital outputs of the ADC should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. For full speed operation, the capacitive load should be kept under 10pF.

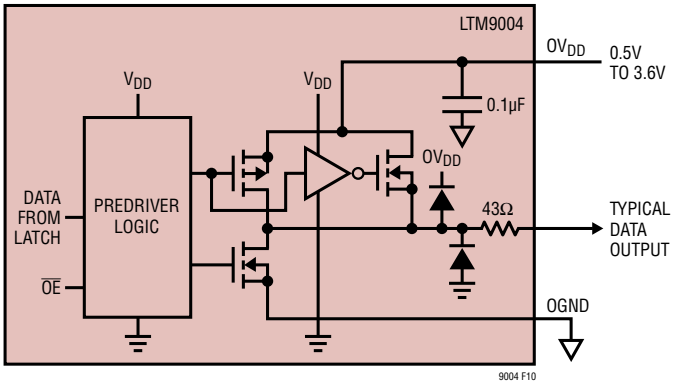


Figure 10. Digital Output Buffer

Lower OV_{DD} voltages will also help reduce interference from the digital outputs.

Data Format

Using the MODE pin, the ADC parallel digital output can be selected for offset binary or 2's complement format. Note that MODE controls both I and Q channels. Connecting MODE to GND or 1/3 V_{DD} selects straight binary output format. Connecting MODE to 2/3 V_{DD} or V_{DD} selects 2's complement output format. An external resistive divider can be used to set the 1/3 V_{DD} or 2/3 V_{DD} logic values. Table 4 shows the logic states for the MODE pin.

Table 4. MODE Pin Function

MODE PIN	OUTPUT FORMAT	CLOCK DUTY CYCLE STABILIZER
0	Straight Binary	Off
1/3V_{DD}	Straight Binary	On
2/3V_{DD}	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

When OF outputs a logic high the converter is either overranged or underranged on I-channel or Q-channel. Note that both channels share a common OF pin. OF is disabled when I-channel is in sleep or nap mode.

APPLICATIONS INFORMATION

Output Clock

The ADC has a delayed version of the CLKQ input available as a digital output, CLKOUT. The falling edge of the CLKOUT pin can be used to latch the digital output data. CLKOUT is disabled when channel Q is in sleep or nap mode.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied to the same supply that powers the logic being driven. For example, if the converter drives a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply.

OV_{DD} can be powered with any voltage from 500mV up to the V_{DD} of the part. OGND can be powered with any volt-age from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{OE}$. $\overline{OE}$ high disables all data outputs including OF. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity. Channels I and Q have independent output enable pins ($\overline{OEI}$, $\overline{OEQ}$.)

Digital Output Multiplexer

The digital outputs of the ADC can be multiplexed onto a single data bus. The MUX pin is a digital input that swaps the two data busses. If MUX is high, I-channel comes out on DI0 to DI13; Q-channel comes out on DQ0 to DQ13. If MUX is low, the output busses are swapped and I-channel comes out on DQ0 to DQ13; Q-channel comes out on DI0 to DI13. To multiplex both channels onto a single output bus, connect MUX, CLKI and CLKQ together (see the Timing Diagrams for the multiplexed mode.) The multiplexed data is available on either data bus – the unused data bus can be disabled with its $\overline{OE}$ pin.

Design Example – UMTS Uplink FDD System

The LTM9004 can be used with an RF front end to build a complete UMTS band uplink receiver. An RF front end will consist of a diplexer, along with one or more LNAs and bandpass filters. Here is an example of typical performance for such a frontend:

Rx frequency range:	1920 to 1980 MHz
RF gain:	15dB maximum
AGC range:	20dB
Noise figure:	1.6dB
IIP2:	50dBm
IIP3:	0dBm
P1dB:	–9.5dBm
Rejection at 20MHz:	2dB
Rejection at Tx band:	95dB

Minimum performance of the receiver is detailed in the 3GPP TS25.104 V7.4.0 specification. We will use the Medium Area Basestation in Operating Band I for this example.

Sensitivity is a primary consideration for the receiver; the requirement is ≤–111dBm, for an input SNR of –19.8dB/5MHz. That means the effective noise floor at the receiver input must be ≤–158.2dBm/Hz. Given the effective noise contribution of the RF frontend, the maximum allowable noise due to the LTM9004 must then be –142.2dBm/Hz. Typical input noise for the LTM9004 is –148.3dBm/Hz, which translates to a calculated system sensitivity of –116.7dBm.

Typically such a receiver enjoys the benefits of some DSP filtering of the digitized signal after the ADC. In this case assume the DSP filter is a 64 tap RRC lowpass with alpha equal to 0.22. To operate in the presence of co-channel interfering signals, the receiver must have sufficient dynamic range at maximum sensitivity. The UMTS specification calls for a maximum co-channel interferer of –73dBm. Note the input level for –1dBFS within the IF passband of the LTM9004 is –15.1dBm for a modulated signal with a 10dB crest factor. The tone interferer amounts to a peak digitized signal level of –42.6dBFS.

APPLICATIONS INFORMATION

With the RF AGC set for minimum gain, the receiver must be able to demodulate the largest anticipated desired signal from the handset. This requirement ultimately sets the maximum signal the LTM9004 must accommodate at or below –1dBFS. Assuming a handset average power of +28dBm, the minimum path loss called out in the specification is 53dB. The maximum signal level is then –25dBm at the receiver input, or –30dBm at the LTM9004 input. This is equivalent to –14.6dBFS peak.

There are several blocker signals detailed in the UMTS system specification. The sensitivity may degrade to no more than –105dBm in the presence of these signals. The first of these is an adjacent channel 5MHz away, at a level of –42dBm. This amounts to a peak digitized signal level of –11.6dBFS. The resulting sensitivity is then –112.8dBm.

The receiver must also contend with a –35dBm interfering channel ≥10MHz away. The RF frontend will offer no rejection of this channel, so it amounts to –6.6dBFS peak, and the resulting sensitivity is –109.2dBm.

Out of band blockers must also be accommodated, but these are at the same level as the inband blockers which have already been addressed.

In all of these cases, the typical input level for –1dBFS of the LTM9004 is well above the maximum anticipated signal levels. Note that the crest factor for the modulated channels will be on the order of 10dB to 12dB, so the largest of these will reach a peak power of approximately –6.5dBFS at the module output.

The largest blocking signal is the –15dBm CW tone ≥20MHz beyond the receive band edges. The RF frontend will offer 37dB rejection of this tone, so it will appear at the input of the LTM9004 at –32dBm. Here again, a signal at this level must not desensitize the baseband module. The equivalent digitized level is only –41.6dBFS peak, so there is no effect upon sensitivity.

Another source of undesired signal power is leakage from the transmitter. Since this is an FDD application, the receiver described herein will be coupled with a transmitter operating simultaneously. The transmitter output level is assumed to be ≤+38dBm, with a transmit to receive isolation of 95dB. Leakage appearing at the LTM9004 input is then –42dBm, offset from the receive signal by at least 130MHz. The equivalent digitized level is only –76.6dBFS peak, so there is no desensitization.

One challenge of direct conversion architectures is 2nd order linearity. Insufficient 2nd order linearity will allow any signal, wanted or unwanted, to create DC offset or pseudo-random noise at baseband. The blocking signals detailed above will then degrade sensitivity if this pseudo-random noise approaches the noise level of the receiver. The system specification allows for sensitivity degradation in the presence of these blockers in each case. Per the system specification, the –35dBm blocking channel may degrade sensitivity to –105dBm. This is equivalent to increasing the effective input noise of the receiver to –148.2dBm/Hz. The 2nd order distortion produced by the LTM9004 input is about 18dB below this level, and the resulting predicted sensitivity is –116.6dBm.

The –15dBm CW blocker will also give rise to a 2nd order product; in this case the product is a DC offset. DC offset is undesirable, as it reduces the maximum signal the A/D converter can process. The one sure way to alleviate the effects of DC offset is to ensure the 2nd order linearity of the baseband module is high enough. The predicted DC offset due to this signal is <1mV at the ADC input.

Note that the transmitter leakage is not included in the system specification, so the sensitivity degradation due to this signal must be held to a minimum. The 2nd order distortion generated in the LTM9004 is such that the loss of sensitivity will be <0.1dB.

There is only one requirement for 3rd order linearity in the specification. In the presence of two interferers, the sensitivity must not degrade below –105dBm. The interferers are a CW tone and a WCDMA channel at –44dBm each. These will appear at the LTM9004 input at –29dBm each. Their frequencies are such that they are 10MHz and 20MHz away from the desired channel, so the 3rd order intermodulation product falls at baseband. Here again, this product appears as pseudo-random noise and thus will reduce signal to noise ratio. For a sensitivity of –105dBm, the allowable 3rd order distortion referred to the receiver input is then –148.2dBm/Hz. The 3rd order distortion produced in the LTM9004 is about 23dB below this level, and the predicted sensitivity degradation is <0.1dB.

APPLICATIONS INFORMATION

Supply Sequencing

The V_{CC} pins provide the supply to the mixer and all amplifiers and the V_{DD} pins provide the supply to the ADC. The mixer, amplifiers and ADC are separate integrated circuits within the LTM9004; however, there are no supply sequencing considerations beyond standard practice.

Grounding and Bypassing

The LTM9004 requires a printed circuit board with a clean unbroken ground plane; a multilayer board with an internal ground plane is recommended. The pinout of the LTM9004 has been optimized for a flowthrough layout so that the interaction between inputs and digital outputs is minimized. A continuous row of ground pads facilitates a layout that ensures that digital and analog signal lines are separated as much as possible.

The LTM9004 is internally bypassed with the ADC (V_{DD}), mixer and amplifier (V_{CC}) supplies returning to a common ground (GND). The digital output supply (OV_{DD}) is returned to OGND. A 0.1µF bypass capacitor should be placed at each of the two OV_{DD} pins. Additional bypass capacitance is optional and may be required if power supply noise is significant.

Heat Transfer

Most of the heat generated by the LTM9004 is transferred through the bottom-side ground pads. For good electrical and thermal performance, it is critical that all ground pins are connected to a ground plane of sufficient area with as many vias as possible.

Recommended Layout

The high integration of the LTM9004 makes the PCB board layout simple. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for ground. This helps to dissipate heat in the package through the board and also helps to shield sensitive on-board analog signals. Common ground (GND) and output ground (OGND) are electrically isolated on the LTM9004, but can be connected on the PCB underneath the part to provide a common return path.
- Use multiple ground vias. Using as many vias as possible helps to improve the thermal performance of the board and creates necessary barriers separating analog and digital traces on the board at high frequencies.
- Separate analog and digital traces as much as possible, using vias to create high frequency barriers. This will reduce digital feedback that can reduce the signal-to-noise ratio (SNR) and dynamic range of the LTM9004.

Figures 11 through 14 give a good example of the recommended layout.

The quality of the paste print is an important factor in producing high yield assemblies. It is recommended to use a type 3 or 4 printing no-clean solder paste. The solder stencil design should follow the guidelines outlined in Application Note 100.

The LTM9004 employs gold-finished pads for use with Pb-based or tin-based solder paste. It is inherently Pb-free and complies with the JEDEC (e4) standard. The materials declaration is available online at http://www.linear.com/leadfree/mat_dec.jsp.

APPLICATIONS INFORMATION

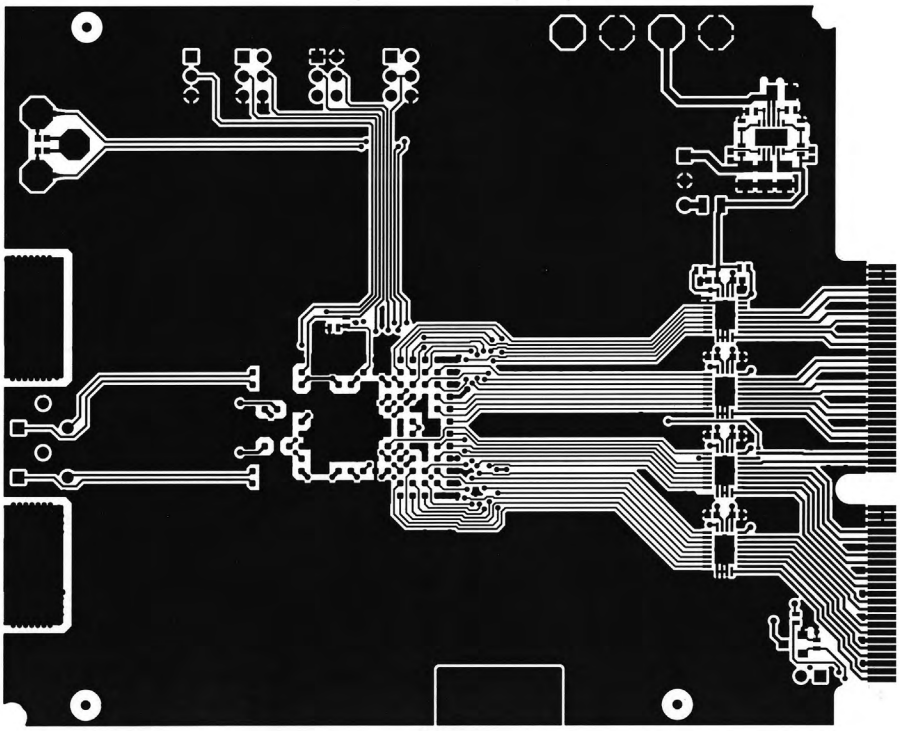


Figure 11. Layer 1

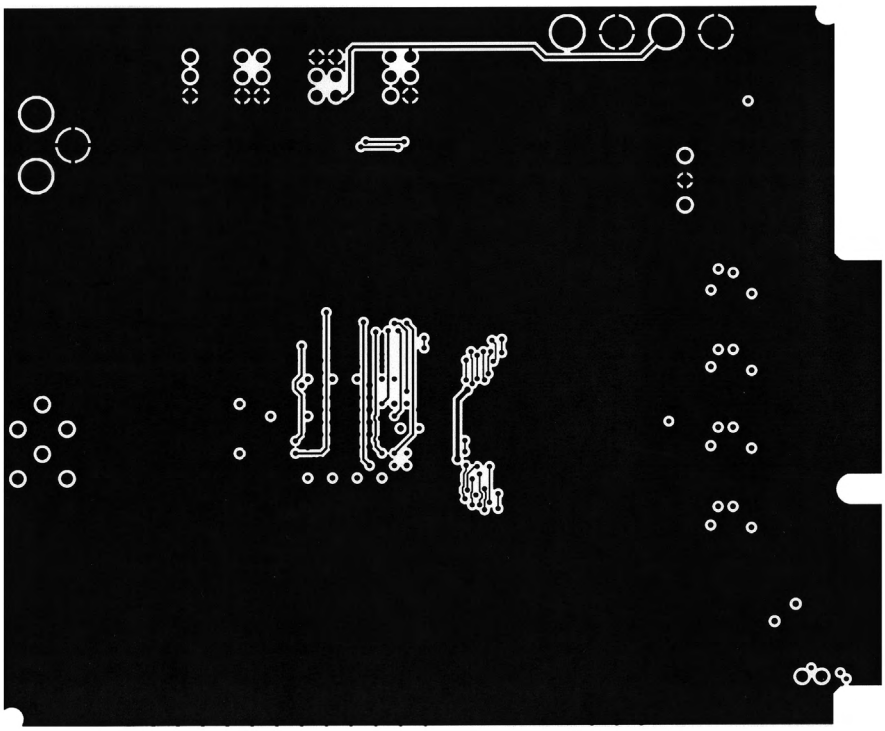


Figure 12. Layer 2

APPLICATIONS INFORMATION

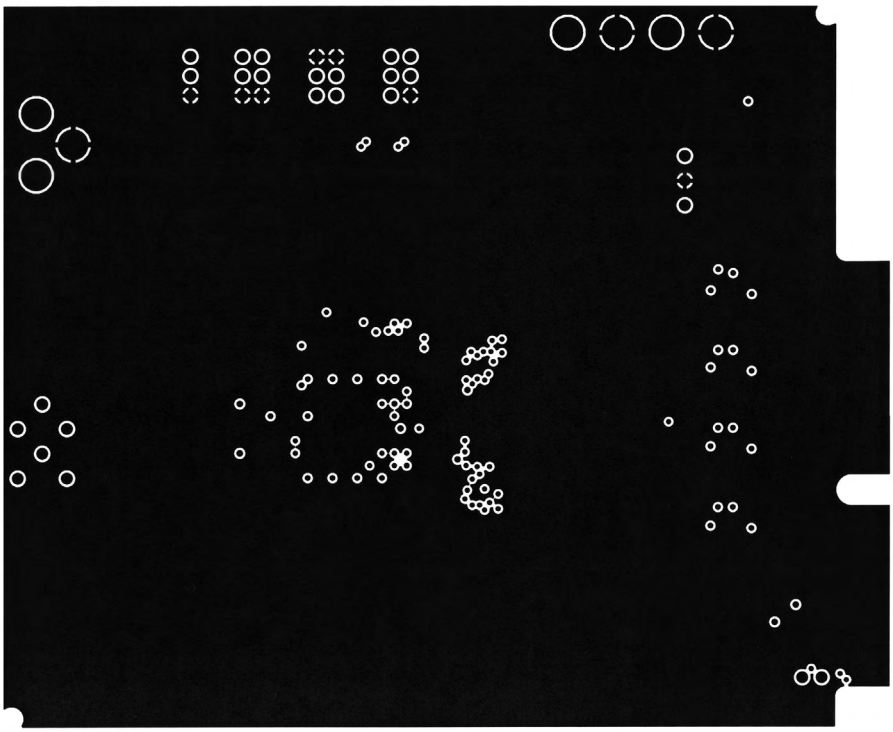


Figure 13. Layer 3

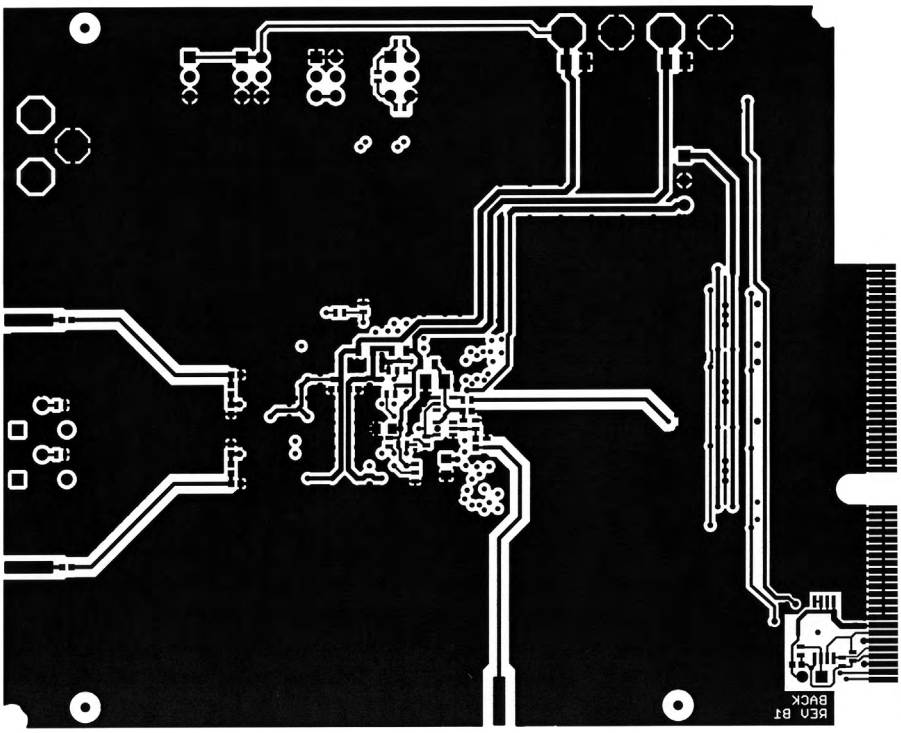
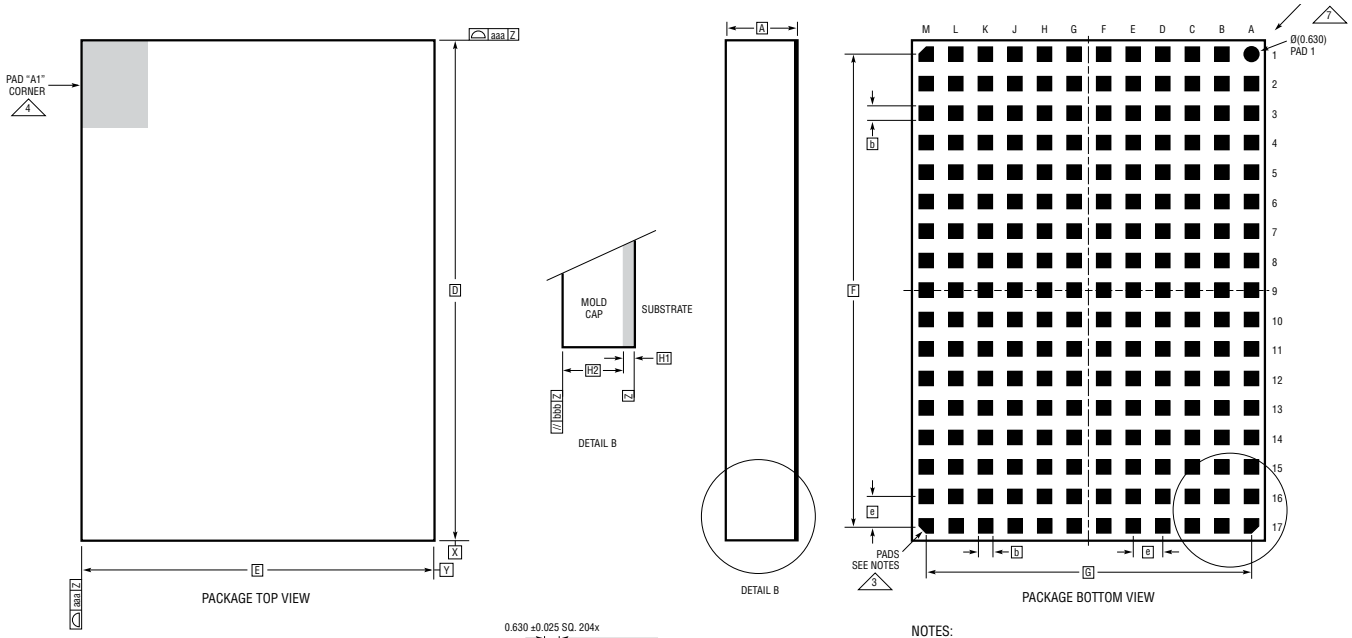


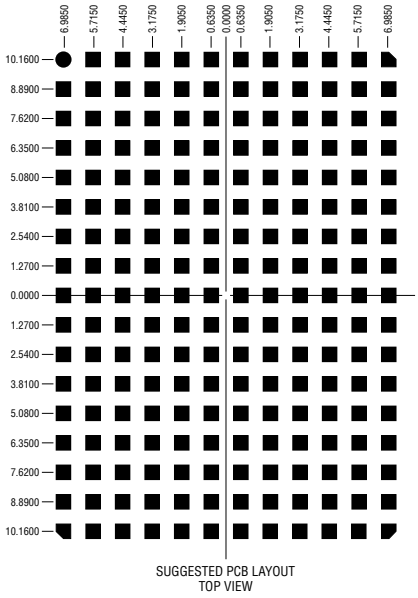
Figure 14. Layer 4

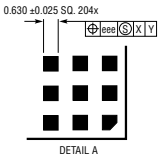
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LGA Package
204-Lead (22mm × 15mm × 2.91mm)
(Reference LTC DWG # 05-08-1822 Rev C)

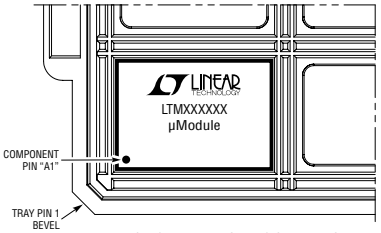






DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.81	2.91	3.01	
b	0.60	0.63	0.66	
D		22.0		
E		15.0		
e		1.27		
F		20.32		
G		13.97		
H1	0.36	0.41	0.46	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 204				

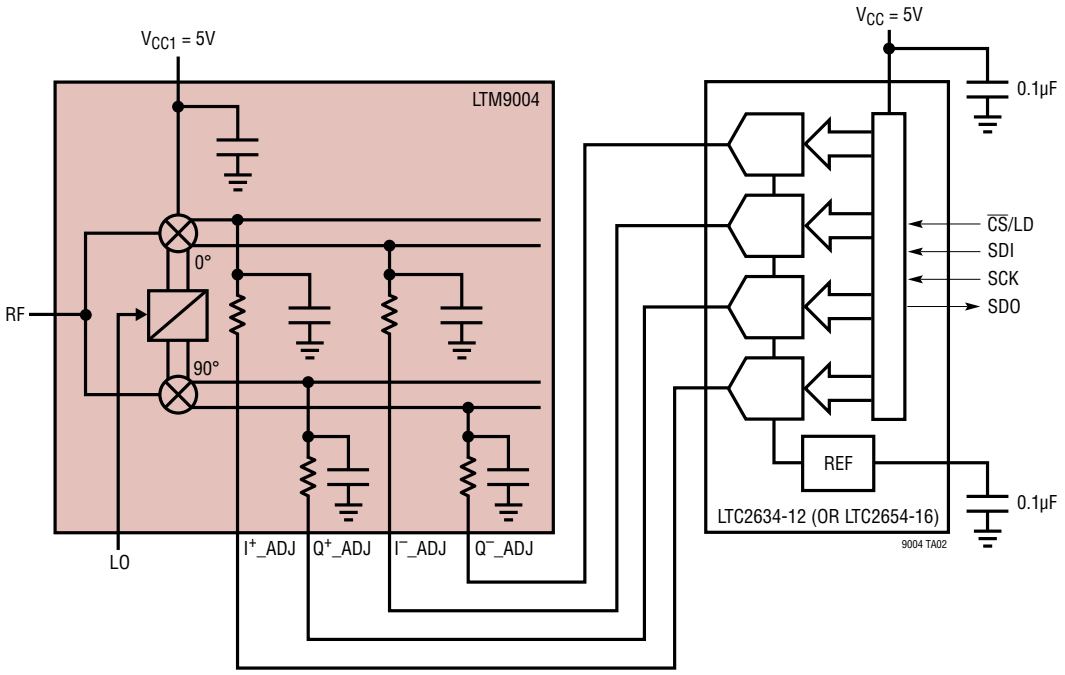
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 204
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/14	Updated package drawing, height changed to 2.91mm	2, 26

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2295	Dual 14-Bit, 10Msps ADC	120mW, 74.4dB SNR, 9mm x 9mm QFN
LTC2296	Dual 14-Bit, 25Msps ADC	150mW, 74dB SNR, 9mm x 9mm QFN
LTC2297	Dual 14-Bit, 40Msps ADC	240mW, 74dB SNR, 9mm x 9mm QFN
LTC2298	Dual 14-Bit, 65Msps ADC	410mW, 74dB SNR, 9mm x 9mm QFN
LTC2299	Dual 14-Bit, 80Msps ADC	445mW, 73dB SNR, 9mm x 9mm QFN
LTC2284	Dual 14-Bit, 105Msps ADC	540mW, 72.4dB SNR, 88dB SFDR, 64-pin QFN
LTC2285	Dual 14-Bit, 125Msps ADC	790mW, 72.4dB SNR, 88dB SFDR, 64-pin QFN
LT5575	800MHz to 2.7GHz High Linearity Direct Conversion Quadrature Demodulator	60dBm IIP2 at 1.9GHz, NF = 12.7dB, Low DC Offsets
LTC6404-1/ LTC6404-2	600MHz, Low Noise, AC Precision Fully Differential Input/Output Amplifier/Driver	3V or 5V, 1.5nV/$\sqrt{Hz}$, Very Low Distortion –92dBc at 10MHz
LTC6406	3GHz Low Noise, Rail-to-Rail Input Differential ADC Driver	Low Noise: 1.6nV/$\sqrt{Hz}$, Low Power: 18µA
LTM9001	16-Bit IF/Baseband Receiver Subsystem	Integrated 16-Bit, 130Msps ADC, Passive Filter and Fixed Gain Differential Amplifier, 11.25mm × 11.25mm LGA Package
LTM9002	14-Bit Dual-Channel IF/Baseband Receiver Subsystem	Integrated, Dual 14-Bit 125Msps ADCs, Passive Filters and Fixed Gain Differential Amplifiers, Up to 300MHz IF Range, 15mm × 11.25mm LGA Package

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