The P1012 and P1021 processors have an advanced set of features for ease of use. The 256 KB L2 cache offers incremental configuration to partition the cache between the two cores or to configure it as SRAM or stashing memory.

Target Applications

The P1012 and P1021 processors serve a wide variety of applications and are well suited for various combinations of data plane and control plane workloads in networking and telecom applications. With an available junction temperature range of –40 ºC to +125 ºC, the devices can be used in powersensitive defense and industrial applications, and outdoor environments less protected from the environment. The devices primarily target applications such as networking and telecom linecards.

A multiservice router or business gateway requires a combination of high performance and a rich set of peripherals to support the datapath throughputs and required system functionality. The P1012 and P1021 devices offer a scalable platform to develop a range of products that can support the same feature set. The QUICC Engine module, as well as integrated 10/100/1000 Ethernet controllers with classification and QoS capabilities, are ideal for managing the datapath traffic between the LAN and WAN interface. PCI Express ports can provide connectivity to IEEE 802.11n radio cards for wireless support, TDM for legacy phone interfaces to support voice and the USB or SD/MMC interfaces can be used to support local storage. The integrated security engine can provide encrypted secure communications for remote users with VPN support.

Technical Specifications

- Single (P1012) and dual (P1021) high-performance Power Architecture e500 cores
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 533 MHz–800 MHz core clock frequency
- 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- Three 10/100/1000 Mb/s enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE 1588 support
  - Lossless flow control
  - RGMII, SGMII
- High-speed interfaces (not all available simultaneously)
  - Four SerDes to 3.125 GHz multiplexed across controllers
  - Two PCI Express controllers
  - Two SGMII interfaces
- QUICC Engine module
  - UTOPIA-L2
  - Up to two 10/100 Ethernet interfaces
  - Up to four T1/E1/J1/E3 or DS-3 serial interfaces
  - Up to four HDLC interfaces with 128 channels of HDLC
  - Up to four BISYNC interfaces
  - Up to four UART interfaces
  - SPI interfaces
  - GPIO
- High-speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Enhanced secure digital host controller
- Serial peripheral interface
- Integrated security engine (SEC 3.3)
  - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Snow 3G and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (e.g., IPsec, SSL, SRTP, WiMAX)
  - XOR acceleration
- 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- Four-channel DMA controller
- Two I^2C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals
- Package: 689-pin wirebond power-BGA (TEPBGA2)

QorIQ P1021 Features

QorIQ Platform	Device	Cores	Top Core Frequency	L2 Size	DDR 2/3 Support	GE Ports	QUICC Engine	SerDes	PCI Express	Serial RapidIO	TDM
P1	P1011	1	800 MHz	256 KB	32-bit with ECC	3	N/A	4	2	N/A	Yes
P1	P1020	2	800 MHz	256 KB	32-bit with ECC	3	N/A	4	2	N/A	Yes
P1	P1012	1	800 MHz	256 KB	32-bit with ECC	3	Yes	4	2	N/A	In QUICC Engine
P1	P1021	2	800 MHz	256 KB	32-bit with ECC	3	Yes	4	2	N/A	In QUICC Engine
P2	P2010	1	1200 MHz	512 KB	64-bit with ECC	3	N/A	4	3	2	N/A
P2	P2020	2	1200 MHz	512 KB	64-bit with ECC	3	N/A	4	3	2	N/A

For more information, please visit freescale.com/QorIQ

Document Number: QORIQP1021FS REV 3

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