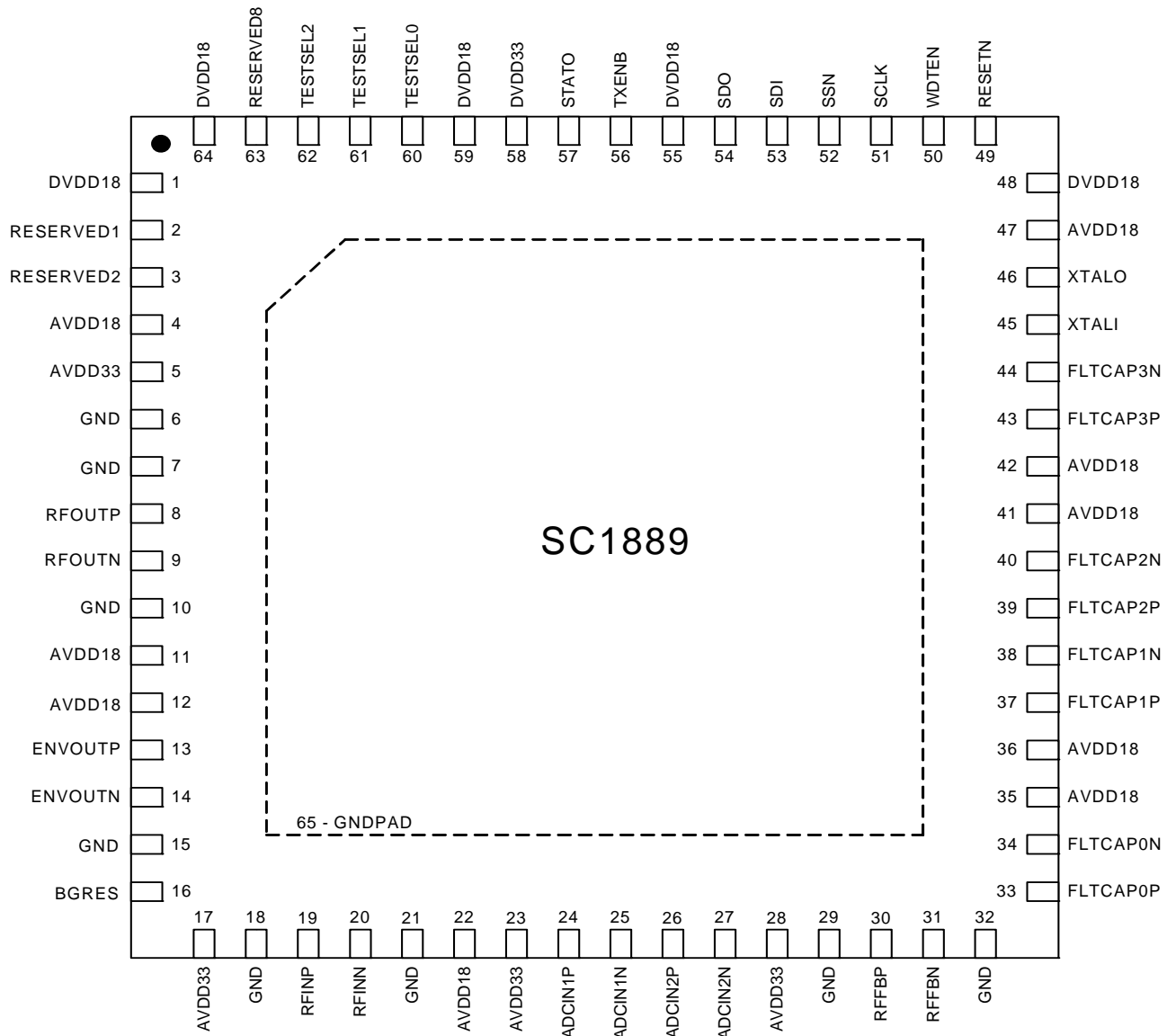


Pin Configuration (Top View)



Pin Description

PIN	NAME	TYPE	FUNCTION
1	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
2	RESERVED1	Analog Out Reserved	Do not connect. Reserved for internal use.
3	RESERVED2	Analog Out Reserved	Do not connect. Reserved for internal use.
4	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
5	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
6	GND	Supply	Ground.
7	GND	RF Shield	Ground for shield of RF signal.
8	RFOUTP	Analog Out	RF Output Signal, differential output. See S-parameters for complex impedance values.
9	RFOUTN		
10	GND	RF Shield	Ground for shield of RF signal.
11	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
12	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
13	ENVOUTP	Analog Out Reserved	Envelope Out. Do not connect. Reserved for future use.
14	ENVOUTN		
15	GND	Supply	Ground.
16	BGRES	Analog In	Bandgap Resistor.
17	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
18	GND	RF Shield	Ground for shield of RF signal.
19	RFINP	Analog In	RF Input Signal, differential input. See S-parameters for complex impedance values.
20	RFINN		
21	GND	RF Shield	Ground for shield of RF signal.
22	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
23	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
24	ADCIN1P	Analog In Reserved	Do not connect. Reserved for future use. .
25	ADCIN1N		
26	ADCIN2P	Analog In Reserved	Do not connect. Reserved for future use.
27	ADCIN2N		
28	AVDD33	Supply	+3.3V DC Supply Voltage for analog circuits.
29	GND	RF Shield	Ground for shield of RF signal.
30	RFFBP	Analog In	RF Feedback Signal, differential input. See S-parameters for complex impedance values.
31	RFFBN		
32	GND	RF Shield	Ground for shield of RF signal.

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
33	FLTCAP0P	Analog Out	Dedicated external filter capacitor #0.
34	FLTCAP0N		
35	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
36	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
37	FLTCAP1P	Analog Out	Dedicated external filter capacitor #1.
38	FLTCAP1N		
39	FLTCAP2P	Analog Out	Dedicated external filter capacitor #2.
40	FLTCAP2N		
41	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
42	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
43	FLTCAP3P	Analog Out	Dedicated external filter capacitor #3.
44	FLTCAP3N		
45	XTALI	Analog In	20 MHz clock reference from crystal or resonator.
46	XTALO	Analog Out	
47	AVDD18	Supply	+1.8V DC Supply Voltage for analog circuits.
48	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
49	RESETN	Digital In	Reset when "Low". Has internal pullup to DVDD33.
50	WDTEN	Digital In	Watch Dog Timer Enable. WDTEN enabled when high. Has internal pullup to DVDD33. See applications schematic for further details.
51	SCLK	Digital In	SPI clock. Has internal pulldown to GND.
52	SSN	Digital In	SPI slave select enabled "Low". Has internal pullup to DVDD33.
53	SDI	Digital In	SPI slave data input to RFPAL. Has internal pulldown to GND.
54	SDO	Digital Out	SPI slave data output from RFPAL. Three-state. DVDD33 logic.
55	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
56	TXENB	Digital In Reserved	Transmit Enable. Do not connect. Reserved for future use. Has internal pullup to DVDD33. See applications schematic for further details.
57	STATO	Digital Out	General purpose Status Output as defined in Firmware Release Notes. Open-drain output with internal pullup to DVDD33.
58	DVDD33	Supply	+3.3V DC Supply Voltage for digital circuits.
59	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
60	TESTSEL0	Digital In	Test Select 0. Required for FW upgrades. Has internal pulldown to GND. See applications schematic for further details.
61	TESTSEL1	Digital In Reserved	Do not connect. Reserved for internal use. Has internal pulldown to GND.
62	TESTSEL2	Digital In Reserved	Do not connect. Reserved for internal use. Has internal pulldown to GND.
63	RESERVED8	Digital In Reserved	Do not connect. Reserved for internal use. Has internal pulldown to GND.
64	DVDD18	Supply	+1.8V DC Supply Voltage for digital circuits.
65	GNDPAD	Supply	Common Ground for entire integrated circuit. Also provides path for thermal dissipation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD33 to GND) -0.3V to +3.8V
 Supply Voltage (VDD18 to GND) -0.2 V to +2.2V
 Input Voltage (1.8V pins) ... -0.2V to (VDD18 + 0.2V)
 Input Voltage (3.3V pins) ... -0.3V to (VDD33 + 0.3V)
 Input into the Balun (RMS) +7dBm
 Junction Temperature +150°C
 Storage Temperature -65°C to +150°C

OPERATING RATING

Operating Case Temperature.....-40°C to +100°C

Warning: Any stress beyond the ranges indicated may damage the device permanently. The specified stress ratings do not imply functional performance in these ranges. Exposure of the device to the absolute maximum ratings for extended periods of time is likely to degrade the reliability of this product.

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage (VDD33 to GND)	3.1	3.3	3.5	V
Supply Voltage (VDD18 to GND)	1.7	1.8	1.9	V
Supply Peak Current (VDD33 to GND) ^{1,2,3, 5}		59		mA
Supply Peak Current (VDD18 to GND) ^{1,2,3, 5}		592		mA
Average Power Dissipation: Full-Scale Adaptation, Track, and PMU ^{3, 5}		1060		mW
Average Power Dissipation: Duty-Cycled Feedback ^{2,4,5}		420		mW

Note 1: Peak current includes supply decoupling network. Refer to Hardware Design Guide for proper sizing of the on-board regulators.

Note 2: Characterized at typical voltages, +25°C operating case temperature and 20MHz input signal BW.

Note 3: Continuous adaptation, tracking (100% duty-cycled feedback) and Power Measurement Unit active or inactive.

Note 4: Duty-cycled feedback power dissipations averaged over ON time of 100ms (9%) and OFF time of 1.024s (91%).

Note 5: Power dissipation may be FW dependent. Refer to the FW release notes for any changes to values listed above.

RADIO FREQUENCY SIGNALS

PARAMETER	SYMBOL	CONDITIONS	MIN	RECOMMENDED	MAX	UNITS
Operating Frequency ¹	f		698		2800	MHz
RFIN_BLN Range for Maximum Correction	P _{RFIN_BLN_P}	Peak power	-4	4	6	dBm
RFIN_BLN Range for Maximum Correction	P _{RFIN_BLN}	RMS power ²	-9	-6	-4	dBm
RFFB_BLN Range for Maximum Correction	P _{RFFB_BLN_P}	Peak power	-14	-4	-2	dBm
RFFB_BLN Range for Maximum Correction	P _{RFFB_BLN}	RMS power ²	-19	-14	-12	dBm
RFIN_BLN Operating Range	P _{RFIN_BLN}	RMS power ²	-40		-4	dBm
RFFB_BLN Operating Range	P _{RFFB_BLN}	RMS power ²	-45		-12	dBm
RF Input Signal Peak-to Avg. Ratio ³	PAR _{IN}	CCDF ⁴ probability=10 ⁻⁴		5 to 10		dB
Input Signal Bandwidth	BW _{signal}		1.2		40 or 60 ⁵	MHz
Noise Power ⁶		Referred to 0dBm at PA input		-138	-135	dBm/Hz

Note 1: See Operating Frequency Ranges table for frequency limits of each defined band.

Note 2: A peak to average ratio (PAR) of 5dB to 10dB is used for this table.

Note 3: Higher PAR values can be supported but at a reduction to a combination of the input signal range and IM correction limits.

Note 4: CCDF = Complementary cumulative distribution function; a measurement of peak to average ratio or crest factor.

Note 5: > 40MHz operation requires a fully occupied signal bandwidth.

Note 6: Worst case over PVT guaranteed by bench characterization.

OPERATING FREQUENCY RANGES

FREQUENCY RANGE ¹	RECOMMENDED APPLICATIONS	DESIGNATION
698MHz to 960MHz	Lowband cellular (698MHz to 960MHz)	-04
800MHz to 1450MHz	IF for SATCOMM (1000MHz to 1400MHz)	-05
1350MHz to 2450MHz	LTE for Japan (1400MHz to 1510MHz)	-06
1600MHz to 2800MHz	Highband cellular (1600MHz to 2800MHz)	-07

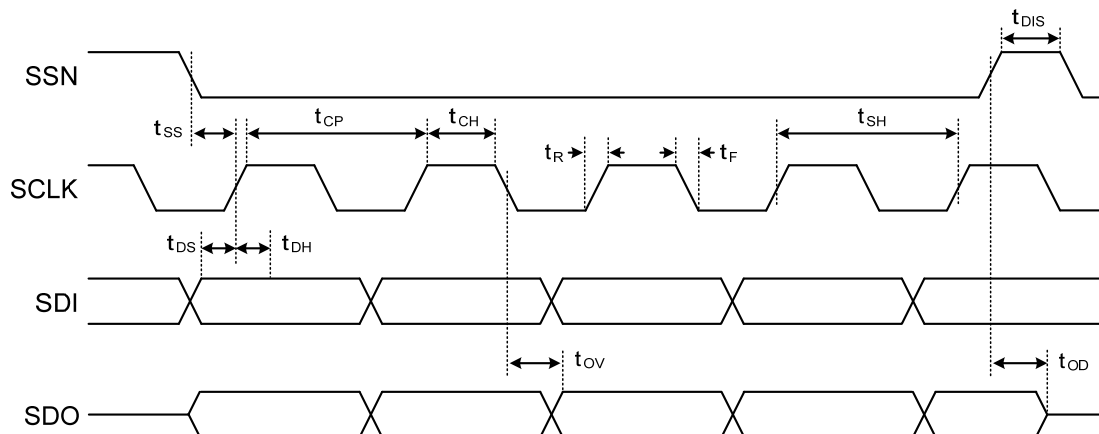
Note 1: Default is -07. May be reprogrammed by user for other ranges listed above. Refer to Design Guide for programming information.

DIGITAL I/O—DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS Input Logic-Low	V_{IL}		-0.3		0.8	V
CMOS Input Logic-High	V_{IH}	VDD = 3.3V	2.0			V
CMOS Output Logic-Low	V_{OL}				0.4	V
CMOS Output Logic-High	V_{OH}	VDD = 3.3V	2.4			V
SDO CMOS Output Current	I_{OL}/I_{OH}	Three-State	-4.0		+4.0	mA
STATO CMOS Output Current	I_{OL}/I_{OH}	Open Drain	-4.0		0.0	mA

SERIAL PERIPHERAL INTERFACE (SPI) BUS SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Select Setup Time	t_{SS}		100			ns
Select Hold Time	t_{SH}		250			ns
Select Disable Time	t_{DIS}		100			ns
Data Setup Time	t_{DS}		25			ns
Data Hold Time	t_{DH}		45			ns
Rise Time	t_R				25	ns
Fall Time	t_F				25	ns
Clock Period	t_{CP}		250			ns
Clock High Time	t_{CH}		100			ns
Time to Output Valid	t_{OV}				100	ns
Output Data Disable	t_{OD}				0	ns

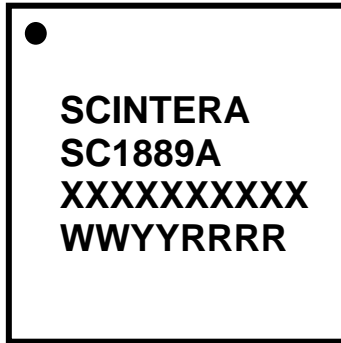


Use of the SPI interface offers the user access to certain monitoring and diagnostic functions as well as other planned advanced features. The SPI bus interface is also used to program the internal EEPROM, allowing changes to the operating frequency range, field upgrades and firmware updates.

CRYSTAL REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESR					50	Ω
Capacitive Load to Ground				10	12	pF
Frequency Accuracy					250	ppm
Frequency Drift		Including aging and temperature			100	ppm

Top Mark



LINE	TOP MARK	DESCRIPTION
1	SCINTERA	Company Name
2	SC1889	Product Part Number
2	A	Product Revision
2	-11	Product Configuration (PC): BLANK = RFPAL Base Configuration -11 = RFPAL + PMU configuration
3	XXXXXXXXXX	Foundry Lot Number (up to 10 characters)
4	WW	Date Code - Work Week
4	YY	Date Code - Year
4	RRRR	Reserved

ESD



ESD (Electrostatic Discharge) sensitive device. Although this product incorporates ESD protection circuitry, permanent damage may occur on devices subjected to electrostatic discharges. Proper ESD precautions are recommended to avoid performance degradation or device failure.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION CHARACTERISTICS

TEST METHODOLOGY	CLASS	VOLTAGE	UNIT
Human Body Model (per JESD22-A114)	1C	1000	V
Charge Device Model (per JESD22-C101)	II	250	V

Ordering Information

PART	DESCRIPTION
SC1889A-00B00	IC, RFPAL, 698MHz to 2800MHz, FW3.0.17.62
SC1889A-00B11	IC, RFPAL+PMU, 698MHz to 2800MHz, FW3.0.17.62

Note: Parts are lead(Pb)-free and RoHS-compliant.

Shipping designator:

E = 7" tape and reel.

Append shipping designator (E) at end of part number. If left blank, designates bulk shipping option.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 QFN	K6499MK+1	21-0765	90-0605

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0.1	8/14		—

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