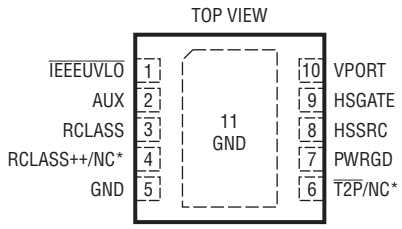
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

VPORT, HSSRC Voltages ..... –0.3V to 100V
HSGATE Current..... ±20mA
$\overline{\text{IEEEUVLO}}$, RCLASS,
RCLASS++ Voltages ..... –0.3V to 8V (and ≤ VPORT)
AUX Current..... ±1.4mA
$\overline{\text{T2P}}$, PWRGD Voltage ..... –0.3V to 100V
$\overline{\text{T2P}}$, PWRGD Current 5mA

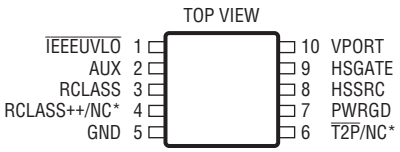
Operating Junction Temperature Range (Note 4)
LT4275AI/LT4275BI/LT4275CI.....–40°C to 85°C
LT4275AH/LT4275BH/LT4275CH .....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB GND



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JC} = 45°C/W

* RCLASS++ is not connected in the LT4275B/C versions. $\overline{\text{T2P}}$ is not connected in the LT4275C version.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	MAX PD POWER	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4275AIDD#PBF	LT4275AIDD#TRPBF	LGBS	90W	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT4275AHDD#PBF	LT4275AHDD#TRPBF	LGBS	90W	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT4275AIMS#PBF	LT4275AIMS#TRPBF	LTGBT	90W	10-Lead Plastic MSOP	–40°C to 85°C
LT4275AHMS#PBF	LT4275AHMS#TRPBF	LTGBT	90W	10-Lead Plastic MSOP	–40°C to 125°C
LT4275BIDD#PBF	LT4275BIDD#TRPBF	LGBV	25.5W	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT4275BHDD#PBF	LT4275BHDD#TRPBF	LGBV	25.5W	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT4275BIMS#PBF	LT4275BIMS#TRPBF	LTGBW	25.5W	10-Lead Plastic MSOP	–40°C to 85°C
LT4275BHMS#PBF	LT4275BHMS#TRPBF	LTGBW	25.5W	10-Lead Plastic MSOP	–40°C to 125°C
LT4275CIDD#PBF	LT4275CIDD#TRPBF	LGBX	13W	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT4275CHDD#PBF	LT4275CHDD#TRPBF	LGBX	13W	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT4275CIMS#PBF	LT4275CIMS#TRPBF	LTGBY	13W	10-Lead Plastic MSOP	–40°C to 85°C
LT4275CHMS#PBF	LT4275CHMS#TRPBF	LTGBY	13W	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	VPORT Operating Input Voltage	At VPORT Pin	●	23		60	V
V_{SIG}	VPORT Signature Range	At VPORT Pin	●	1.5		10	V
V_{CLASS}	VPORT Classification Range	At VPORT Pin	●	12.5		21	V
V_{MARK}	VPORT Mark Range	At VPORT Pin, Preceded by V_{CLASS}	●	5.6		10	V
	VPORT Aux Mode Range	At VPORT Pin, AUX > V_{AUXT}	●	8		60	V
	Signature/Class Hysteresis Window		●	1.0			V
V_{RESET}	Reset Threshold		●	2.6		5.6	V
V_{HSON}	Hot Swap Turn-On Voltage	$\overline{IEEEUVLO}$ = 0V $\overline{IEEEUVLO}$ Open	● ●		35 27	37 29	V V
V_{HSOFF}	Hot Swap Turn-Off Voltage	$\overline{IEEEUVLO}$ = 0V $\overline{IEEEUVLO}$ Open	● ●	30 21.5	31 22.5		V V
	Hot Swap On/Off Hysteresis Window		●	3			V
Supply Current							
	Supply Current	VPORT = HSSRC = 57V	●			2	mA
	Supply Current During Classification	VPORT = 17.5V, RCLASS and RCLASS++ Open	●	0.4	0.7	1.1	mA
	Supply Current During Mark Event	V_{MARK}	●	0.5		2.2	mA
Signature and Classification							
	Signature Resistance	V_{SIG} (Note 2)	●	23.7	24.4	25.2	kΩ
	Signature Resistance During Mark Event	V_{MARK} (Note 2)	●	5.8	8.3	11	kΩ
V_{RCLS}	RCLASS/RCLASS++ Operating Voltage	–10mA ≥ I_{RCLASS} ≥ –36mA, V_{CLASS}	●	1.32	1.40	1.43	V
	Classification Stability Time	VPORT Step to 17.5V, RCLASS = 34.8Ω	●			2	ms
Analog/Digital Interface							
V_{AUXT}	AUX Threshold		●	6.1	6.3	6.5	V
I_{AUXH}	AUX Pin Hysteresis Current	AUX = 6.1V	●	4	5.8	8	µA
	$\overline{T2P}$ Output Low	1mA Load (LT4275A/LT4275B Only)	●			0.8	V
	PWRGD Output Low	1mA Load	●			0.8	V
	PWRGD Leakage Current	PWRGD = 60V	●			5	µA
	$\overline{T2P}$ Leakage Current	$\overline{T2P}$ = 60V	●			5	µA
Hot Swap Control							
I_{GPU}	HSGATE Pull-Up Current	V_{HSGATE} – V_{HSSRC} = 5V, V_{PORT} > 42V, Out of Pin	●	18	22	27	µA
V_{GOC}	HSGATE Open Circuit Voltage	V_{HSGATE} – V_{HSSRC}, 0µA to 10µA Load with Respect to HSSRC	●	10		18	V
	HSGATE Pull-Down Current	V_{HSGATE} – V_{HSSRC} = 5V	●	200			µA
Timing							
f_{T2P}	$\overline{T2P}$ Frequency	After PWRGD Valid, if LTPoE++ PSE Is Mutually Identified	●	690	840	990	Hz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

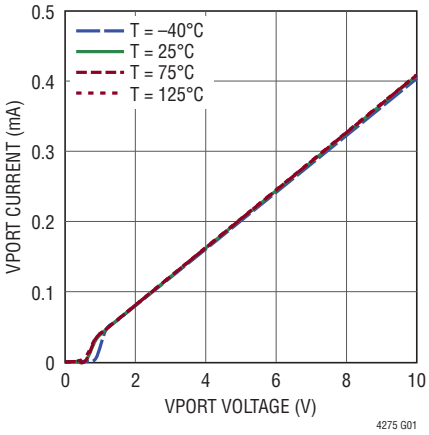
Note 2: Signature resistance specifications do not include resistance added by the external diode bridge which can add as much as 1.1k to the port resistance.

Note 3: All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

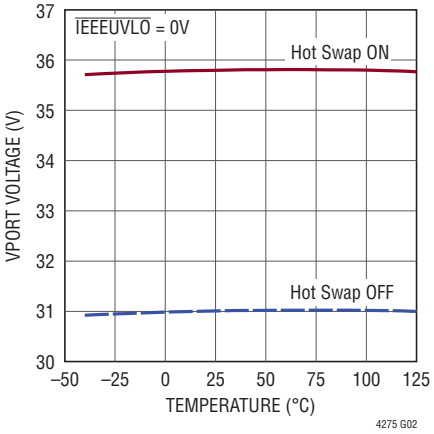
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

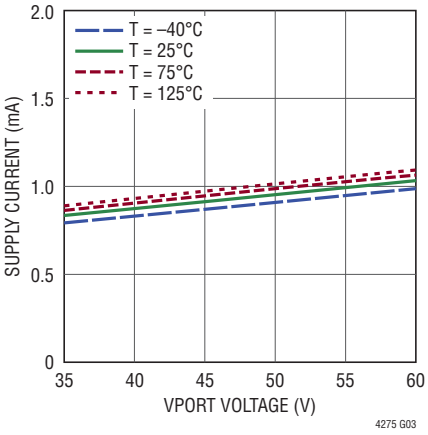
VPORT Current vs VPORT Voltage 25k Detection Range



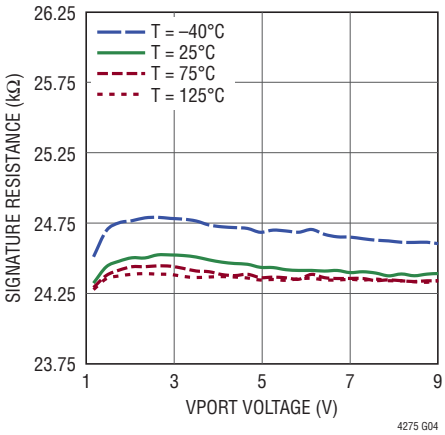
VPORT Hot Swap Thresholds



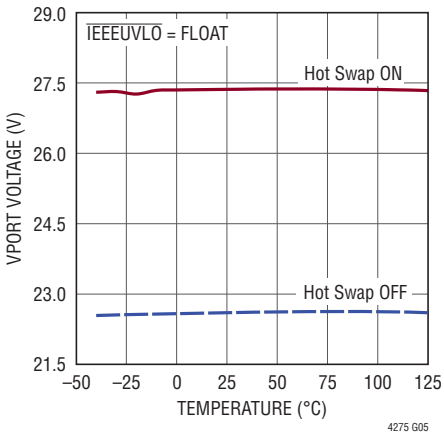
Supply Current During Power-On



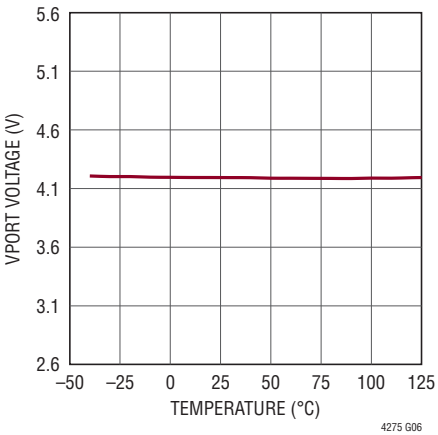
Signature Resistance vs Input Voltage



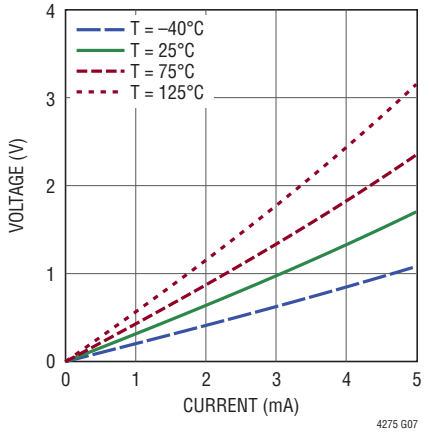
VPORT Hot Swap Thresholds



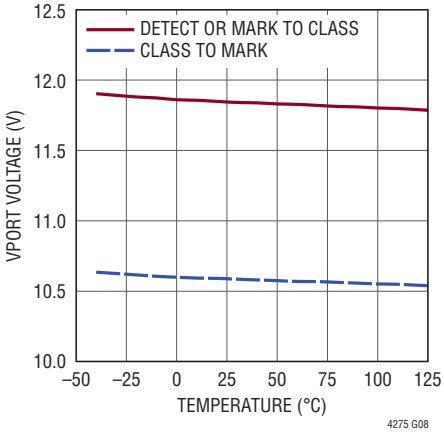
Reset Threshold



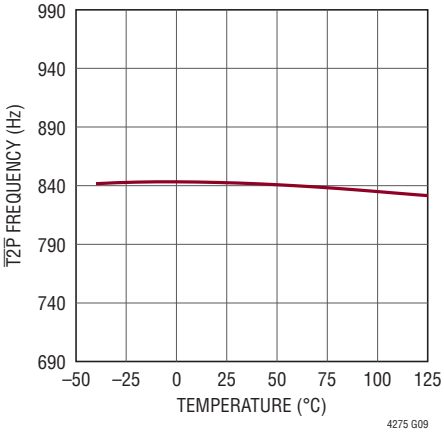
PWRGD, $\overline{T2P}$ Output Low Voltage vs Current



VPORT Classification Thresholds



$\overline{T2P}$ Frequency



PIN FUNCTIONS

$\overline{\text{IEEEUVLO}}$ (Pin 1): Hot Swap Turn-on Threshold Level Control. Connect to ground for IEEE compliant turn-on and turn-off (UVLO) voltage thresholds. Leave open for lower turn-on and turn-off voltage thresholds.

AUX (Pin 2): Auxiliary Sense. Assert AUX via a resistive divider from the auxiliary power input to set the voltage at which the auxiliary supply takes over. Asserting AUX pulls down HSGATE, disconnects the signature resistor, disables classification and floats the PWRGD pin. The AUX pin sinks I_{AUXH} when below its threshold voltage of V_{AUXT} to provide hysteresis. Tie to GND when not used.

RCLASS (Pin 3): Programmable PoE Classification Resistor. See Table 1.

RCLASS++ (Pin 4, LT4275A Only): Programmable LTPoE++ Classification Resistor. This pin is not connected on the LT4275B/LT4275C. See Table 1.

GND (Pin 5): Ground Pin. Must be soldered to PCB GND.

$\overline{\text{T2P}}$ (Pin 6, LT4275A/LT4275B Only): PSE Type Indicator, Open-Drain Output. $\overline{\text{T2P}}$ floats for a 13W PSE. $\overline{\text{T2P}}$ pulls down for a 25.5W PSE. $\overline{\text{T2P}}$ pulls down at f_{T2P} with a 50% (typical) duty cycle to indicate the presence of an LTPoE++ PSE. $\overline{\text{T2P}}$ is valid after PWRGD is active. This pin is not connected on the LT4275C. See the Applications Information section for behavior when using the AUX pin.

PWRGD (Pin 7): Power Good Indicator, Open-Drain Output. Pulls down during V_{CLASS} and inrush.

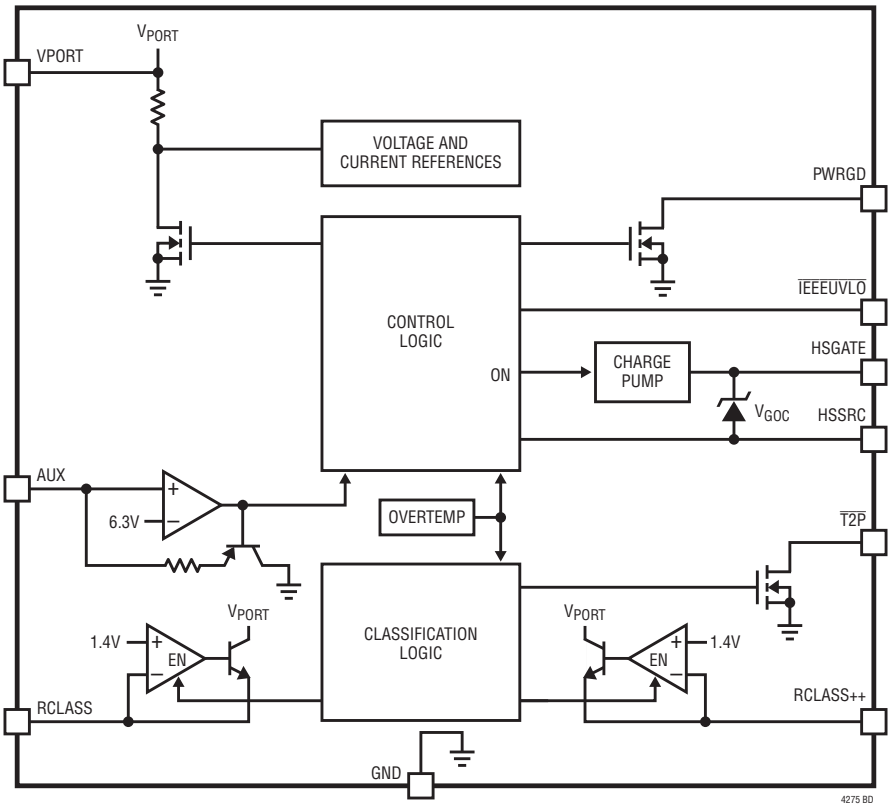
HSSRC (Pin 8): External Hot Swap MOSFET Source. Connect to source of the external MOSFET.

HSGATE (Pin 9): External Hot Swap MOSFET Gate Control, Output. Connect to gate of the external MOSFET.

VPORT (Pin 10): PD interface upper power rail and external Hot Swap MOSFET drain connection.

Exposed Pad (Pin 11, DFN Package Only): GND. Must be soldered to PCB GND.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as products take advantage of DC power and high speed data available from a single RJ45 connector. Powered device (PD) equipment vendors are running into the 25.5W power limit established by the IEEE 802.3 standard. The LT4275A allows higher power while maintaining backwards compatibility with existing PSE systems. The LT4275 utilizes a low $R_{DS(ON)}$ N-channel MOSFET to maximize efficiency and delivered power. Heat is also reduced, easing thermal design.

MODES OF OPERATION

The LT4275 has several modes of operation depending on the input voltage sequence applied to the VPORT pin. These modes include 25kΩ signature detection, classification, mark, inrush and powered on.

DETECTION

During detection, the PSE looks for a 25kΩ signature resistor which identifies the device as a PD. The PSE will apply two voltages in the range of 2.8V to 10V and measure the corresponding currents. Figure 1 shows the detection voltages. The PSE calculates the signature resistance using a ΔV/ΔI measurement technique.

The LT4275 presents its precision, temperature-compensated 24.4k resistor between the VPORT and GND pins, allowing the PSE to recognize a PD is present and requesting power to be applied. The LT4275 signature resistor is smaller than 25k to compensate for the additional series resistance introduced by the IEEE required bridge.

CLASSIFICATION

The detection/classification process varies depending on whether the PSE is Type 1, Type 2, or LTPoE++. A Type 2 PSE may use Type 1 classification signaling and later renegotiate a higher power classification with the PD over the data layer.

A Type 1 PSE, after a successful detection, may apply a classification probe voltage of 15.5V to 20.5V and measure current.

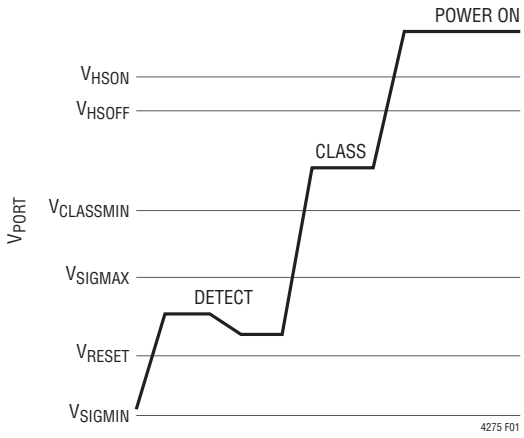


Figure 1. Type 1 Detect/Class Signaling Waveform

A Type 2 PSE may declare the availability of high power by performing 2-event (Physical Layer) classification or by communicating over the (Data Link Layer) high speed data line. A Type 2 PD must recognize both types of communication. Since Layer 2 communications takes place directly between the PSE and the PD application, the LT4275A/LT4275B responsibility ends with supporting 2-event classification.

In 2-event classification, a Type 2 PSE probes for power classification twice as shown in Figure 2. The LT4275A or LT4275B recognizes this and pulls the $\overline{T2P}$ pin down to signal the load that Type 2 power is available. If an LT4275A senses an LTPoE++ PSE it alternates between pulling $\overline{T2P}$ down and floating $\overline{T2P}$ at a rate of f_{T2P}.

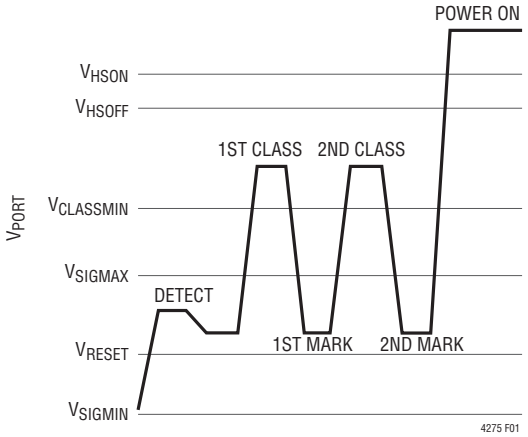


Figure 2. Type 2 Detect/Class Signaling Waveform

APPLICATIONS INFORMATION

Table 1. Classification Codes, Power Levels and Resistor Selection

CLASS	PD POWER AVAILABLE	PD TYPE	NOMINAL CLASS CURRENT	LT4275 GRADE CAPABILITY			RESISTOR	
				A	B	C	R_{CLS}	R_{CLS}++
0	13W	Type 1	<0.4mA	✓	✓	✓	Open	Open
1	3.84W	Type 1	10.5mA	✓	✓	✓	140Ω	Open
2	6.49W	Type 1	18.5mA	✓	✓	✓	76.8Ω	Open
3	13W	Type 1	28mA	✓	✓	✓	49.9Ω	Open
4	25.5W	Type 2	40mA	✓	✓		34.8Ω	Open
4*	38.7W	LTPoE++	40mA	✓			Open	34.8Ω
4*	52.7W	LTPoE++	40mA	✓			140Ω	46.4Ω
4*	70W	LTPoE++	40mA	✓			76.8Ω	64.9Ω
4*	90W	LTPoE++	40mA	✓			49.9Ω	118Ω

*An LTPoE++ PD will be classified as class 4 by an IEEE 802.3 compliant PSE.

LTPoE++ CLASSIFICATION

The LT4275A allows higher power allocation while maintaining backwards compatibility with existing PSE systems by extending the classification signaling of IEEE 802.3. Linear Technology PSE controllers that are capable of LTPoE++ are listed in the Related Parts section. IEEE PSEs will classify an LTPoE++ PD as a Type 2 PD.

SIGNATURE CORRUPT DURING MARK

During the mark state, the LT4275 presents <11kΩ to the port as required by the IEEE specification.

INRUSH AND POWERED ON

Once the PSE detects and optionally classifies the PD, the PSE then powers on the PD. When the port voltage rises above the V_{HSON} threshold, it begins to source I_{GPU} out of the HSGATE pin. This current flows into an external capacitor (C_{GATE} in Figure 3) that causes a voltage to ramp up the gate of the external MOSFET. The external MOSFET acts as a source follower and ramps the voltage up on the output bulk capacitor (C_{PORT} in Figure 3) thereby determining the inrush current (I_{INRUSH} in Figure 3).

To meet IEEE requirements, design I_{INRUSH} to be approximately 100mA. See equation below:

$$I_{INRUSH} = I_{GPU} \bullet \frac{C_{PORT}}{C_{GATE}}$$

The LT4275 internal charge pump provides an N-channel MOSFET solution, eliminating a larger and more costly P-channel FET. The low $R_{DS(ON)}$ MOSFET also maximizes power delivery and efficiency, reduces power and heat dissipation, and eases thermal design.

The PWRGD pin is held low by its open drain output until HSGATE charges up to approximately 7V above HSSRC. The PWRGD pin is used to hold off the isolated power supply until inrush is complete and the external MOSFET is fully enhanced. The HSGATE pin will remain high and the PWRGD pin pulled down until the port voltage falls below V_{HSOFF} or the AUX pin is above V_{AUXT}.

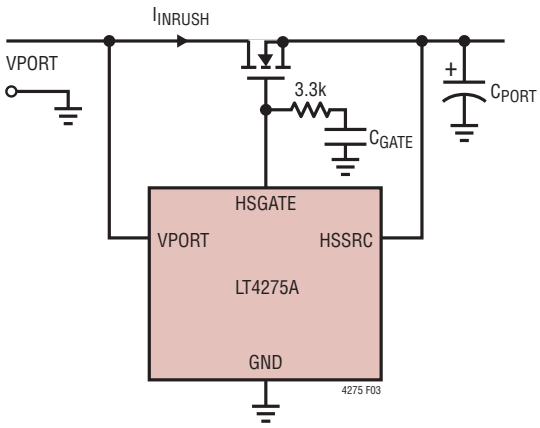


Figure 3. Programming I_{INRUSH}

AUXILIARY SUPPLY OVERRIDE

If the AUX pin is held above V_{AUXT}, the LT4275 enters auxiliary power supply override mode. In this mode the signature resistor is disconnected, classification is disabled, HSGATE is pulled down, and the PWRGD pin is allowed to float. The $\overline{T2P}$ pin pulls down on the LT4275A/LT4275B when no R_{CLS}++ resistor is present. The $\overline{T2P}$ pin alternates between pulling down and floating at f_{T2P} on the LT4275A when the R_{CLS}++ resistor is present.

APPLICATIONS INFORMATION

The AUX pin allows for setting the auxiliary supply turn on (V_{AUXON}) and turn off (V_{AUXOFF}) voltage thresholds. The auxiliary supply hysteresis voltage (V_{AUXHYS}) is set by sinking current (I_{AUXH}) only when the AUX pin voltage is less than V_{AUXT}. Use the following equations to set V_{AUXON} and V_{AUXOFF} via R1 and R2 in Figure 4.

$$R1 = \frac{V_{AUXON} - V_{AUXOFF}}{I_{AUXH}} = \frac{V_{AUXHYS}}{I_{AUXH}}$$

$$R2 = \frac{R1}{\left(\frac{V_{AUXOFF}}{V_{AUXT}} - 1\right)}$$

$$R1 \geq \frac{V_{AUX(MAX)} - V_{AUXT}}{1.4mA}$$

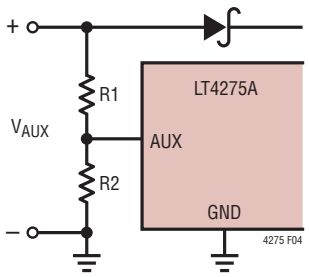


Figure 4. AUX Threshold and Hysteresis Calculation

THERMAL PROTECTION

The IEEE 802.3 specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. During classification, however, the power dissipation in the LT4275 may be as high as 1.5W. The LT4275 can easily tolerate this power for the maximum IEEE timing but will overheat if this condition persists abnormally.

The LT4275 includes a thermal protection feature which protects itself from excessive heating. If the junction temperature exceeds the overtemperature threshold, the LT4275 pulls down the HSGATE and PWRGD pins and disables classification.

EXTERNAL INTERFACE AND COMPONENT SELECTION

Input Diode Bridge

The input diode bridge introduces a voltage drop that affects the voltage range for each mode of operation. The LT4275 is designed to tolerate these voltage drops. The voltages shown in the Electrical Specifications are measured at the LT4275 package pins.

Input Capacitor

A 0.1µF capacitor is needed from VPORT to GND to meet an input impedance requirement in IEEE 802.3.

Transient Voltage Suppressor

The LT4275 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world can routinely see excessive peak voltages. To protect the LT4275, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ58A between the port voltage and GND. This TVS must be mounted near the LT4275.

For extremely high cable discharge and surge protection contact Linear Technology Applications.

Classification Resistor (R_{CLS} and R_{CLS}++)

The R_{CLS} resistors set the classification load current corresponding to the PD power classification. Select the value of R_{CLS} from Table 1 and connect the resistor between the RCLASS pin and GND, or float the RCLASS pin if class 0 is required. The resistor tolerance must be 1% or better to avoid degrading the overall accuracy of the classification circuit. For LTPoE++ use the LT4275A and select the value of R_{CLS}++ from Table 1 in addition to R_{CLS}.

Power Good Interface

The LT4275 provides a power good signal (PWRGD) to simplify the isolated power supply design. The power good signal is used to delay isolated power supply startup until the C_{PORT} capacitor is fully charged.

Exposed Pad

The LT4275A/LT4275B/LT4275C DFN package has an exposed pad that is internally electrically connected to GND. The exposed pad may only be connected to GND on the printed circuit board.

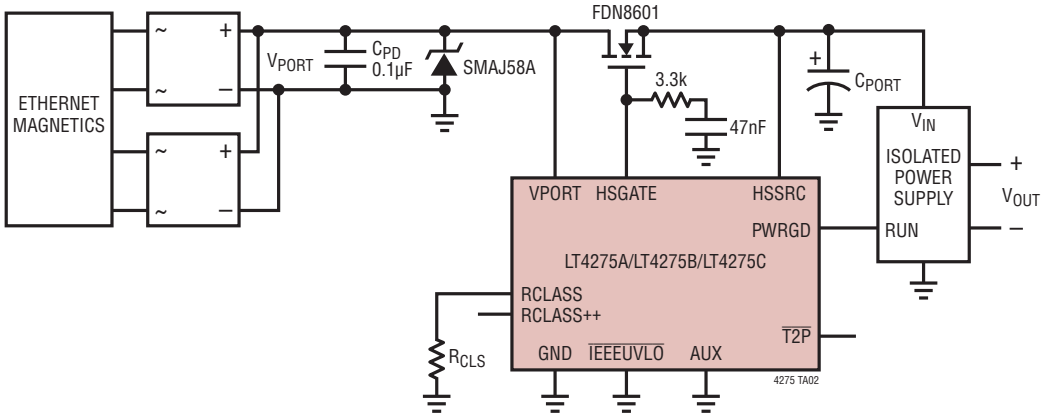
LAYOUT CONSIDERATIONS

Avoid excessive parasitic capacitance on the RCLASS pin and place resistor R_{CLS} close to the LT4275. For the LT4275A, place R_{CLS}++ nearby as well.

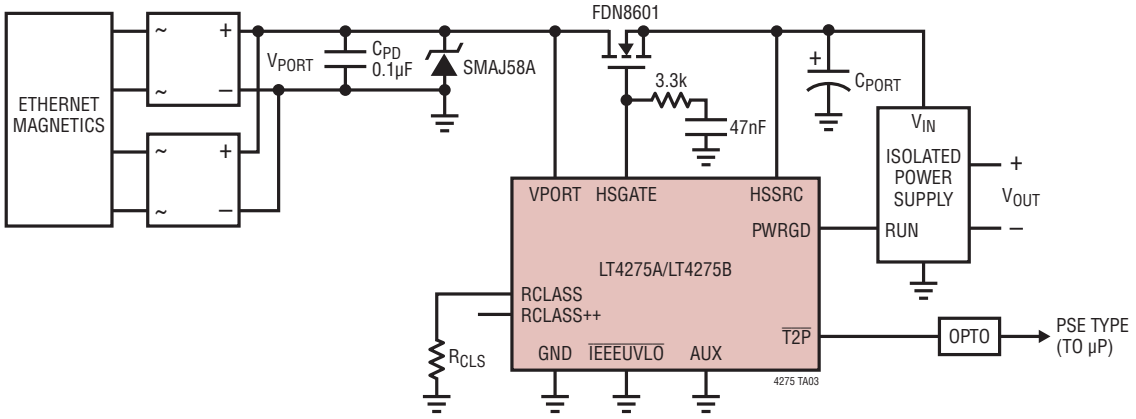
It is strictly required for maximum protection to place the input capacitor (C_{PD}) and transient voltage suppressor as close to the LT4275 as possible.

TYPICAL APPLICATIONS

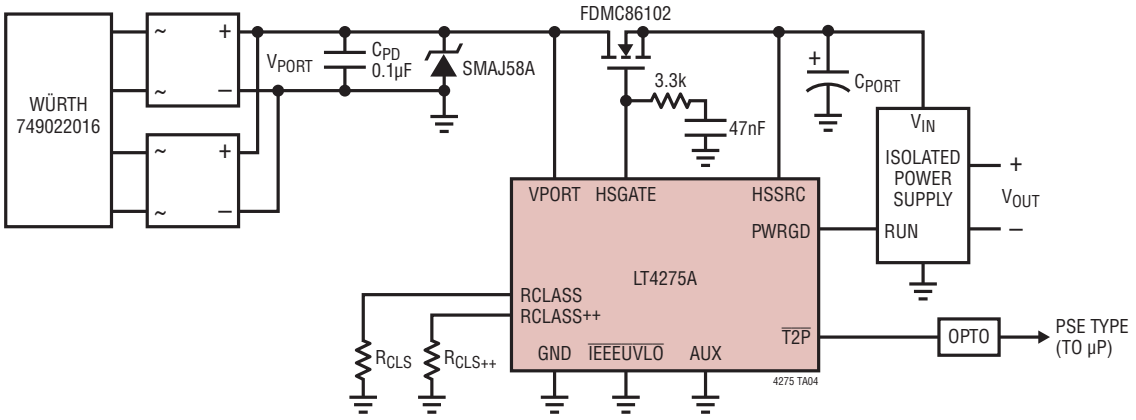
IEEE 802.3af (Type 1) 13W Powered Device



IEEE 802.3at (Type 2) 25.5W Powered Device



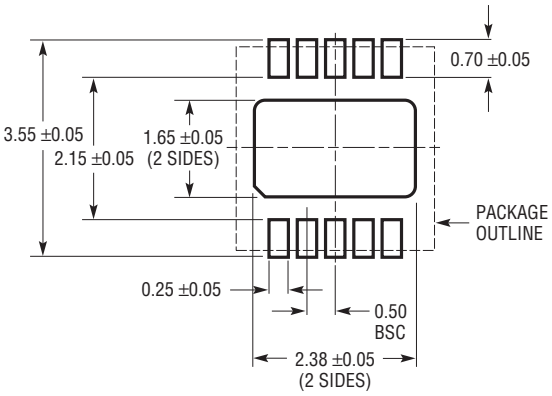
LTPoE++ 38.7W to 90W Powered Device



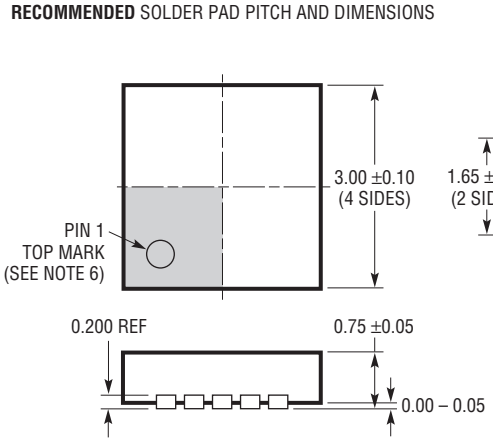
PACKAGE DESCRIPTION

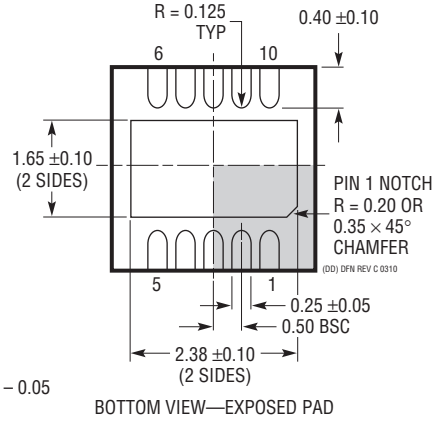
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





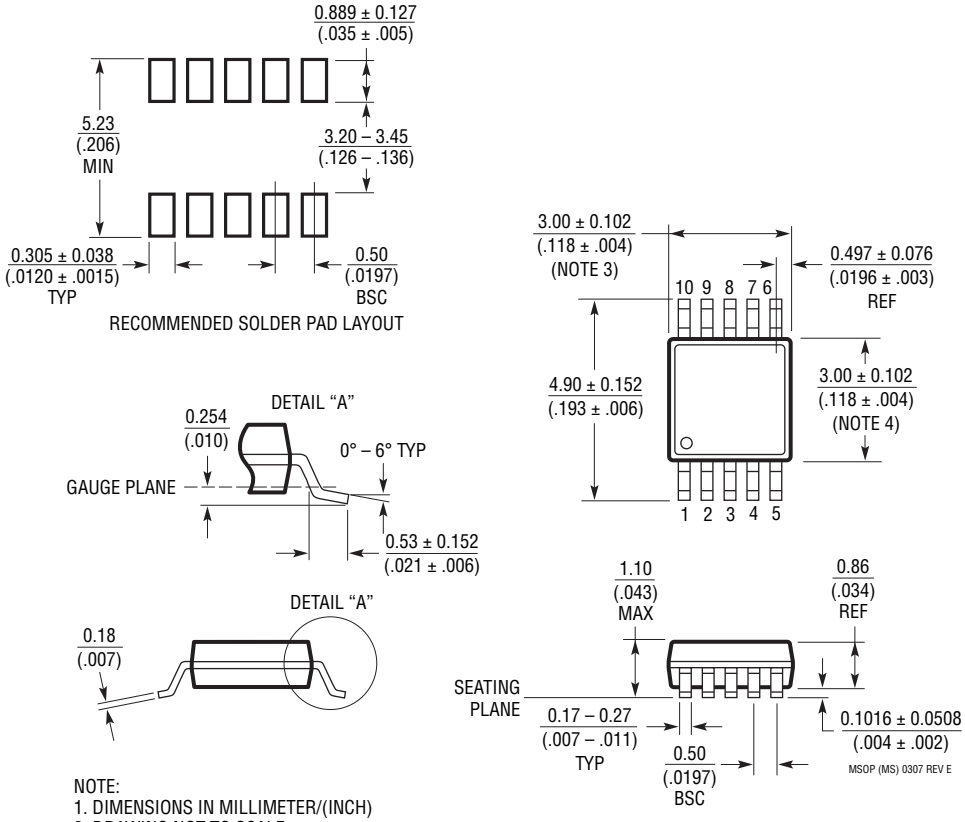
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

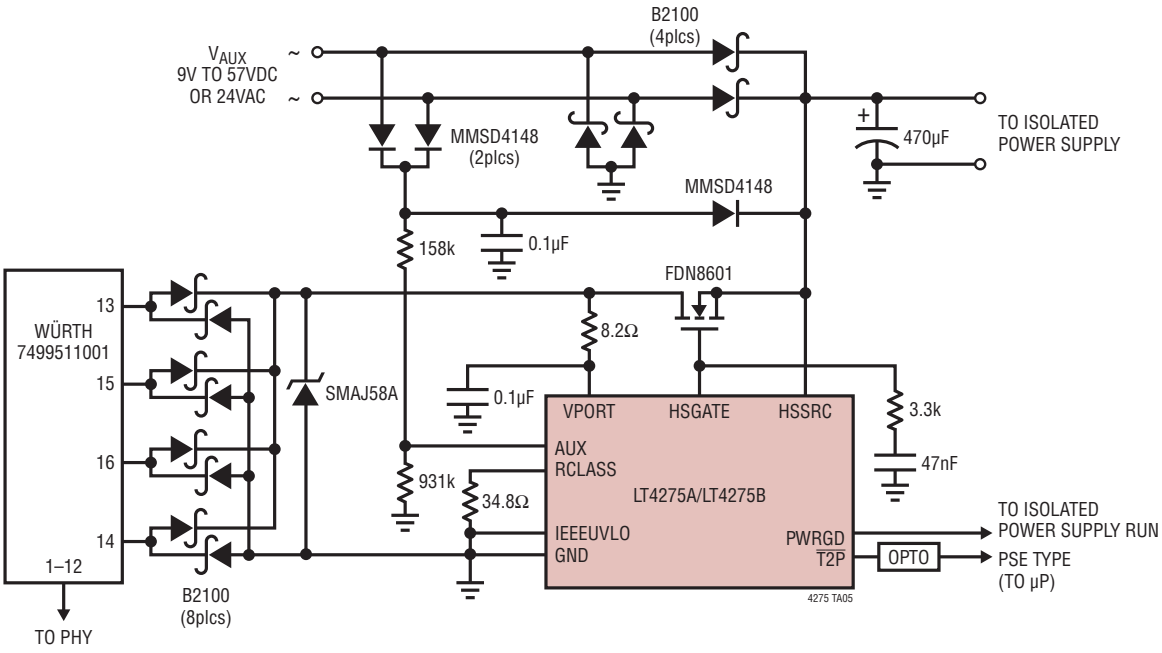
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

25W PD Solution with 12VDC and 24VAC Auxiliary Input



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4257-1	IEEE 802.3af PD Interface Controller	Internal 100V, 400mA Switch, Dual Current Limit, Programmable Class
LTC4263	Single IEEE 802.3af PSE Controller	Internal FET Switch
LTC4265	IEEE 802.3at PD Interface Controller	Internal 100V, 1A Switch, 2-Event Classification Recognition
LTC4266	Quad IEEE 802.3at PoE PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification
LTC4266A	Quad LTPoE++ PSE Controller	Provides Up to 90W. Backwards Compatible with IEEE 802.3af and IEEE 802.3at PDs. With Programmable I_{CUT}/I_{LIM}, 2-Event Classification
LTC4266C	Quad IEEE 802.3af PSE Controller	With Programmable I_{CUT}/I_{LIM}, 1-Event Classification
LTC4267-3	IEEE 802.3af PD Interface with Integrated Switching Regulator	Internal 100V, 400mA Switch, Programmable Class, 300kHz Constant Frequency PWM
LTC4269-1	IEEE 802.3af PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, Aux Support
LTC4269-2	IEEE 802.3af PD Interface with Integrated Forward Switching Regulator	2-Event Classification, Programmable Class, Synchronous Forward Controller, 100kHz to 500kHz, Aux Support
LTC4270/LTC4271	12-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs
LTC4274	Single IEEE 802.3at PoE PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification
LTC4274A	Single LTPoE++ PSE Controller	Provides Up to 90W. Backwards Compatible with IEEE 802.3 PDs. With Programmable I_{CUT}/I_{LIM}, 2-Event Classification
LTC4274C	Single IEEE 802.3af PSE Controller	With Programmable I_{CUT}/I_{LIM}, 1-Event Classification
LTC4278	IEEE 802.3af PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4290/LTC4271	8-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs

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