Absolute Maximum Ratings

Voltage Range on Any Pin (with respect to GND) .....-1V to +7V
Operating Temperature Range
C Suffix .....0°C to +70°C
E Suffix ..... -40°C to +85°C
M Suffix..... -55°C to +125°C

Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
$\overline{ST}$ and $\overline{PBRST}$ Input High Level (Note 1)	V_{IH}		2.0		V_{CC} + 0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{IL}		-0.3		+0.8	V

DC Electrical Characteristics

(V_{CC} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage $\overline{ST}$, TOL	I_{IL}		-1.0		+1.0	µA
Output Current RST	I_{OH}	V_{OH} = 2.4V	-1.0	-12		mA
Output Current RST, $\overline{RST}$	I_{OL}	V_{OL} = 0.4V	2.0	10		mA
Operating Current (Note 2)	I_{CC}			50	200	µA
V_{CC} 5% Trip Point (Note 3)	V_{CCTP}	TOL = GND	4.50	4.62	4.74	V
V_{CC} 10% Trip Point (Note 3)	V_{CCTP}	TOL = V_{CC}	4.25	4.37	4.49	V

Capacitance (Note 4)

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance $\overline{ST}$, TOL	C_{IN}				5	pF
Output Capacitance RST, $\overline{RST}$	C_{OUT}				7	pF

AC Electrical Characteristics

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{PBRST}$ (Note 5)	t_{PB}	Figure 3	20			ms
$\overline{PBRST}$ Delay	t_{PBD}	Figure 3	1	4	20	ms
Reset Active Time	t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	Figure 4	75			ns
$\overline{ST}$ Timeout Period	t_{TD}	Figure 4, TD pin = 0V	62.5	150	250	ms
		TD pin = open	250	600	1000	
		TD pin = V_{CC}	500	1200	2000	
V_{CC} Fall Time (Note 4)	t_F	Figure 5	10			µs
V_{CC} Rise Time (Note 4)	t_B	Figure 6	0			µs
V_{CC} Detect to RST High and $\overline{RST}$ Low	t_{BPD}	Figure 7, V_{CC} falling			100	ns
V_{CC} Detect to RST Low and $\overline{RST}$ Open (Note 6)	t_{BPU}	Figure 8, V_{CC} rising	250	610	1000	ms

Note 1: $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of typically 40kΩ.
Note 2: Measured with outputs open.
Note 3: All voltages referenced to GND.
Note 4: Guaranteed by design.
Note 5: $\overline{PBRST}$ must be held low for a minimum of 20ms to guarantee a reset.
Note 6: t_R = 5µs.

Pin Description

PIN		NAME	FUNCTION
WIDE SO	DIP/SO		
1, 3, 5, 7, 10, 12, 14, 16	—	N.C.	No Connection
2	1	$\overline{PBRST}$	Pushbutton Reset Input. A debounced active-low input that ignores pulses less than 1ms in duration and is guaranteed to recognize inputs of 20ms or greater.
4	2	TD	Time Delay Set. The watchdog timebase select input (t_{TD} = 150ms for TD = 0V, t_{TD} = 600ms for TD = open, t_{TD} = 1.2s for TD = V_{CC}).
6	3	TOL	Tolerance Input. Connect to GND for 5% tolerance or to V_{CC} for 10% tolerance.
8	4	GND	Ground
9	5	RST	Reset Output (Active High). Goes active: (1) If V_{CC} falls below the selected reset voltage threshold. (2) If $\overline{PBRST}$ is forced low. (3) If $\overline{ST}$ is not strobed within the minimum timeout period. (4) During power-up.
11	6	$\overline{RST}$	Reset Output (Active Low, Open Drain). See RST.
13	7	$\overline{ST}$	Strobe Input. Input for watchdog timer.
15	8	V_{CC}	+5V Power-Supply Input

Detailed Description

Power Monitor

A voltage detector monitors V_{CC} and holds the reset outputs (RST and $\overline{RST}$) in their active states whenever V_{CC} is below the selected 5% or 10% tolerance (4.62V or 4.37V, typically). To select the 5% level, connect TOL to ground. To select the 10% level, connect TOL to V_{CC}. The reset outputs will remain in their active states until V_{CC} has been continuously in-tolerance for a minimum of 250ms (the reset active time) to allow the power supply and µP to stabilize.

The RST output both sinks and sources current, while the $\overline{RST}$ output, an open-drain MOSFET, sinks current only and must be pulled high.

Pushbutton Reset Input

The MAX1232's debounced manual reset input ($\overline{PBRST}$) manually forces the reset outputs into their active states. The reset outputs go active after $\overline{PBRST}$ has been held low for a time t_{PBD}, the pushbutton reset delay time. The reset outputs remain in their active states for a minimum of 250ms after $\overline{PBRST}$ rises above V_{IH} (Figure 3).

A mechanical pushbutton or an active logic signal can drive the $\overline{PBRST}$ input. The debounced input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or greater. The $\overline{PBRST}$ input has an internal pullup to V_{CC} of about 100µA; therefore, an external pullup resistor is not necessary.

Watchdog Timer

The microprocessor drives the $\overline{ST}$ input with an input/output (I/O) line. The microprocessor must toggle the $\overline{ST}$ input within a set period (as determined by TD) to verify proper software execution. If a hardware or software failure keeps $\overline{ST}$ from toggling within the minimum timeout period—$\overline{ST}$ is activated only by falling edges (a high-to-low transition)—the MAX1232 reset outputs are forced to their active states for 250ms (Figure 2). This typically initiates the microprocessor's power-up routine. If the interruption continues, new reset pulses are generated each timeout period until $\overline{ST}$ is strobed. The timeout period is determined by the TD input connection. This timeout period is typically 150ms with TD connected to GND, 600ms with TD floating, or 1200ms with TD connected to V_{CC}.

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that executes frequently enough so the time between toggles is less than the watchdog timeout period. One common technique controls the microprocessor I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode, and set it low while in the background or interrupt mode. If both modes do not execute correctly, the watchdog timer issues reset pulses.

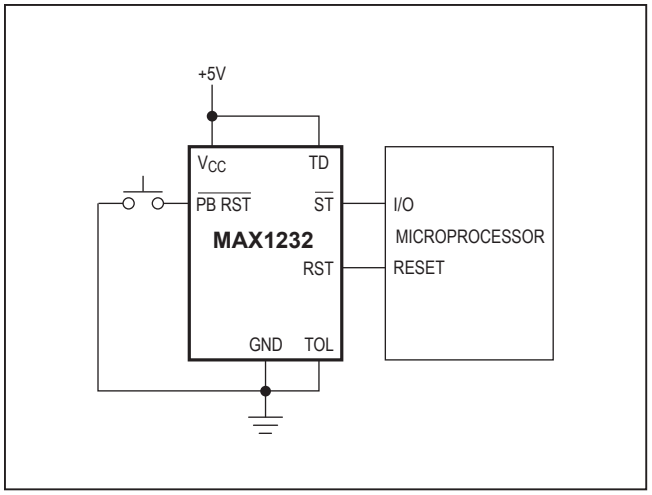


Figure 1. Pushbutton Reset

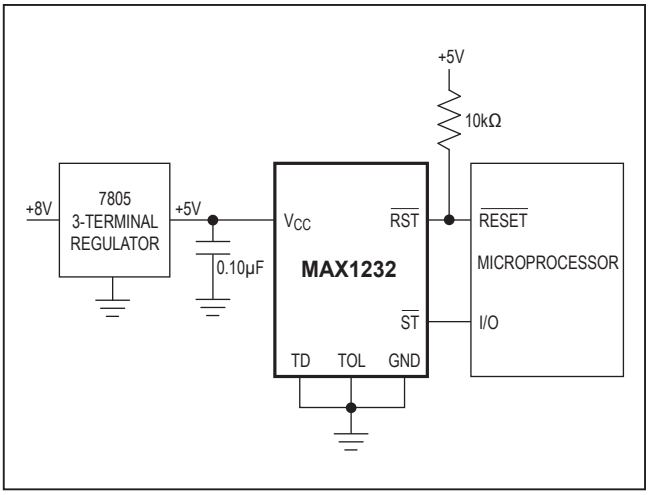


Figure 2. Watchdog Timer

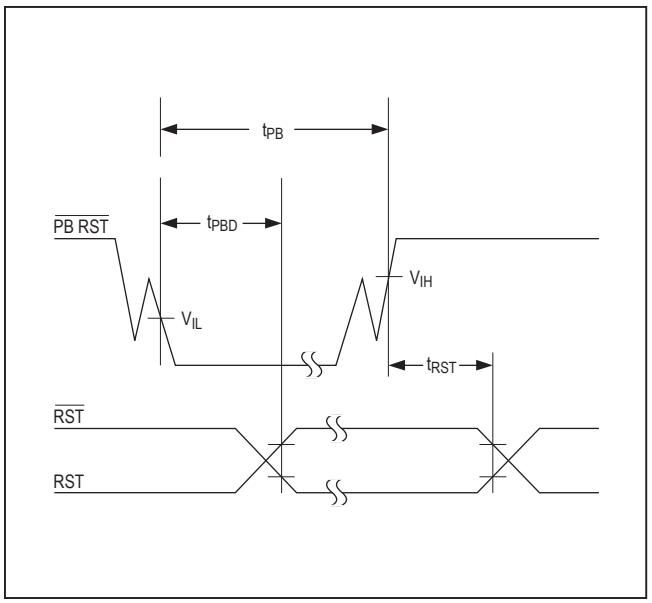
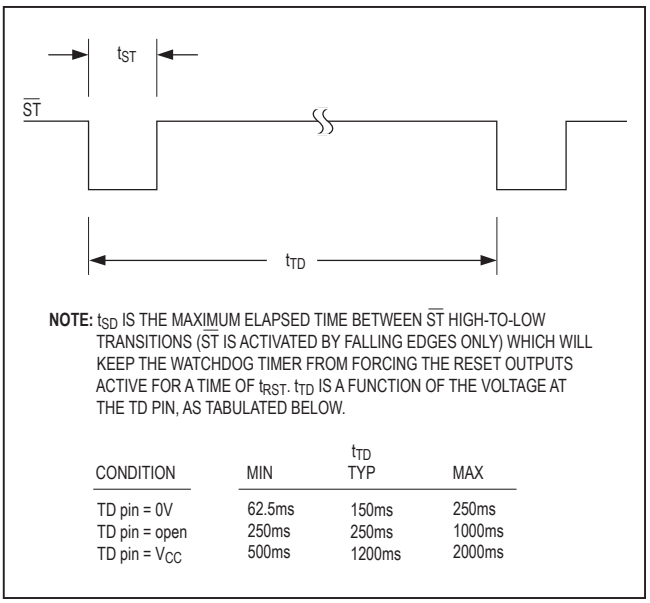


Figure 3. Pushbutton Reset. The debounced PBRST input ignores input pulses less than 1ms and is guaranteed to recognize pulses of 20ms or greater.



NOTE: t_{SD} IS THE MAXIMUM ELAPSED TIME BETWEEN $\overline{ST}$ HIGH-TO-LOW TRANSITIONS ($\overline{ST}$ IS ACTIVATED BY FALLING EDGES ONLY) WHICH WILL KEEP THE WATCHDOG TIMER FROM FORCING THE RESET OUTPUTS ACTIVE FOR A TIME OF t_{RST}. t_{TD} IS A FUNCTION OF THE VOLTAGE AT THE TD PIN, AS TABULATED BELOW.

		t_{TD}	
CONDITION	MIN	TYP	MAX
TD pin = 0V	62.5ms	150ms	250ms
TD pin = open	250ms	250ms	1000ms
TD pin = V_{CC}	500ms	1200ms	2000ms

Figure 4. Watchdog Strobe Input

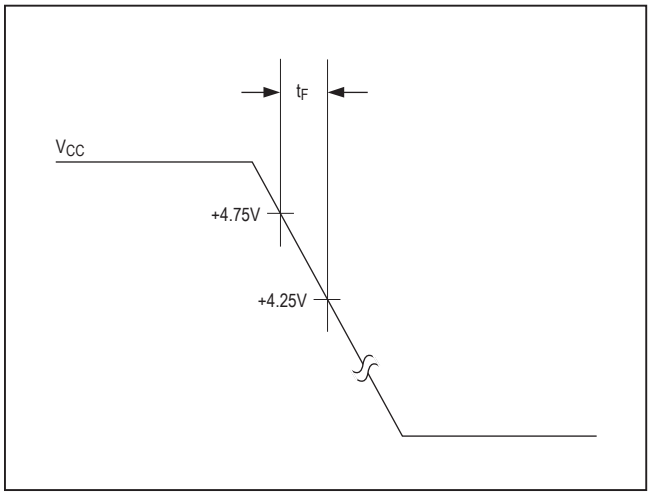


Figure 5. Power-Down Slew Rate

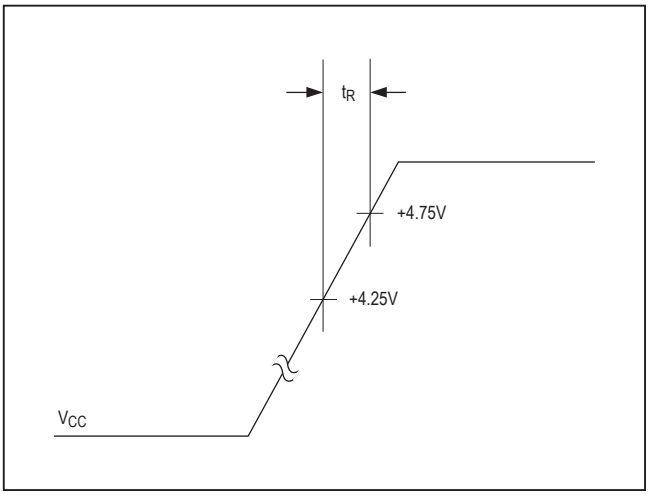


Figure 6. Power-Up Slew Rate

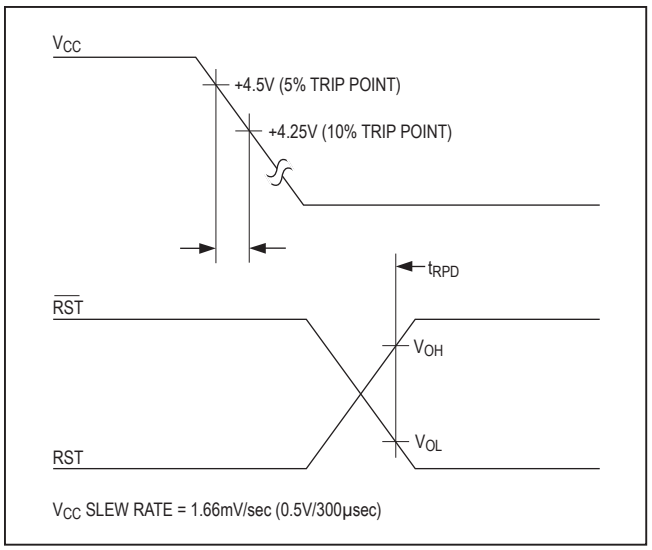


Figure 7. VCC Detect Reset Output Delay (Power-Down)

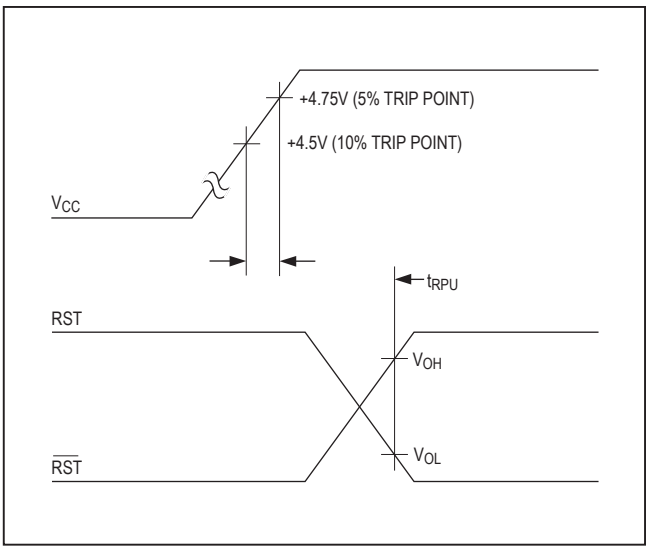
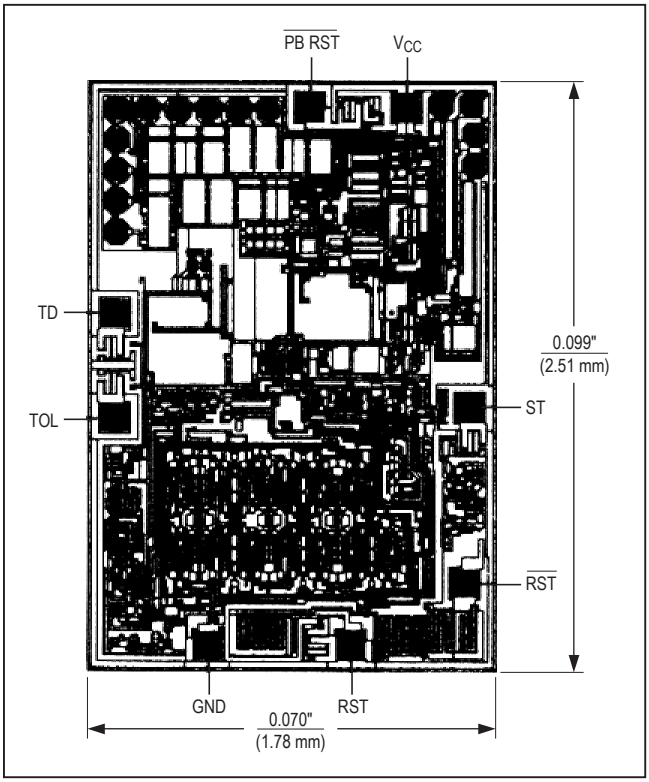


Figure 8. VCC Detect Reset Output Delay (Power-Up)

Chip Topography



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1232CWE	0°C to +70°C	16 Wide SO
MAX1232EPA	-40°C to +85°C	8 PDIP
MAX1232ESA	-40°C to +85°C	8 SO
MAX1232EWE	-40°C to +85°C	16 Wide SO
MAX1232MJA	-55°C to +125°C	8 CERDIP

**Contact factory for dice specifications.*

Note: *Devices in PDIP and SO packages are available in both leaded(Pb) and lead(Pb)-free packaging. Specify lead(Pb)-free by adding the "+" symbol at the end of the part number when ordering. Lead-free not available for CERDIP package.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 CERDIP	J8-2	21-0045	—
8 PDIP	P8+2	21-0043	—
8 SO	S8+4	21-0041	90-0096
16 Wide SO	W16+1	21-0042	90-0107

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	11/05	Added lead-free information to the *Ordering Information* table	1, 6
2	9/14	Removed reference to automotive systems in the *Applications*	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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