System-Level Cost Saving

The P1022 processor's highly integrated architecture is designed to enhance performance and deliver system-level cost savings in a small board footprint. Key system-level peripherals include dual Gigabit Ethernet, dual USB 2.0, dual SATA, SD/MMC and triple PCI Express interconnects. Furthermore, the P1022 integrates LCD controller, I²S audio and VoIP TDM interfaces for use in creating engaging human interfaces. Special care was taken to design the P1022 processor's pin locations for mounting on low-cost six layer PCBs. The P1022 is a full-featured, high-performance gigahertz processor that is designed to support fanless operation for power-sensitive applications.

Advanced Energy-Efficient Modes

Balancing the performance requirements for powerful new networking- and Internet-centric applications, with the increasing concerns over energy consumption, is driving manufacturers to develop intelligent strategies for optimizing performance within specific energy budgets. This is a key challenge for the next-generation green embedded systems. The P1022 processor implements sophisticated power-saving modes for managing energy consumption in both dynamic and static power modes. These include the traditional nap, doze plus the jog (dynamic frequency scaling) and packet-lossless deep-sleep modes. Designers may leverage these modes to efficiently match work accomplished with the correct level of energy consumed.

The combination of these features makes the P1022 processor an optimal embedded processing solution for Ethernet or PCI Express interworking applications, such as enterprise networking, industrial, storage, security and office automation applications. Examples include control plane processing, protocol processing, media processing while producing an engaging human machine interface.

Key Features

- Dual (P1022) or single (P1013) high-performance e500v2 cores built on Power Architecture technology
  - 36-bit physical addressing
  - Double precision floating point support
  - Signal processing engine (SPE) APU (auxiliary processing unit)
  - 32 KB L1 instruction cache and 32 KB L1 data cache for each core
  - 600 MHz to 1055 MHz core clock frequency
- 256 KB L2 cache with ECC, also configurable as SRAM and stashing memory
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Two 10/100/1000 Mbps virtualized enhanced three-speed Ethernet controllers (eTSECs)
  - TCP/IP acceleration and classification capabilities
  - IEEE® 1588 support
  - Loseless flow control
  - RMII, RGMII, SGMII
- Integrated security engine (optional)
  - Crypto algorithm support includes 3DES, AES, RSA/ECC, MD5/SHA, ARC4, Kasumi, Snow 3G and FIPS deterministic RNG
  - Single pass encryption/message authentication for common security protocols (IPsec, SSL, SRTP, WiMAX)
  - XOR acceleration
- High-speed interfaces (not all available simultaneously)
  - Six SerDes lanes (multiplexed across controllers)
  - One x4 and two x1 PCI Express interfaces
  - Two serial ATA (SATA) interfaces
  - Two SGMII interfaces
- Audio visual interfaces
  - LCD interface supporting a display of 1280 x 1024P @ 60 Hz, 24 bits per pixel
  - I²S interface with maximum sampling frequency of 192 kHz
- VoIP TDM interface
  - Support for up to 128 channels
- Two High-Speed USB controllers (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface to PHY
- Enhanced secure digital host controller (SD/MMC)
- Serial peripheral interface
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Dual four-channel DMA controllers
- Dual I²C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- Advanced power and energy management
  - Low power operation
  - Support for dynamic and static power management
  - Doze, nap and sleep modes for dynamic power management
  - Packet-lossless deep sleep: power removed from major portion of the chip
  - PMC wake on: filtered LAN activity, USB connection, GPIO, internal timer or external interrupt event
- Up to 87 general-purpose signals
- Available in extended temperature (optional)
- 689-pin TEPBGA package

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Document Number: QP1022FS / REV 1

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