Absolute Maximum Ratings

CELL to GND .....-0.3V to +12V
All Other Pins to GND .....-0.3V to +6V
Continuous Sink Current, SDA, $\overline{ALRT}$ 20mA
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (TDFN only) (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = 2.5V to 4.5V, T_A= -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	(Note 2)	2.5		4.5	V
Fuel-Gauge SOC Reset (VRESET Register)	V_{RST}	Configuration range, in 40mV steps	2.28		3.48	V
		Trimmed at 3V	2.85	3.0	3.15	V
Data I/O Pins	SCL, SDA, $\overline{ALRT}$	(Note 2)	-0.3		+5.5	V
Supply Current	I_{DD0}	Sleep mode, $T_A \le +50°C$		0.5	2	µA
		Hibernate mode, reset comparator disabled (VRESET.Dis = 1)		3	5	
		Hibernate mode, reset comparator enabled (VRESET.Dis = 0)		4		
	I_{DD1}	Active mode		23	40	
Time Base Accuracy	t_{ERR}	Active, hibernate modes (Note 3)	-3.5	±1	+3.5	%
ADC Sample Period		Active mode		250		ms
		Hibernate mode		45		s
Voltage Error	V_{ERR}	V_{CELL} = 3.6V, T_A = +25°C (Note 4)	-7.5		+7.5	mV/cell
			-20		+20	
Voltage-Measurement Resolution				1.25		mV/cell
Voltage-Measurement Range		MAX17048: V_{DD} pin	2.5		5	V
		MAX17049: CELL pin	5		10	
SDA, SCL, QSTRT Input Logic-High	V_{IH}		1.4			V
SDA, SCL, QSTRT Input Logic-Low	V_{IL}				0.5	V
SDA, $\overline{ALRT}$ Output Logic-Low	V_{OL}	I_{OL} = 4mA			0.4	V
SDA, SCL Bus Low-Detection Current	I_{PD}	$V_{SDA} = V_{SCL}$ = 0.4V (Note 5)		0.2	0.4	µA
Bus Low-Detection Timeout	t_{SLEEP}	(Note 6)	1.75		2.5	s

Electrical Characteristics (I²C INTERFACE)

(2.5V < V_{DD} < 4.5V, T_A = -20°C to +70°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 7)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold Time	$t_{HD:STA}$	(Note 8)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 9, 10)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 9)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F		20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 11)	0		50	ns
Capacitive Load for Each Bus Line	C_B	(Note 12)			400	pF
SCL, SDA Input Capacitance	$C_{B,IN}$				60	pF

Note 1: Specifications are 100% tested at T_A = +25°C. Limits over the operating range are guaranteed by design and characterization.
Note 2: All voltages are referenced to GND.
Note 3: Test is performed on unmounted/unsoldered parts.
Note 4: The voltage is trimmed and verified with 16x averaging.
Note 5: This current is always present.
Note 6: The IC enters shutdown mode after SCL < V_{IL} and SDA < V_{IL} for longer than 2.5s.
Note 7: Timing must be fast enough to prevent the IC from entering sleep mode due to bus low for period > t_{SLEEP}.
Note 8: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 9: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 10: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the $V_{IH,MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 11: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instance.
Note 12: C_B is total capacitance of one bus line in pF.

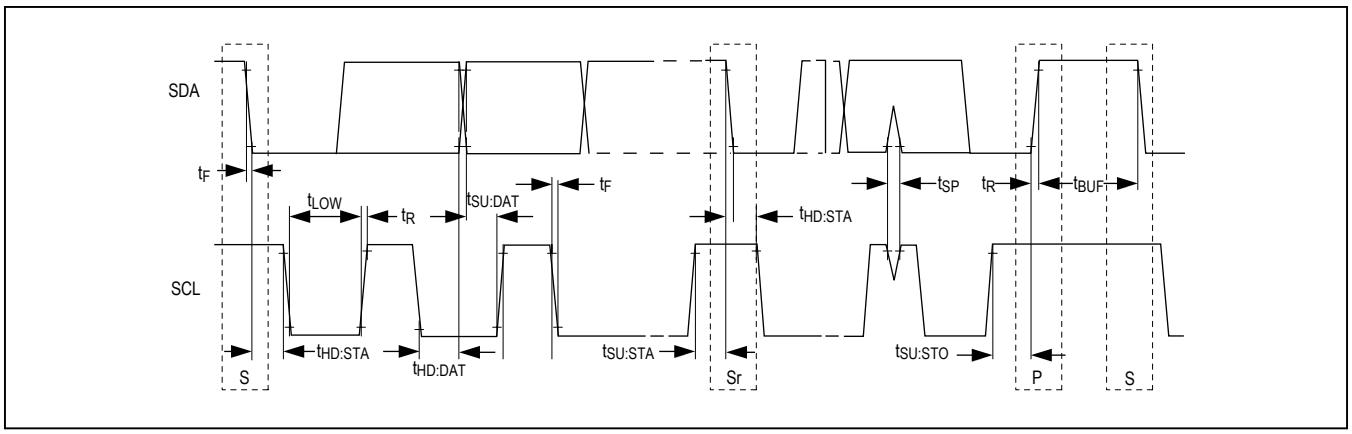
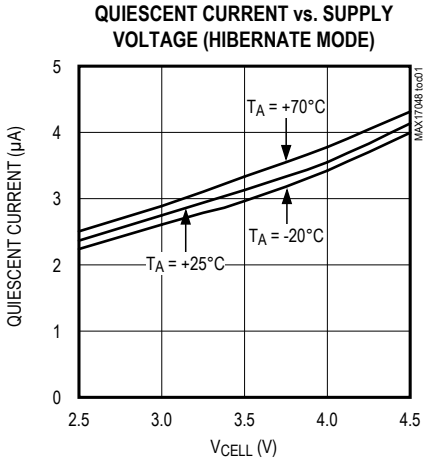
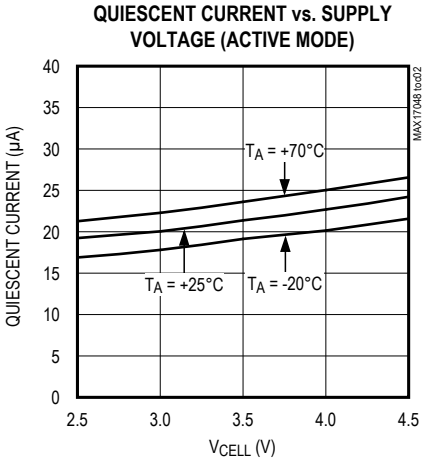


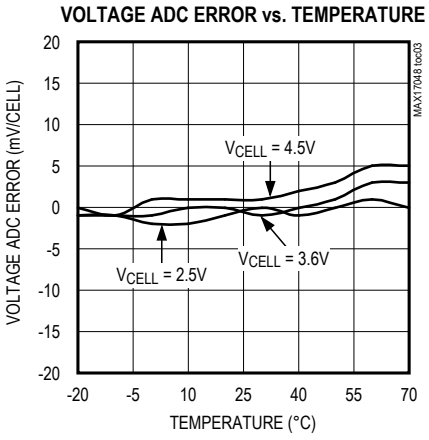
Figure 1. I²C Bus Timing Diagram

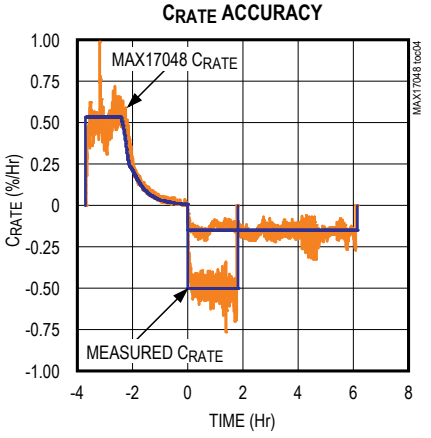
Typical Operating Characteristics

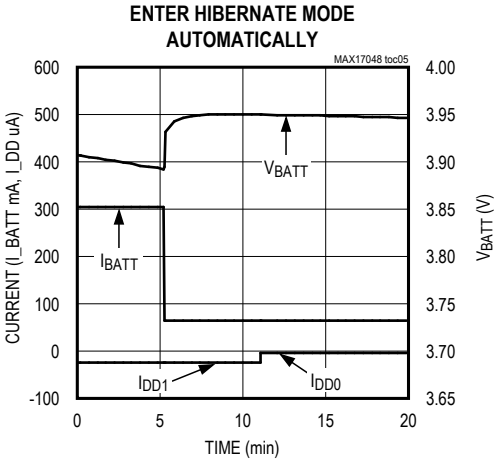
(T_A = +25°C, battery is Sanyo UF504553F, unless otherwise noted.)







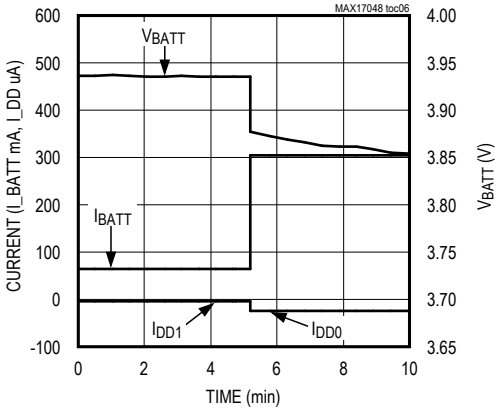




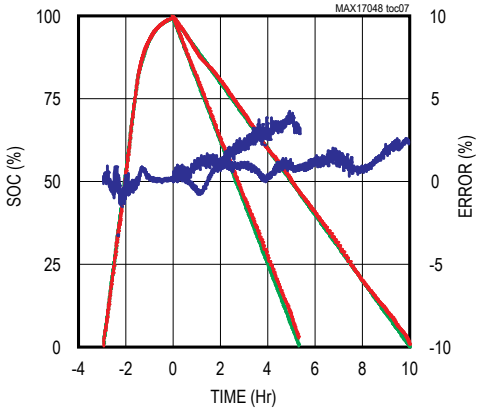
Typical Operating Characteristics (continued)

(T_A = +25°C, battery is Sanyo UF504553F, unless otherwise noted.)

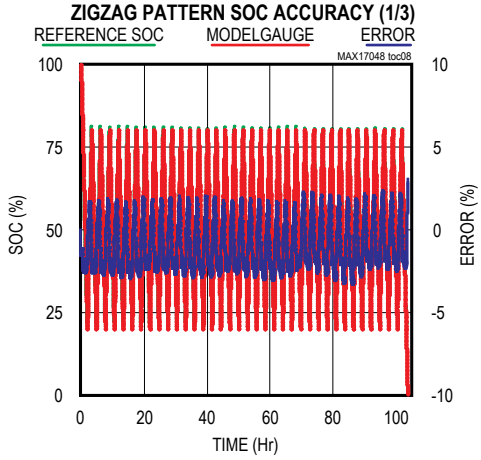
EXIT HIBERNATE MODE AUTOMATICALLY



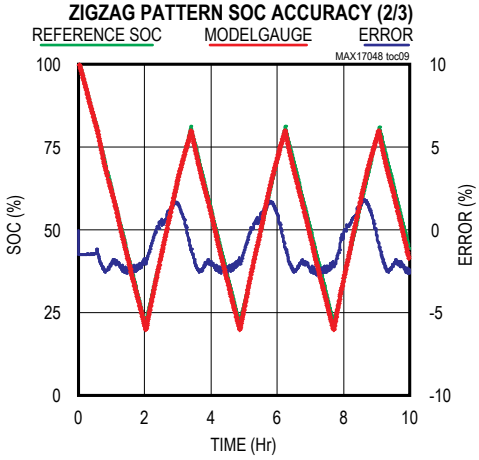
SOC ACCURACY T_A = 20°C, HIBERNATE MODE



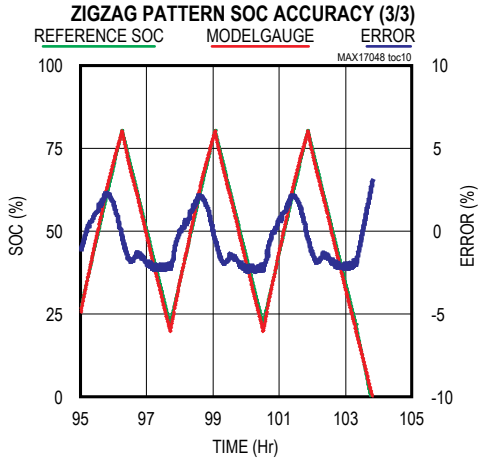
ZIGZAG PATTERN SOC ACCURACY (1/3)



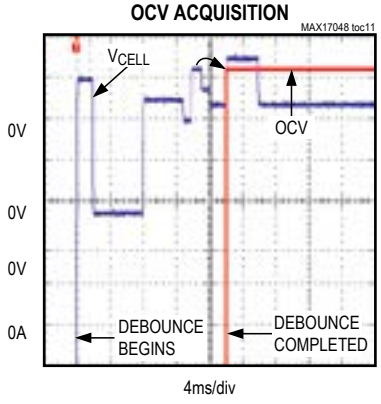
ZIGZAG PATTERN SOC ACCURACY (2/3)



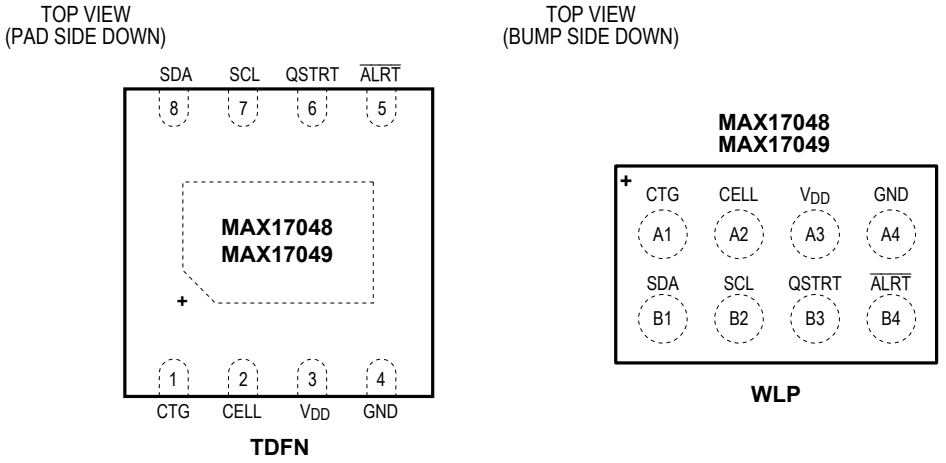
ZIGZAG PATTERN SOC ACCURACY (3/3)



BATTERY-INSERTION DEBOUNCE/ OCV ACQUISITION



Pin/Bump Configurations



Pin/Bump Descriptions

PIN/BUMP		NAME	FUNCTION
TDFN	WLP		
1	A1	CTG	Connect to Ground
2	A2	CELL	Connect to the Positive Battery Terminal. MAX17048: Not internally connected. MAX17049: Voltage sense input.
3	A3	V_{DD}	Power-Supply Input. Bypass with 0.1µF to GND. MAX17048: Voltage sense input. Connect to positive battery terminal. MAX17049: Connect to regulated power-supply voltage.
4	A4	GND	Ground. Connect to negative battery terminal.
5	B4	$\overline{ALRT}$	Open-Drain, Active-Low Alert Output. Optionally connect to interrupt input of the system microcontroller.
6	B3	QSTRT	Quick-Start Input. Allows reset of the device through hardware. Connect to GND if not used.
7	B2	SCL	I^2C Clock Input. SCL has an internal pulldown (I_{PD}) for sensing disconnection.
8	B1	SDA	Open-Drain I^2C Data Input/Output. SDA has an internal pulldown (I_{PD}) for sensing disconnection.
—	—	EP	Exposed Pad (TDFN Only). Connect to GND.

Detailed Description

ModelGauge Theory of Operation

The MAX17048/MAX17049 ICs simulate the internal, nonlinear dynamics of a Li+ battery to determine its SOC. The sophisticated battery model considers impedance and the slow rate of chemical reactions in the battery (Figure 2).

ModelGauge performs best with a custom model, obtained by characterizing the battery at multiple discharge currents and temperatures to precisely model it. At power-on reset (POR), the ICs have a preloaded ROM model that performs well for some batteries. Contact Maxim if you need a custom model.

Fuel-Gauge Performance

In coulomb counter-based fuel gauges, SOC drifts because offset error in the current-sense ADC measurement accumulates over time. Instantaneous error can be very small, but never precisely zero. Error accumulates over time in such systems (typically 0.5%–2% per day) and requires periodic corrections. Some algorithms correct drift using occasional events, and until such an event occurs the algorithm's error is boundless:

- Reaching predefined SOC levels near full or empty
- Measuring the relaxed battery voltage after a long period of inactivity
- Completing a full charge/discharge cycle

ModelGauge requires no correction events because it uses only voltage, which is stable over time. As TOCs 8, 9, and 10 show, ModelGauge remains accurate despite the absence of any of the above events; it neither drifts nor accumulates error over time.

To correctly measure performance of a fuel gauge as experienced by end-users, exercise the battery dynamically. Accuracy cannot be fully determined from only simple cycles.

Battery Voltage and State-Of-Charge

Open-circuit voltage (OCV) of a Li+ battery uniquely determines its SOC; one SOC can have only one value of OCV. In contrast, a given V_{CELL} can occur at many different values of OCV because V_{CELL} is a function of time, OCV, load, temperature, age, and impedance, etc.; one value of OCV can have many values of V_{CELL}. Therefore, one SOC can have many values of V_{CELL}, so V_{CELL} cannot uniquely determine SOC.

Figure 3 shows that V_{CELL} = 3.81V occurs at 2%, 50%, and 72% SOC.

Even the use of sophisticated tables to consider both voltage and load results in significant error due to the load transients typically experienced in a system. During charging or discharging, and for approximately 30min after, V_{CELL} and OCV differ substantially, and V_{CELL} has been affected by the preceding hours of battery activity. ModelGauge uses voltage comprehensively.

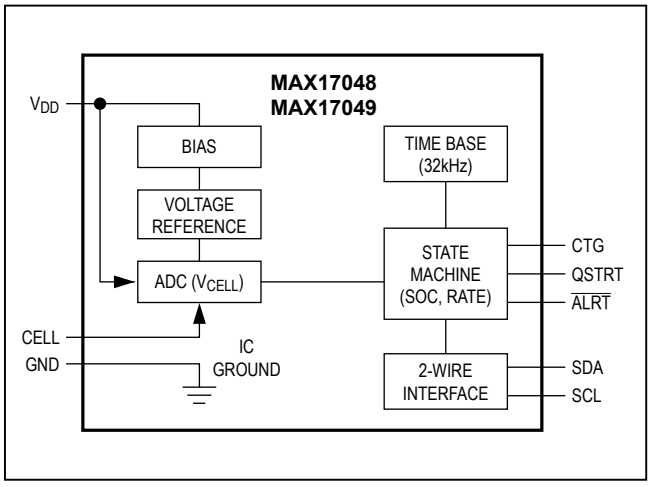


Figure 2. Block Diagram

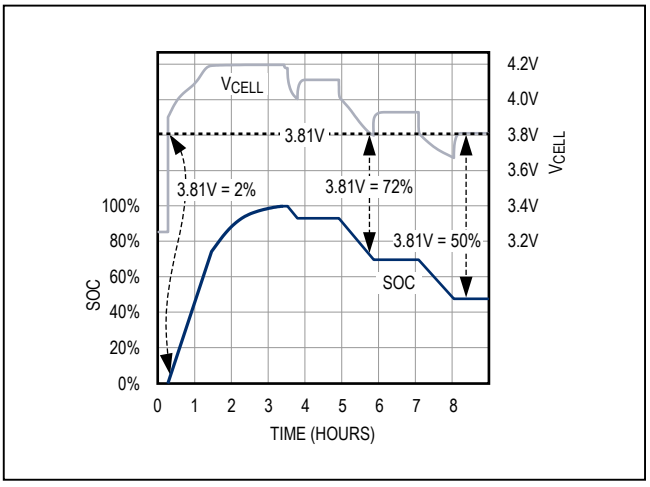


Figure 3. Instantaneous Voltage Does Not Translate Directly to SOC

Temperature Compensation

For best performance, the host microcontroller must measure battery temperature periodically, and compensate the RCOMP ModelGauge parameter accordingly, at least once per minute. Each custom model defines constants RCOMP0 (default is 0x97), TempCoUp (default is -0.5), and TempCoDown (default is -5.0). To calculate the new value of CONFIG.RCOMP:

```
// T is battery temperature (degrees Celsius)
if (T > 20) {
    RCOMP = RCOMP0 + (T - 20) x TempCoUp;
}
else {
    RCOMP = RCOMP0 + (T - 20) x TempCoDown;
}
```

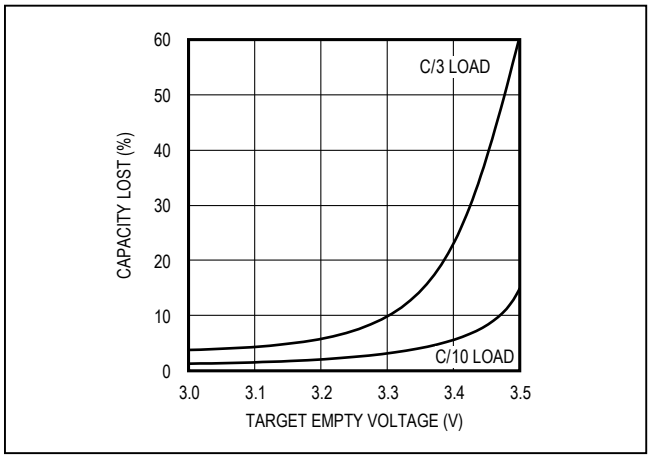


Figure 4. Increasing Empty Voltage Reduces Battery Capacity

Impact of Empty-Voltage Selection

Most applications have a minimum operating voltage below which the system immediately powers off (empty voltage). When characterizing the battery to create a custom model, choose empty voltage carefully. As shown in Figure 4, capacity unavailable to the system increases at an accelerating rate as empty voltage increases.

To ensure a controlled shutdown, consider including operating margin into the fuel gauge based on some low threshold of SOC, for example shutting down at 3% or 5%. This utilizes the battery more effectively than adding error margin to empty voltage.

Battery Insertion

When the battery is first inserted into the system, the fuel-gauge IC has no previous knowledge about the battery's SOC. Assuming that the battery is relaxed, the IC translates its first V_{CELL} measurement into the best initial estimate of SOC. Initial error caused by the battery not being in a relaxed state diminishes over time, regardless of loading following this initial conversion. While SOC estimated by a coulomb counter diverges, ModelGauge SOC converges, correcting error automatically as illustrated in Figure 5; initial error has no long-lasting impact.

Battery Insertion Debounce

Any time the IC powers on or resets (see the *VRESET/ID Register (0x18)* section), it estimates that OCV is the maximum of 16 V_{CELL} samples (1ms each, full 12-bit resolution). OCV is ready 17ms after battery insertion, and SOC is ready 175ms after that.

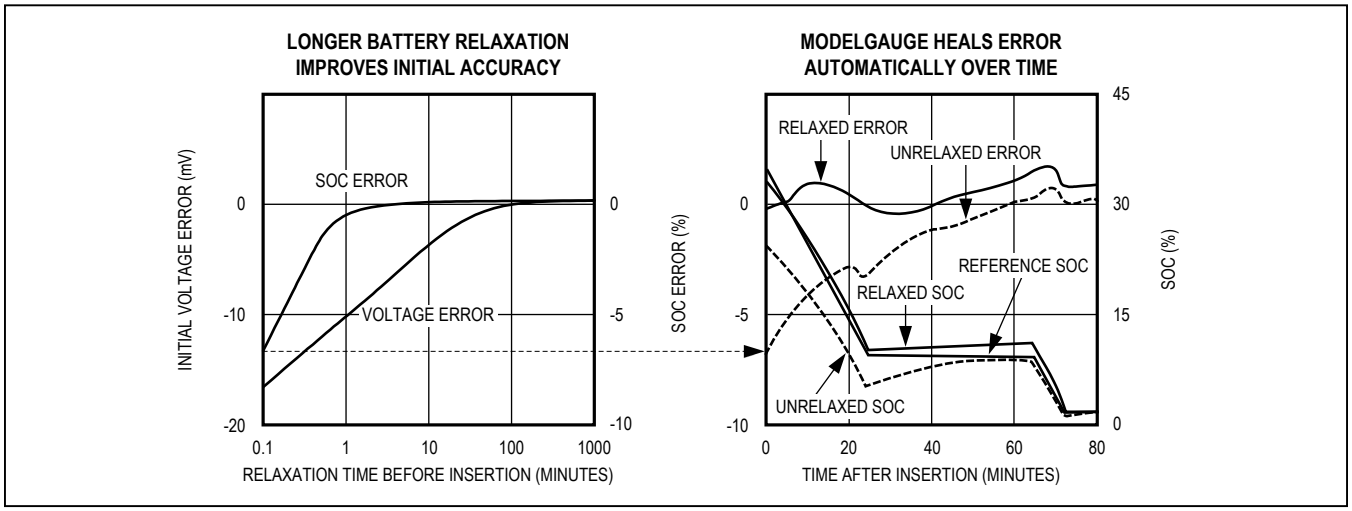


Figure 5. ModelGauge Heals Error Automatically

Battery Swap Detection

If V_{CELL} falls below V_{RST}, the IC quick-starts when V_{CELL} returns above V_{RST}. This handles battery swap; the SOC of the previous battery does not affect that of the new one. See the *Quick-Start* and *VRESET/ID Register (0x18)* sections.

Quick-Start

If the IC generates an erroneous initial SOC, the battery insertion and system powerup voltage waveforms must be examined to determine if a quick-start is necessary, as well as the best time to execute the command. The IC samples the maximum V_{CELL} during the first 17ms. See the *Battery Insertion Debounce* section. Unless V_{CELL} is fully relaxed, even the best sampled voltage can appear greater or less than OCV. Therefore, quick-start must be used cautiously.

Most systems should not use quick-start because the ICs handle most startup problems transparently, such as intermittent battery-terminal connection during insertion. If battery voltage stabilizes faster than 17ms, as illustrated in Figure 6, then do not use quick-start.

The quick-start command restarts fuel-gauge calculations in the same manner as initial power-up of the IC. If the system power-up sequence is so noisy that the initial estimate of SOC has unacceptable error, the system microcontroller might be able to reduce the error by using quick-start. A quick-start is initiated by a rising edge on the QSTRT pin, or by writing 1 to the quick-start bit in the MODE register.

Power-On Reset (POR)

POR includes a quick-start, so only use it when the battery is fully relaxed. See the *Quick-Start* section. This command restores all registers to their default values. After this command, reload the custom model. See the *CMD Register (0xFE)* section.

Hibernate Mode

The ICs have a low-power hibernate mode that can accurately fuel gauge the battery when the charge/discharge rate is low. By default, the device automatically enters and exits the hibernate mode according to the charge/discharge rate, which minimizes quiescent current (below 5µA) without compromising fuel-gauge accuracy. The ICs can be forced into hibernate or active modes. Force the IC into hibernate mode to reduce power consumption in applications with less than C/4-rate maximum loading. For applications with higher loading, Maxim recommends the default configuration of automatic control of hibernate mode.

In hibernate mode, the device reduces its ADC conversion period and SOC update to once per 45s. See the *HIBRT Register (0x0A)* section for details on how the IC automatically enters and exits hibernate mode.

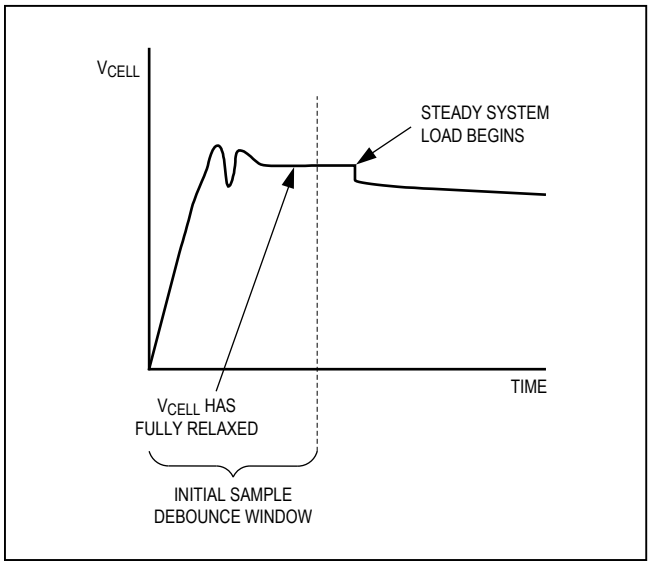


Figure 6. Insertion Waveform Not Requiring Quick-Start Command

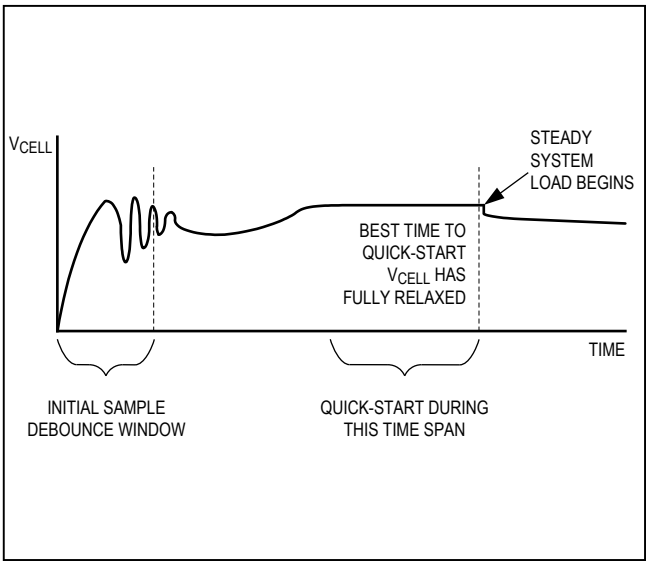


Figure 7. Insertion Waveform Requiring Quick-Start Command

Alert Interrupt

The ICs can interrupt a system microcontroller with five configurable alerts (see Table 1). All alerts can be disabled or enabled with software. When the interrupt occurs, the system microcontroller can determine the cause from the STATUS register.

When an alert is triggered, the IC drives the $\overline{ALRT}$ pin logic-low and sets CONFIG.ALRT = 1. The $\overline{ALRT}$ pin remains logic-low until the system software writes CONFIG.ALRT = 0 to clear the alert. The alert function is enabled by default, so any alert can occur immediately upon power-up. Entering sleep mode clears no alerts.

Sleep Mode

In sleep mode, the IC halts all operations, reducing current consumption to below 1µA. After exiting sleep mode, the IC continues normal operation. In sleep mode, the IC does not detect self-discharge. If the battery changes state while the IC sleeps, the IC cannot detect it, causing SOC error. Wake up the IC before charging or discharging. To enter sleep mode, write MODE.EnSleep = 1 and either:

- Hold SDA and SCL logic-low for a period for t_{SLEEP}. A rising edge on SDA or SCL wakes up the IC.
- Write CONFIG.SLEEP = 1. To wake up the IC, write CONFIG.SLEEP = 0. Other communication does not wake up the IC. POR does wake up the IC.

Applications which can tolerate 4µA should use hibernate rather than sleep mode.

Register Summary

All registers must be written and read as 16-bit words; 8-bit writes cause no effect. Any bits marked X (don't care) or read only must be written with the rest of the register, but the value written is ignored by the IC. The values read from don't care bits are undefined. Calculate the register's value by multiplying the 16-bit word by the register's LSb value, as shown in Table 2.

VCELL Register (0x02)

The MAX17048 measures VCELL between the V_{DD} and GND pins. The MAX17049 measures VCELL between the CELL and GND pins. VCELL is the average of four ADC conversions. The value updates every 250ms in active mode and every 45s in hibernate mode.

SOC Register (0x04)

The ICs calculate SOC using the ModelGauge algorithm. This register automatically adapts to variation in battery size since ModelGauge naturally recognizes relative SOC.

The upper byte least-significant bit has units of 1%. The lower byte provides additional resolution.

The first update is available approximately 1s after POR of the IC. Subsequent updates occur at variable intervals depending on application conditions.

Table 1. Alert Interrupt Summary

ALERT FUNCTION	WHERE CONFIGURED	INDICATOR BIT
Low SOC	CONFIG.ATHD	STATUS.HD
SOC 1% change	CONFIG.ALSC	STATUS.SC
Reset	VRESET, STATUS.RI	STATUS.VR
Overvoltage	VALRT.MAX	STATUS.VH
Undervoltage	VALRT.MIN	STATUS.VL

Table 2. Register Summary

ADDRESS	REGISTER NAME	16-BIT LSb	DESCRIPTION	READ/WRITE	DEFAULT
0x02	VCELL	78.125µV/cell	ADC measurement of VCELL.	R	—
0x04	SOC	1%/256	Battery state of charge.	R	—
0x06	MODE	—	Initiates quick-start, reports hibernate mode, and enables sleep mode.	W	0x0000
0x08	VERSION	—	IC production version.	R	0x001_
0x0A	HIBRT	—	Controls thresholds for entering and exiting hibernate mode.	R/W	0x8030

Table 2. Register Summary (continued)

ADDRESS	REGISTER NAME	16-BIT LSb	DESCRIPTION	READ/WRITE	DEFAULT
0x0C	CONFIG	—	Compensation to optimize performance, sleep mode, alert indicators, and configuration.	R/W	0x971C
0x14	VALRT	—	Configures the VCELL range outside of which alerts are generated.	R/W	0x00FF
0x16	CRATE	0.208%/hr	Approximate charge or discharge rate of the battery.	R	—
0x18	VRESET/ID	—	Configures VCELL threshold below which the IC resets itself, ID is a one-time factory-programmable identifier.	R/W	0x96__
0x1A	STATUS	—	Indicates overvoltage, undervoltage, SOC change, SOC low, and reset alerts.	R/W	0x01__
0x40 to 0x7F	TABLE	—	Configures battery parameters.	W	—
0xFE	CMD	—	Sends POR command.	R/W	0xFFFF

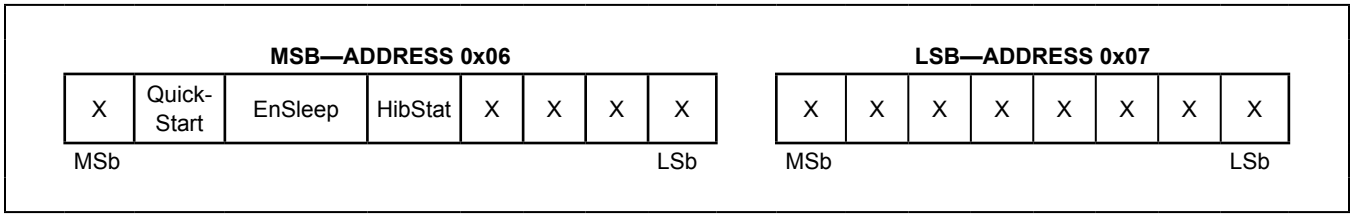


Figure 8. MODE Register Format

MODE Register (0x06)

The MODE register allows the system processor to send special commands to the IC (see Figure 8).

- **Quick-Start** generates a first estimate of OCV and SOC based on the immediate cell voltage. Use with caution; see the *Quick-Start* section.
- **EnSleep** enables sleep mode. See the *Sleep Mode* section.
- **HibStat** indicates when the IC is in hibernate mode (read only).

VERSION Register (0x08)

The value of this read-only register indicates the production version of the IC.

HIBRT Register (0x0A)

To disable hibernate mode, set HIBRT = 0x0000. To always use hibernate mode, set HIBRT = 0xFFFF (see Figure 9).

- **ActThr** (active threshold): If at any ADC sample |OCV-CELL| is greater than ActThr, the IC exits hibernate mode. 1 LSb = 1.25mV.
- **HibThr** (hibernate threshold). If the absolute value of CRATE is less than HibThr for longer than 6min, the IC enters hibernate mode. 1 LSb = 0.208%/hr.

CONFIG Register (0x0C)

- **RCOMP** is an 8-bit value that can be adjusted to optimize IC performance for different lithium chemistries or different operating temperatures. Contact Maxim for instructions for optimization. The POR value of RCOMP is 0x97.
- **SLEEP** forces the IC in or out of sleep mode if Mode. EnSleep is set. Writing 1 forces the IC to enter sleep mode, and 0 forces the IC to exit. The POR value of SLEEP is 0.
- **ALSC** (SOC change alert) enables alerting when SOC changes by at least 1%. Each alert remains until STATUS.SC is cleared, after which the alert automatically clears until SOC again changes by 1%. Do not use this alert to accumulate changes in SOC.
- **ALRT** (alert status bit) is set by the IC when an alert occurs. When this bit is set, the $\overline{ALRT}$ pin asserts low. Clear this bit to service and deassert the $\overline{ALRT}$ pin. The power-up default value for ALRT is 0. The STATUS register specifies why the $\overline{ALRT}$ pin was asserted.
- **ATHD** (empty alert threshold) sets the SOC threshold, where an interrupt is generated on the $\overline{ALRT}$ pin and can be programmed from 1% up to 32%. The value is (32 - ATHD)% (e.g., 00000b → 32%, 00001b → 31%, 00010b → 30%, 11111b → 1%). The POR value of ATHD is 0x1C, or 4%. The alert only occurs on a falling edge past this threshold.

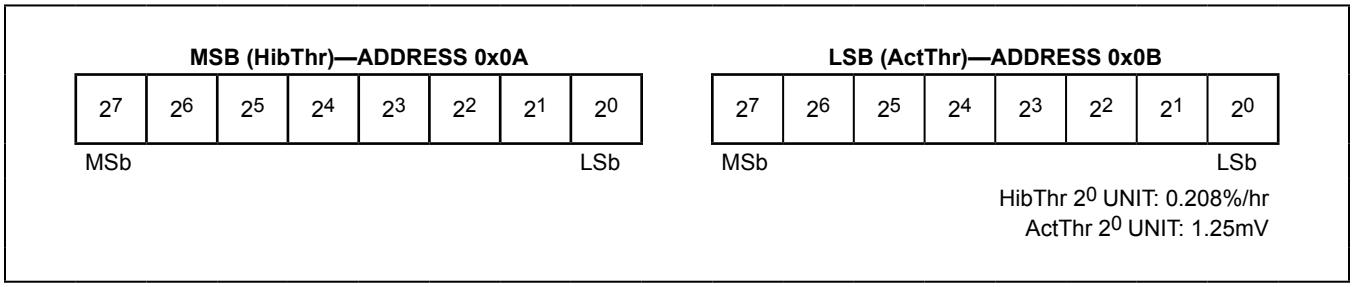


Figure 9. HIBRT Register Format

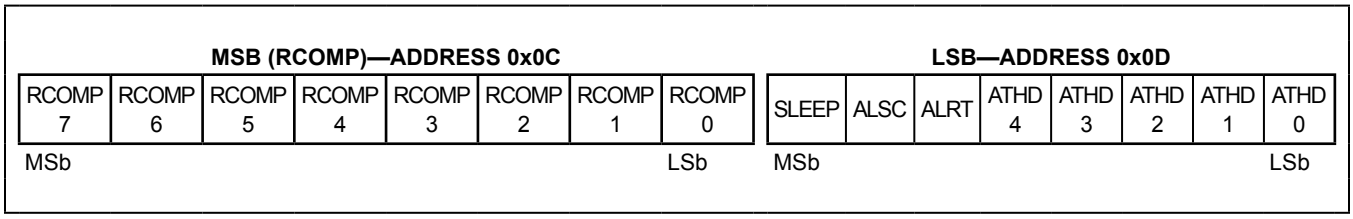


Figure 10. CONFIG Register Format

VALRT Register (0x14)

This register is divided into two thresholds: Voltage alert maximum (VALRT.MAX) and minimum (VALRT. MIN). Both registers have 1 LSb = 20mV. The IC alerts while VCELL > VALRT.MAX or VCELL < VALRT.MIN (see Figure 11).

CRATE Register (0x16)

The IC calculates an approximate value for the average SOC rate of change. 1 LSb = 0.208% per hour (not for conversion to ampere).

VRESET/ID Register (0x18)

See Figure 12.

- **ID** is an 8-bit read-only value that is one-time programmable at the factory, which can be used as an identifier to distinguish multiple cell types in production. Writes to these bits are ignored.
- **VRESET[7:1]** adjusts a fast analog comparator and a slower digital ADC threshold to detect battery removal and reinsertion. For captive batteries, set to 2.5V. For removable batteries, set to at least 300mV below the application's empty voltage, according to the desired reset threshold for your application. If the comparator is enabled, the IC resets 1ms after VCELL rises above the threshold. Otherwise, the IC resets 250ms after the VCELL register rises above the threshold.
- **Dis.** Set Dis = 1 to disable the analog comparator in hibernate mode to save approximately 0.5µA.

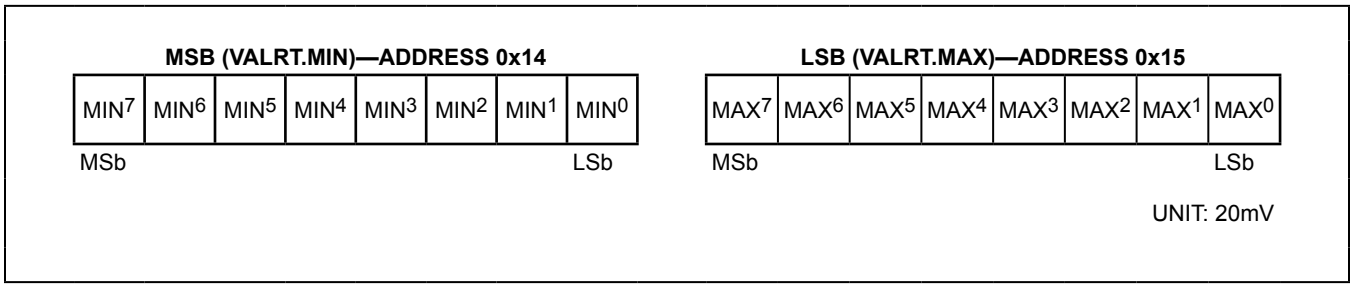


Figure 11. VALRT Register Format

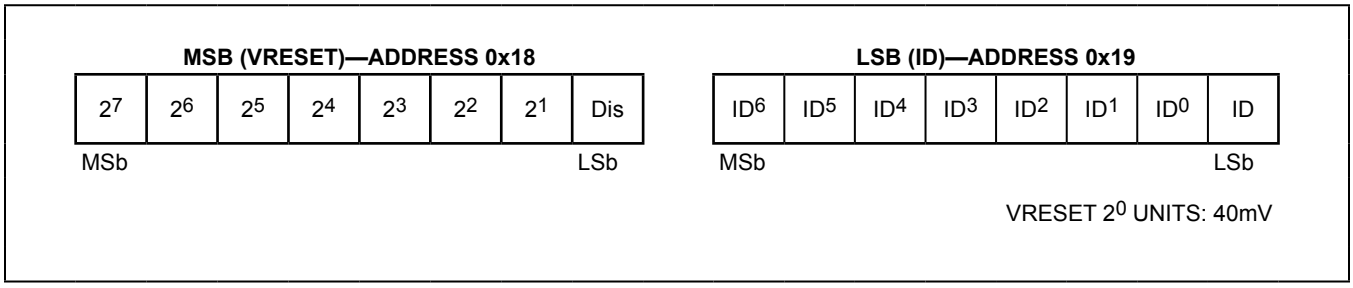


Figure 12. VRESET/ID Register Format

STATUS Register (0x1A)

An alert can indicate many different conditions. The STATUS register identifies which alert condition was met. Clear the corresponding bit after servicing the alert (see Figure 13).

Reset Indicator:

- **RI** (reset indicator) is set when the device powers up. Any time this bit is set, the IC is not configured, so the model should be loaded and the bit should be cleared.

Alert Descriptors:

These bits are set only when they cause an alert (e.g., if CONFIG.ALSC = 0, then SC is never set).

- **VH** (voltage high) is set when VCELL has been above ALRT.VALRTMAX.
- **VL** (voltage low) is set when VCELL has been below ALRT.VALRTMIN.
- **VR** (voltage reset) is set after the device has been reset if EnVr is set.
- **HD** (SOC low) is set when SOC crosses the value in CONFIG.ATHD.
- **SC** (1% SOC change) is set when SOC changes by at least 1% if CONFIG.ALSC is set.

Enable or Disable VRESET Alert:

- **EnVr** (enable voltage reset alert) when set to 1 asserts the $\overline{\text{ALRT}}$ pin when a voltage-reset event occurs under the conditions described by the VRESET/ ID register.

TABLE Registers (0x40 to 0x7F)

Contact Maxim for details on how to configure these registers. The default value is appropriate for some Li+ batteries.

To unlock the TABLE registers, write 0x57 to address 0x3F, and 0x4A to address 0x3E. While TABLE is unlocked, no ModelGauge registers are updated, so relock as soon as possible by writing 0x00 to address 0x3F, and 0x00 to address 0x3E.

CMD Register (0xFE)

Writing a value of 0x5400 to this register causes the device to completely reset as if power had been removed (see the *Power-On Reset (POR)* section). The reset occurs when the last bit has been clocked in. The IC does not respond with an I^2C ACK after this command sequence.

Application Examples

The ICs have a variety of configurations, depending on the application. Table 3 shows the most common system configurations and the proper pin connections for each.

In all cases, the system must provide pullup circuits for $\overline{\text{ALRT}}$ (if used), SDA, and SDL.

Figure 14 shows an example application for a 1S cell pack. In this example, the $\overline{\text{ALRT}}$ pin is connected to the microcontroller's interrupt input to allow the MAX17048 to signal when the battery is low. The QSTRT pin is unused in this application and is connected to GND.

Figure 15 shows a MAX17049 example application using a 2S cell pack. The MAX17049 is mounted on the system side and powered from a 3.3V supply generated by the system. The CELL pin is still connected directly to PACK+.

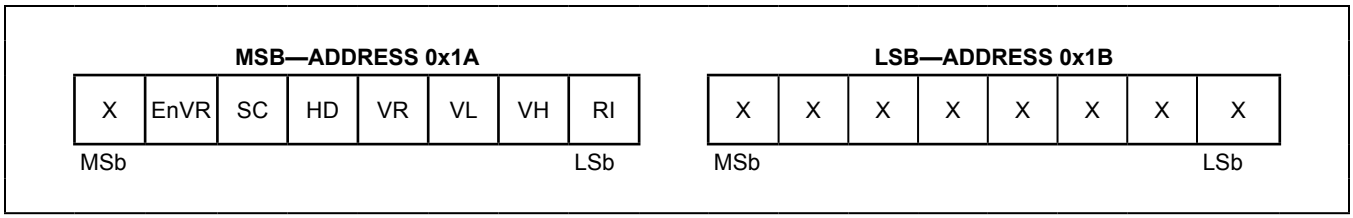


Figure 13. STATUS Register Format

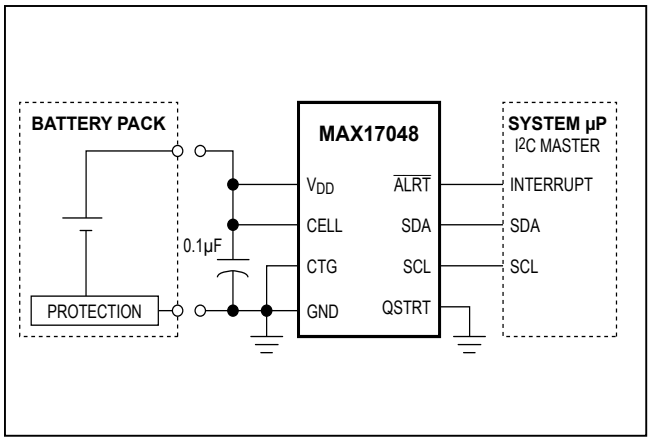


Figure 14. MAX17048 Application Circuit (1S Cell Pack)

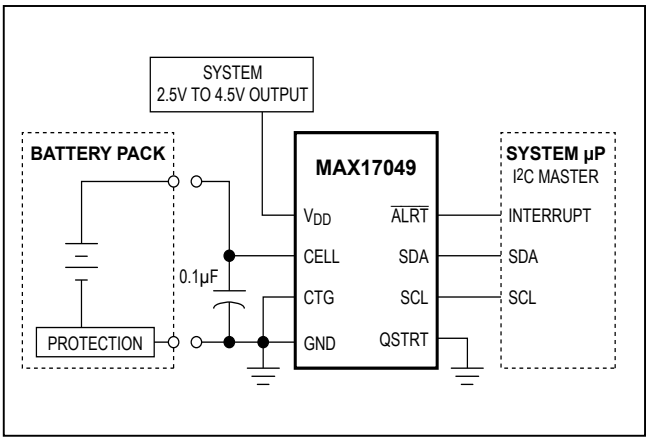


Figure 15. MAX17049 Application Circuit (2S Cell Pack)

Table 3. Possible Application Configurations

SYSTEM CONFIGURATION	IC	V_{DD}	ALRT	QSTRT
1S pack-side location	MAX17048	Power directly from battery	Leave unconnected	Connect to GND
1S host-side location	MAX17048	Power directly from battery	Leave unconnected	Connect to GND
1S host-side location, low-cell interrupt	MAX17048	Power directly from battery	Connect to system interrupt	Connect to GND
1S host-side location, hardware quick-start	MAX17048	Power directly from battery	Leave unconnected	Connect to rising-edge reset signal
2S pack-side location	MAX17049	Power from +2.5V to +4.5V LDO in pack	Leave unconnected	Connect to GND
2S host-side location	MAX17049	Power from +2.5V to +4.5V LDO or PMIC	Leave unconnected	Connect to GND
2S host-side location, low-cell interrupt	MAX17049	Power from +2.5V to +4.5V LDO or PMIC	Connect to system interrupt	Connect to GND
2S host-side location, hardware quick-start	MAX17049	Power from +2.5V to +4.5V LDO or PMIC	Leave unconnected	Connect to rising-edge reset signal

I²C Bus System

The I²C bus system supports operation as a slave-only device in a single or multislave, and single or multimaster system. Slave devices can share the bus by uniquely setting the 7-bit slave address. The I²C interface consists of a serial-data line (SDA) and serial-clock line (SCL). SDA and SCL provide bidirectional communication between the IC's slave device and a master device at speeds up to 400kHz. The IC's SDA pin operates bidirectionally; that is, when the IC receives data, SDA operates as an input, and when the IC returns data, SDA operates as an open-drain output, with the host system providing a resistive pullup. The IC always operates as a slave device, receiving and transmitting data under the control of a master device. The master initiates all transactions on the bus and generates the SCL signal, as well as the START and STOP bits, which begin and end each transaction.

Bit Transfer

One data bit is transferred during each SCL clock cycle, with the cycle defined by SCL transitioning low-to-high and then high-to-low. The SDA logic level must remain stable during the high period of the SCL clock pulse. Any change in SDA when SCL is high is interpreted as a START or STOP control signal.

Bus Idle

The bus is defined to be idle, or not busy, when no master device has control. Both SDA and SCL remain high when the bus is idle. The STOP condition is the proper method to return the bus to the idle state.

START and STOP Conditions

The master initiates transactions with a START condition (S) by forcing a high-to-low transition on SDA while SCL is high. The master terminates a transaction with a STOP condition (P), a low-to-high transition on SDA while SCL is high. A Repeated START condition (Sr) can be used in place of a STOP then START sequence to terminate one transaction and begin another without returning the bus to the idle state. In multimaster systems, a Repeated START allows the master to retain control of the bus. The START and STOP conditions are the only bus activities in which the SDA transitions when SCL is high.

Acknowledge Bits

Each byte of a data transfer is acknowledged with an acknowledge bit (A) or a no-acknowledge bit (N). Both the master and the MAX17048 slave generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low until SCL returns low. To generate a no- acknowledge (also called NAK), the receiver releases SDA before the rising edge of the acknowledge-related clock pulse and leaves SDA high until SCL returns low. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer can occur if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication.

Data Order

A byte of data consists of 8 bits ordered most significant bit (MSb) first. The least significant bit (LSb) of each byte is followed by the acknowledge bit. The IC registers composed of multibyte values are ordered MSB first. The MSB of multibyte registers is stored on even data-memory addresses.

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by a slave address (SAddr) and the read/write (R/W) bit. When the bus is idle, the ICs continuously monitor for a START condition followed by its slave address. When the ICs receive a slave address that matches the value in the slave address register, they respond with an acknowledge bit during the clock period following the R/W bit. The 7-bit slave address is fixed to 0x6C (write)/0x6D (read):

MAX17048/MAX17049 SLAVE ADDRESS	0110110

Read/Write Bit

The R/W bit following the slave address determines the data direction of subsequent bytes in the transfer. R/W = 0 selects a write transaction with the following bytes being written by the master to the slave. R/W = 1 selects a read transaction with the following bytes being read from the slave by the master (Table 4).

Table 4. I²C Protocol Key

KEY	DESCRIPTION	KEY	DESCRIPTION
S	START bit	Sr	Repeated START
SAddr	Slave address (7 bit)	W	R/W bit = 0
MAddr	Memory address byte	P	STOP bit
Data	Data byte written by master	Data	Data byte returned by slave
A	Acknowledge bit—master	A	Acknowledge bit—slave
N	No acknowledge—master	N	No acknowledge bit—slave
		R	R/W bit = 1

Bus Timing

The ICs are compatible with any bus timing up to 400kHz. No special configuration is required to operate at any speed.

I²C Command Protocols

The command protocols involve several transaction formats. The simplest format consists of the master writing the START bit, slave address, R/W bit, and then monitoring the acknowledge bit for presence of the ICs. More complex formats, such as the Write Data and Read Data, read data and execute device-specific operations. All bytes in each command format require the slave or host to return an acknowledge bit before continuing with the next byte. Table 4 shows the key that applies to the transaction formats.

Basic Transaction Formats

A write transaction transfers 2 or more data bytes to the ICs. The data transfer begins at the memory address supplied in the MAddr byte. Control of the SDA signal is retained by the master throughout the transaction, except for the acknowledge cycles:

A read transaction transfers 2 or more bytes from the ICs. Read transactions are composed of two parts, a write portion followed by a read portion, and are therefore inherently longer than a write transaction. The write portion communicates the starting point for the read operation. The read portion follows immediately, beginning with a Repeated START, slave address with R/W set to a 1. Control of SDA is assumed by the ICs, beginning with the slave address acknowledge cycle. Control of the SDA signal is retained by the ICs throughout the transaction, except for the acknowledge cycles. The master indicates the end of a read transaction by responding to the last byte it requires with a no acknowledge. This signals the ICs that control of SDA is to remain with the master following the acknowledge clock.

Write: S. SAddr W. A. MAddr. A. Data0. A. Data1. A. P

Read: S. SAddr W. A. MAddr. A. Sr. SAddr R. A. Data0. A. Data1. N. P

Write Portion | Read Portion

Write Data Protocol

The write data protocol is used to write to register to the ICs starting at memory address MAddr. Data0 represents the data written to MAddr, Data1 represents the data written to MAddr + 1, and DataN represents the last data byte, written to MAddr + N. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit:

S. SAddr W. A. MAddr. A. Data0. A. Data1. A... DataN. A. P

The MSb of the data to be stored at address MAddr can be written immediately after the MAddr byte is acknowledged. Because the address is automatically incremented after the LSb of each byte is received by the ICs, the MSb of the data at address MAddr + 1 can be written immediately after the acknowledgment of the data at address MAddr. If the bus master continues an autoincremented write transaction beyond address 4Fh, the ICs ignore the data. A valid write must include both register bytes. Data is also ignored on writes to read-only addresses. Incomplete bytes and bytes that are not acknowledged by the ICs are not written to memory.

Read Data Protocol

The read data protocol is used to read to register from the ICs starting at the memory address specified by MAddr. Both register bytes must be read in the same transaction for the register data to be valid. Data0 represents the data byte in memory location MAddr, Data1 represents the data from MAddr + 1, and DataN represents the last byte read by the master:

S. SAddr W. A. MAddr. A. Sr. SAddr R. A.
Data0. A. Data1. A... DataN. N. P

Data is returned beginning with the MSb of the data in MAddr. Because the address is automatically incremented after the LSb of each byte is returned, the MSb of the data at address MAddr + 1 is available to the host immediately after the acknowledgment of the data at address MAddr. If the bus master continues to read beyond address FFh, the ICs output data values of FFh. Addresses labeled Reserved in the memory map return undefined data. The bus master terminates the read transaction at any byte boundary by issuing a no acknowledge followed by a STOP or Repeated START.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION
MAX17048G+	-40°C to +85°C	8 TDFN-EP*	1-Cell ModelGauge IC
MAX17048G+T10	-40°C to +85°C	8 TDFN-EP*	1-Cell ModelGauge IC
MAX17048X+	-40°C to +85°C	8 WLP	1-Cell ModelGauge IC
MAX17048X+T10	-40°C to +85°C	8 WLP	1-Cell ModelGauge IC
MAX17049G+	-40°C to +85°C	8 TDFN-EP*	2-Cell ModelGauge IC
MAX17049G+T10	-40°C to +85°C	8 TDFN-EP*	2-Cell ModelGauge IC
MAX17049X+	-40°C to +85°C	8 WLP	2-Cell ModelGauge IC
MAX17049X+T10	-40°C to +85°C	8 WLP	2-Cell ModelGauge IC

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 WLP	W80B1+1	**21-0555**	Refer to **Application Note 1891**
8 TDFN-EP	T822+3	**21-0168**	**90-0065**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/12	Initial release	—
1	4/12	Corrected byte-order errors	10, 11, 13
2	8/12	Updated soldering temperature in *Absolute Maximum Ratings*; corrected Hibernate register names that were switched	2, 12, 14
3	10/12	Corrected V_{DD} pin names in *Absolute Maximum Ratings* and *Electrical Characteristics*	2, 3
4	8/13	Corrected version number	10
5	10/13	Corrected conditions for Supply Current in *Electrical Charateristics*	2
6	10/14	Updated VRESET recommendation from 40mV–80mV below 300mW empty voltage and corrected VR bit of Status register	13, 14
7	11/16	Updated front page title, description, applications, and features	1

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