

PARAMETER	SYMBOL		TEST CON	DITIONS	VALUES	UNITS
PANAIVIETEN	STIVIBUL	. TEST CONDITIONS				
Maximum DC output current at case temperature	Io	Full bridge			25 85	°C
	I _{TSM} , I _{FSM}	t = 10 ms	No voltage	Sinusoidal half wave,	357	A
Maximum peak, one-cycle non-repetitive		t = 8.3 ms	reapplied		375	
on-state or forward current		t = 10 ms	100 % V _{RRM}		300	
		t = 8.3 ms	reapplied		315	
Maximum I ² t for fusing		t = 10 ms	No voltage	initial T _J = T _J maximum	637	- A ² s
	l ² t	t = 8.3 ms	reapplied		580	
		t = 10 ms	100 % V _{RBM}		450	
		t = 8.3 ms	reapplied		410	
Maximum I ² √t for fusing	I²√t	$t=0.1$ ms to 10 ms, no voltage reapplied I^2t for time $tx=I^2\sqrt{t}\cdot\sqrt{t}x$		6365	A²√s	
Maximum value of threshold voltage	V _{T(TO)}	T _J = 125 °C		0.82	V	
Maximum level value of on-state slope resistance	r _{t1}	$T_J = 125$ °C, average power = $V_{T(TO)} \times I_{T(AV)} + r_t + (I_{T(RMS)})^2$		12	mΩ	
Maximum on-state voltage drop	V_{TM}	$I_{TM} = \pi \times I_{T(AV)}$ $T_J = 25 ^{\circ}C$		1.35	V	
Maximum forward voltage drop	V_{FM}	$I_{FM} = \pi \times I_{F(AV)}$ $T_J = 25 ^{\circ}C$		1.35	V	
Maximum non-repetitive rate of rise of turned-on current	dl/dt	$T_J = 125 ^{\circ}\text{C} \text{ from } 0.67 V_{DRM} \\ I_{TM} = \pi x I_{T(AV)}, I_g = 500 \text{mA}, t_r < 0.5 \mu\text{s}, t_p > 6 \mu\text{s}$		200	A/μs	
Maximum holding current	I _H	T _J = 25 °C anode supply = 6 V, resistive load, gate open		130	mΛ	
Maximum latching current	ΙL	T _J = 25 °C anode supply = 6 V, resistive load		250	mA	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T _J = 125 °C, exponential to 0.67 V _{DRM} gate open	200	V/µs
Maximum peak reverse and off-state leakage current at V _{RRM} , V _{DRM}	I _{RRM} , I _{DRM}	T _J = 125 °C, gate open circuit	10	mA
Maximum peak reverse leakage current	I _{RRM}	T _J = 25 °C	100	μA
RMS isolation voltage	V _{ISOL}	50 Hz, circuit to base, all terminals shorted, $T_J = 25$ °C, $t = 1$ s	2500	V

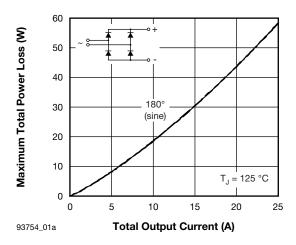
TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P_{GM}			8	W
Maximum average gate power	P _{G(AV)}			2	VV
Maximum peak gate current	I _{GM}			2	Α
Maximum peak negative gate voltage	-V _{GM}			10	V
Maximum gate voltage required to trigger	V _{GT}	T _J = -40 °C	Anode supply = 6 V resistive load	3	
		T _J = 25 °C		2	V mA
		T _J = 125 °C		1	
	I _{GT}	T _J = -40 °C		90	
Maximum gate current required to trigger		T _J = 25 °C		60	
		T _J = 125 °C		35	
Maximum gate voltage that will not trigger	V_{GD}	- T _J = 125 °C, rated V _{DRM} applied		0.2	V
Maximum gate current that will not trigger	I _{GD}			2	mA



THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction operating and storage temperature range	T _J , T _{Stg}		-40 to +125	°C	
Maximum thermal resistance, junction to case per junction	R _{thJC}	DC operation	2.24	K/W	
Maximum thermal resistance, case to heatsink	R _{thCS}	Mounting surface, smooth and greased	0.10	r√ vv	
Mounting torque, base to heatsink (1)			4	Nm	
Approximate weight			58	g	
Approximate weight			2.0	OZ.	
Case style			PACE-PA	AK (D-19)	

Note

⁽¹⁾ A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound



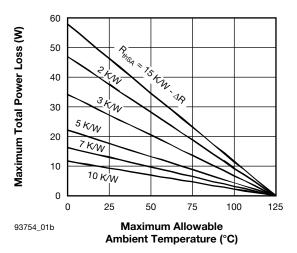


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

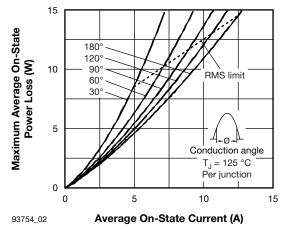


Fig. 2 - On-State Power Loss Characteristics

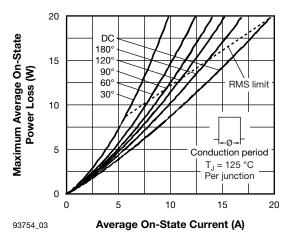


Fig. 3 - On-State Power Loss Characteristics



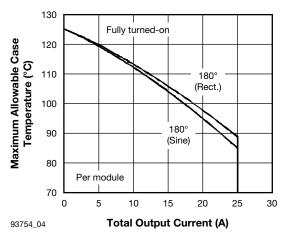


Fig. 4 - Current Ratings Characteristics

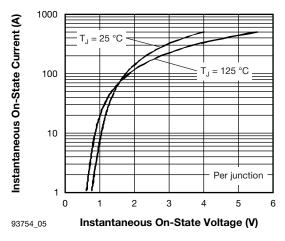


Fig. 5 - On-State Voltage Drop Characteristics

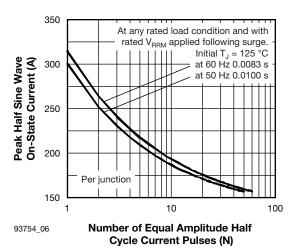


Fig. 6 - Maximum Non-Repetitive Surge Current

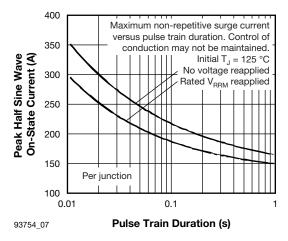


Fig. 7 - Maximum Non-Repetitive Surge Current

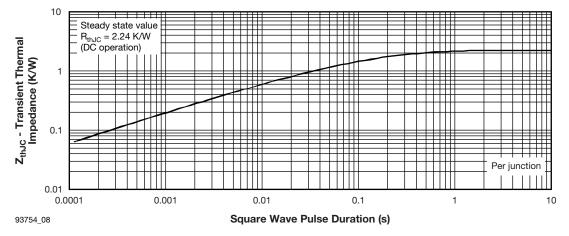


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics



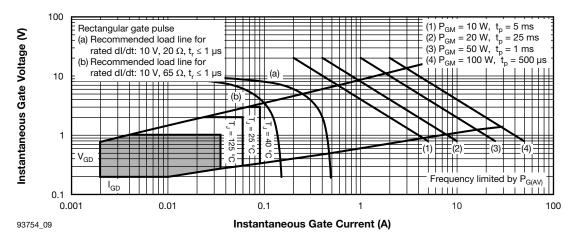
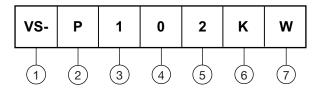


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code



- Vishay Semiconductors product
- 2 Module type
- Current rating
 - 1 = 25 A DC (P100 series)
 - 4 = 40 A DC (P400 series)
- 4 Circuit configuration
 - 0 = single phase, hybrid bridge common cathode
 - 2 = single phase, hybrid bridge doubler connection
 - 3 = single phase, all SCR Bridge
- 5 Voltage code
 - 1 = 400 V
 - 2 = 600 V
 - 3 = 800 V
 - 4 = 1000 V
 - 5 = 1200 V
- 6 K = optional voltage suppression
- 7 W = optional freewheeling diode



CIRCUIT CONFIGURATION				
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	SCHEMATIC DIAGRAM	TERMINAL POSITIONS	
Single phase, hybrid bridge common cathode	0	AC20 (+)	AC1 G1 - AC2 G2 +	
Single phase, hybrid bridge doubler connection	2	G1 9 9 G2 AC2 AC1 (+)	AC1 G1 - AC2 G2 +	
Single phase, all SCR bridge	3	G3 9 G1 AC10 AC20 G4 G2 (+)	AC2 G2 - G1 G4 - AC1 G3 +	

CODING (1)					
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	BASIC SERIES	WITH VOLTAGE SUPPRESSION	WITH FREEWHEELING DIODE	WITH BOTH VOLTAGE SUPPRESSION AND FREEWHEELING DIODE
Single phase, hybrid bridge common cathode	0	P10.	P10.K	P10.W	P10.KW
Single phase, hybrid bridge doubler connection	2	P12.	P12.K	-	-
Single phase, all SCR bridge	3	P13.	P13.K	-	-

Note

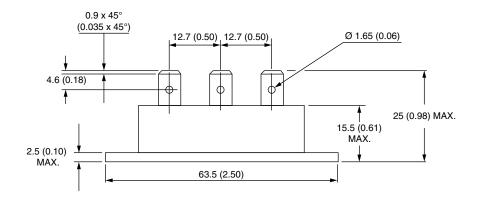
⁽¹⁾ To complete code refer to Voltage Ratings table, i.e.: for 600 V P10.W complete code is P102W

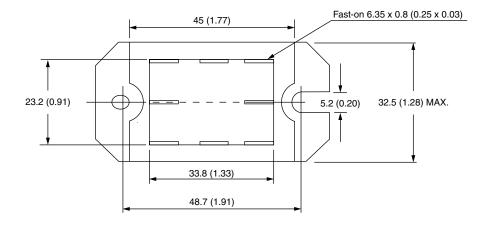
LINKS TO RELATED DOCUMENTS			
Dimensions	www.vishay.com/doc?95335		



D-19 PACE-PAK

DIMENSIONS in millimeters (inches)







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